Chapter 15

IC Photolithography

Advances in integrated circuit density are driven by the self-fulfilling prophecy known as Moore's "law," which specifies that there is an exponential increase in circuit density with time.

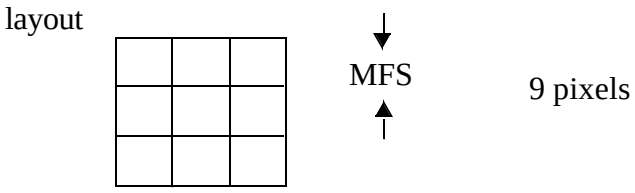
Dynamic random access memory (DRAM) chips, which are used for the main memory in a computer, represent the highest density circuits that are built. This is because they are dominated by a very regular array of storage cells that can be packed extremely densely. They serve as a kind of "technology driver" and set the pace of progress. What are the consequences of Moore's law in DRAM? About every three years, DRAM chips with a factor of four more bits become available. And the price per bit decreases! This is what we mean when we speak of a "generation."

The minimum linewidth decreases by a factor of two every two generations, so about $\sqrt{2}$ per generation. The minimum linewidth features on a chip are typicaly the poly gate length, and the minimum contact hole size.

Note: the transistor density only increases 2X per generation. How do DRAM designers get 4X per generation increases?

There are two factors at work here:

1. Increase in the chip area, about 1.5X per generation.
2. Cell design results in about a 1.3X improvement per generation.



We get the same circuit with less pixels. How? One trend is toward more three dimensional structures, with trench or stacked capacitors. Another innovation has been borderless contacts.

Year	86	89	92	95	98	01	04
DRAM	1M	4M	16M	64M	256M	1G	4G
LW(μm)	1.2	0.8	0.5	.35	.25	.18	.13
# of pixels/cell	20	17	14	12	10	8	7
area(cm^2)	.6	.9	1.3	2.0	3	4.4	6.6
# of pixels/ chip	4×10^7	1.4×10^8	4.7×10^8	1.6×10^9	5.3×10^9	1.8×10^{10}	6×10^{10}

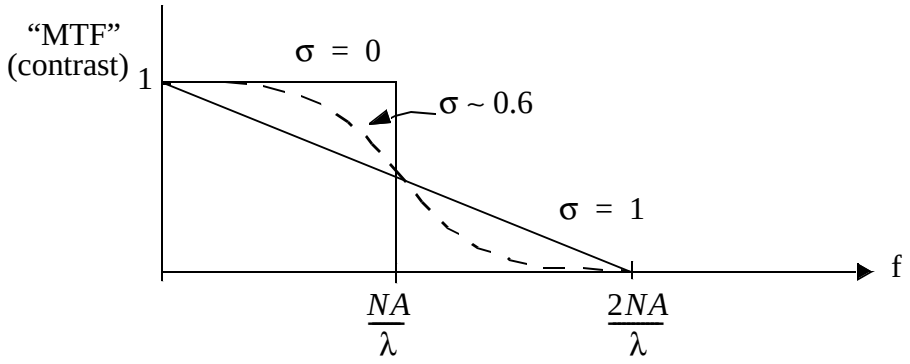
Feature size (LW) impacts on the requirements of the projection printer resolution and the highest spatial frequency it must be capable of printing.

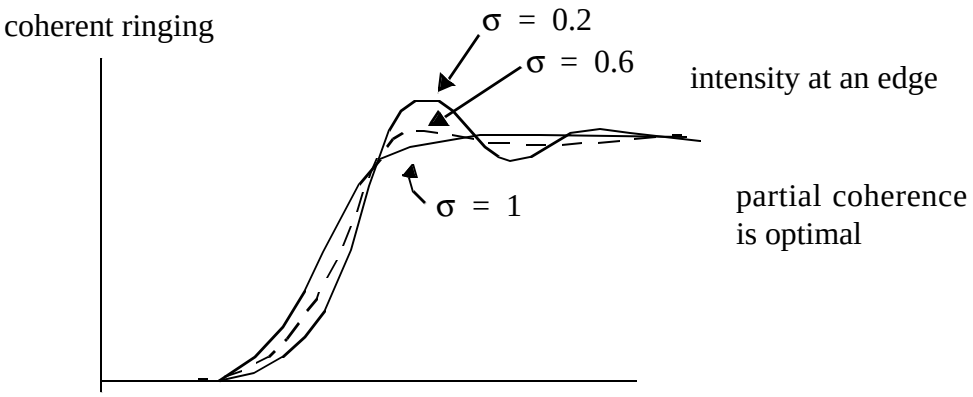
Number of pixels impacts on the projection lens complexity, its field size, and distortion. These requirements are unique to IC photolithography and are higher than for any other optics application

At 600 dpi, 1 page has 4 x 10^7 dots. This is roughly equivalent to the number of pixels in a 1 M DRAM. Printing a 64M DRAM is like photocopying 100 such sheets at once.

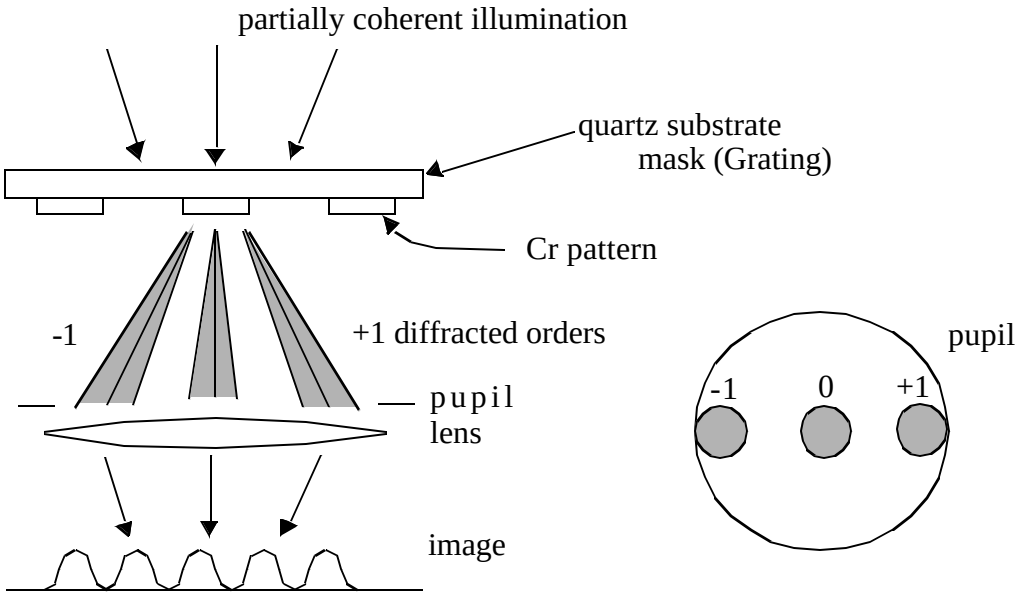
Optical projection printing

Partial coherence in lithography





Fourier Optics picture



Resolution: $= k_1 \lambda / NA$

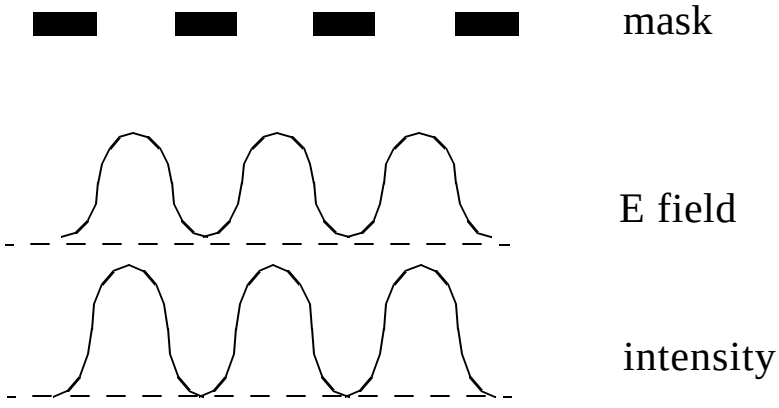
k_1: "aggressiveness" factor Rayleigh limit ~0.6

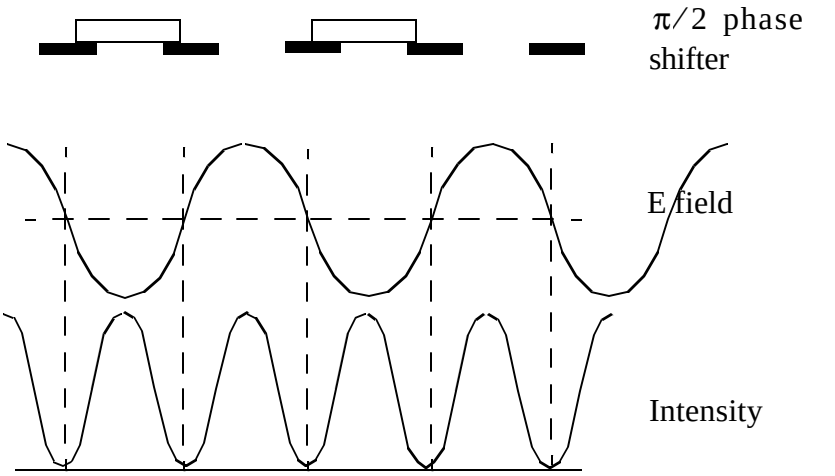
IC production today is about 0.5-0.6.

Reducing k_1 using "resolution enhancement" has received much attention.

Phase-shift masks

There are many types of phase-shift masks. One example is called Levenson style. Consider a given spatial frequency grating input:





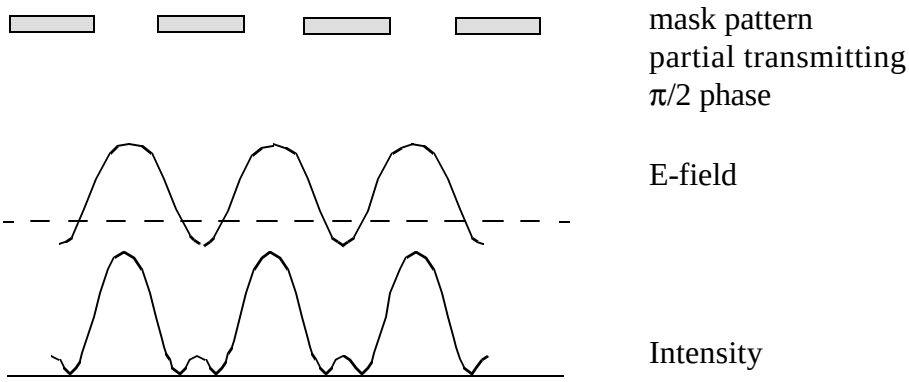
get $k_1 \sim 0.25$

good hard zero

Chromeless pure phase shifter - see vugraph

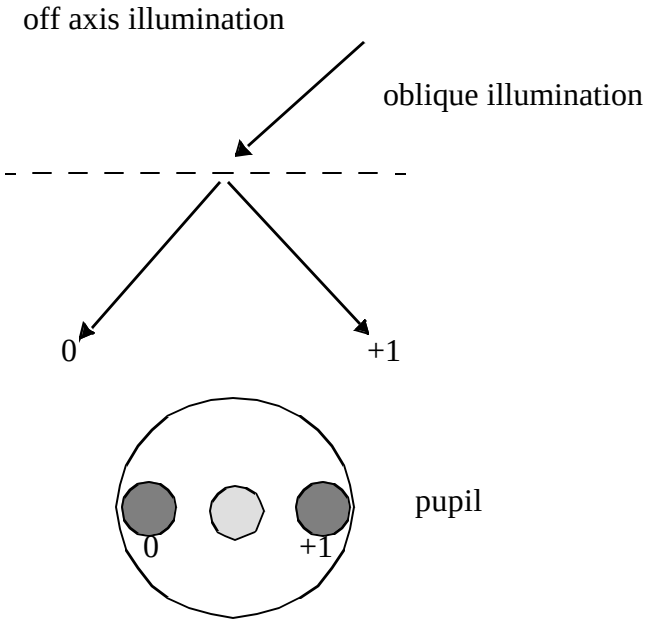
The problem is, how to get general patterns? We can't make the line ends.

The solution: an attenuated phase shifter.



improves edge slope, allows general

layouts $k_1 \sim 0.5 - 0.6$



The DC component is eliminated and this improves the contrast. However, the effect is undesireably pattern dependent. We can combine off axis illumination and attenuated phase shifters.

Ultimately $\lambda \sim 193nm \quad NA \sim 0.7 \quad k_1 \sim 0.4$. This combination can reach down close to 100 nm feature size!

And after that, the industry is now (2001) working hard on developing 157 nm lithography, which may extend down to 70 nm feature size.