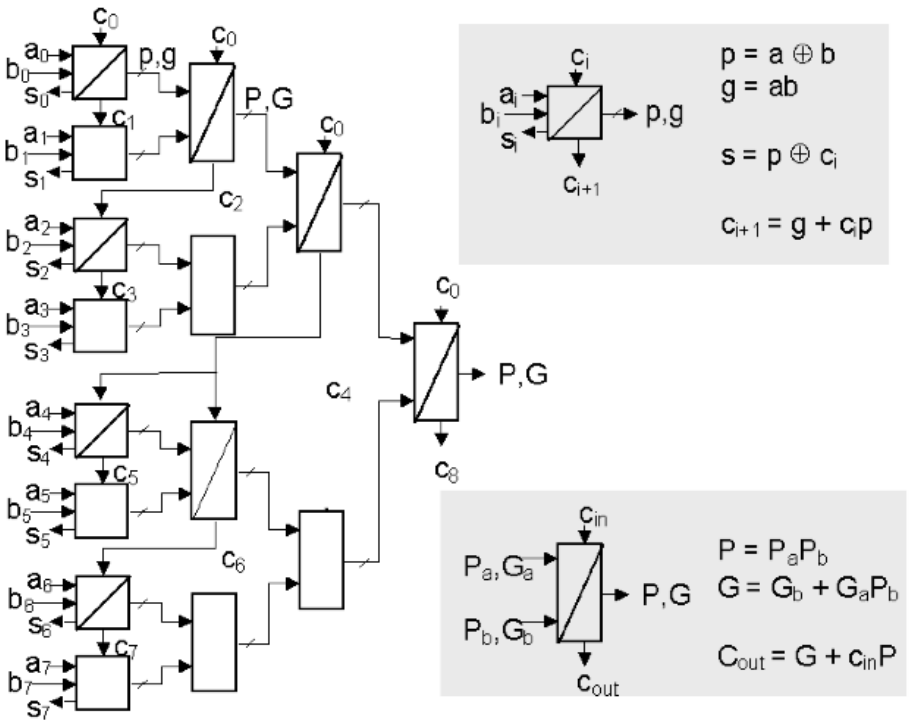
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2011

Homework Assignment 10: FSMs & Adders
Due April 14^{th}, 2pm

1. DDCA, Problem 3.24
2. DDCA, Problem 3.26
3. Implement a 2-bit adder (inputs A and B, each 2 bits wide) using two-level logic. Hint: Use a K-map
4. Suppose that your friend taking CS61C comes up with a brilliant idea to build all his adders using two-level logic. He argues that since the critical path consists of only 2 gate delays, regardless of how many bits he is adding, this adder is far superior than any other adder architectures out there. How well does his idea scale to larger adders? Is this a reasonable way of building large adders?
5. Consider the 8-bit carry-lookahead adder in Figure 1. How many 6-LUTs (only 1 output per LUT) would it take to map this adder?

Figure 1 An 8-bit carry-lookahead adder



6. Carry-select adders.

   (a) Assuming that the select groups are all of the same number of bits, and the carry delay through a full-adder cell is equal to the delay of a 2-to-1 mux, what is the optimal size select group for a 32-bit adder?

   (b) Consider the possibility of applying the carry-select idea hierarchically. The idea is that a ripple adder of n-bits can be split and implemented as a carry-select adder with group size n/2 (implemented as three ripple adders of size n/2 along with muxes). Then each of the three adders of size n/2 could be split and implemented as a carry-select adder with group size n/4, etc. By continuing this process, eventually the adder size would be 1-bit and the process ends.

   Discuss the worst-case delay through this adder. Again using big O notation, how does the delay scale with n? How does the cost (amount of hardware - number of gates or transistors) scale with n?

7. For this problem, assume that your complete library of logic components comprises 2-input AND, OR, and XOR gates and inverters. Assume that inverters have cost of one unit and a delay of one unit, and all other logic gates have cost of 2 units and delay of 2 units (ignore delays contributed by the fanout or wires). With these assumptions, a 2-input mux would be implemented with two AND gates, one OR gate, and one inverter, and would cost 7 and have delay 5. Generate a table comparing the following four adder architectures for delay and cost:

   (a) 32-bit ripple adder

   (b) 32-bit carry-select adder from the previous problem, part a.

   (c) 32-bit hierarchical carry-select adder from the previous problem, part b.

   (d) 32-bit carry look-ahead adder based on the 8-bit carry look-ahead adder presented in Figure 1.