University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2011

Homework Assignment 11: Midterm 2 Exam Review

Your "homework" for this week is to review for the midterm exam.

The exam will be closed notes and cover material from Lecture 13 through Lecture 22. Problems will be in the style of homework problems, but in some cases more challenging and requiring synthesis of several concepts. A rough outline of important topics follows:

1. Basics of DRAM internal implementation and interface.
2. Video:
   (a) Basics of Video display subsystem and framebuffers.
   (b) Line drawing acceleration algorithm operation.
3. Ethernet:
   (a) Ethernet frame organization.
   (b) Concept of packet "encapsulation" and protocol stacks.
   (c) Hardware network interface organization.
4. Timing:
   (a) Relation of clock speed to performance.
   (b) Determination of maximum clock frequency from circuit.
   (c) Origin of logic delay.
   (d) Origin of flip-flop delay.
   (e) Wire delay and mitigation.
   (f) Effects of clock skew.
5. Representations of Combinational Logic:
   (a) Definitions of the three representations for combinational logic.
   (b) Strengths, weaknesses, and uses for each CL representation.
   (c) Conversion of simple logic functions among all CL representations.
   (d) Definition and axioms of Boolean algebra Laws (theorems) of Boolean algebra.
   (e) Proving theorems via axioms.
   (f) DeMorgan's law and relationship to NAND/NOR gates.

(g) Forming SOP and POS canonical forms of Boolean expressions.

(h) Using axioms and laws of Boolean algebra for simplification.

(i) Using K-maps for deriving reduced POS and SOP forms (up to 6 variables).

(j) Exploiting function "don't care" values in logic simplication.

(k) Factoring and multi-level combinational logic.

(l) "Bubble pushing" and translating between AND/OR and NAND and NORs.

6. Synchronizer failure and design.

7. Design and operation of finite state machines:

   (a) "By hand" design procedure from state-transision-diagram (STD) to FSM circuit implementation.

   (b) Design procedure for STD to "one-hot" encoded FSM circuit.

   (c) Moore versus Mealy machine STDs and implementations and timing behavior.

   (d) Moore versus Mealy in Verilog specifications.

8. Counters:

   (a) Binary up/down counter design.

   (b) General counter design.

9. Adders Circuits:

   (a) Carry-select adder design principle, cost/performance analysis, optimization.

   (b) Carry look-ahead adder design principle, cost/performance analysis, optimization.

   (c) Bit-serial adders design and operation.

   (d) Familiarity with Virtex-5 adder carry-chain.