University of California at Berkeley
**College of Engineering**
Department of Electrical Engineering and Computer Science

EECS150, Spring 2011

Homework Assignment 2: Synchronous Digital Systems Review, FPGA basics
**Due Feb 3, 2pm**

Homework submissions are electronic, Please format your homework as plain text with PDF for any necessary figures.

1. The circuit shown below is an "equal comparitor". It takes 2 4-bit numbers and outputs a 1 iff the two input numbers are the same in every bit position.
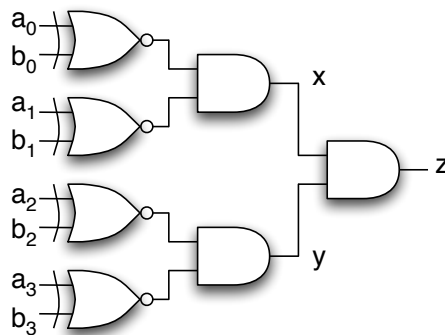
   (a) How many rows does this circuit have in its truth-table?

   (b) Write down the truth-table for the sub-circuits with outputs at node x and y.

2. Consider the 3-input circuit shown below:
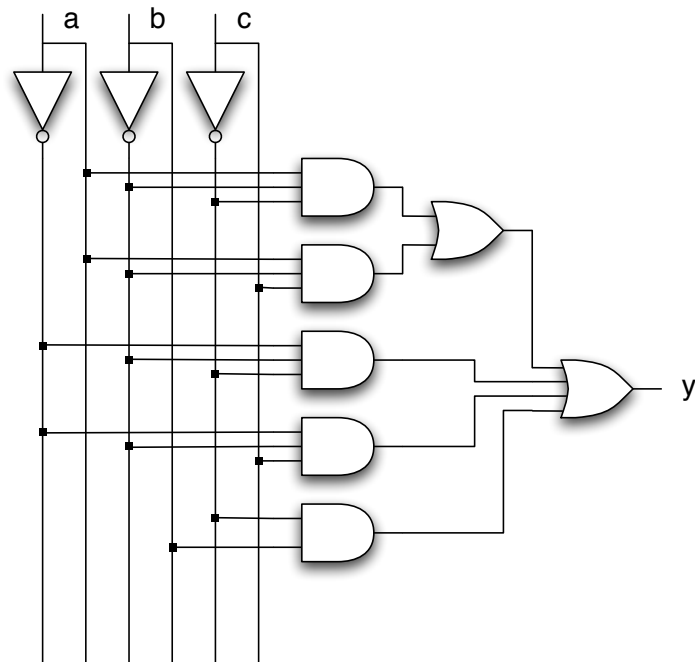
(a) Derive and write down its corresponding truth-table.

(b) Based on observing the truth-table, is it possible to simplify the circuit (remove some gates)? If so, draw the simplified circuit.

3. Imagine that you are given a collection of 3-input lookup-tables (3-LUTs) and *no other elements*, and you desire a 5-LUT. Draw a circuit diagram showing how you would create a 5-LUT from the 3-LUTs.

4. Consider the circuit shown below. Its function is an *odd parity detector*—the output is a 1 iff the number of input bits that are a 1 is odd. It has M single-bit inputs.
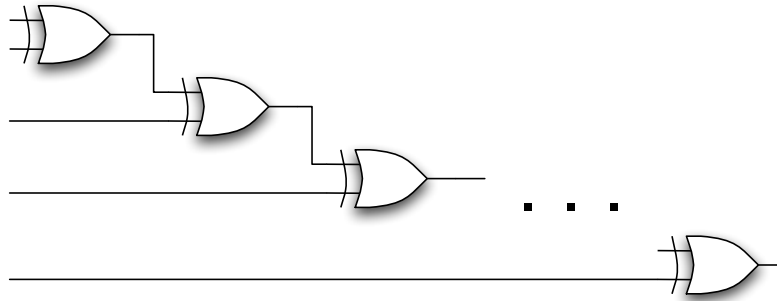

Assume that you can choose to use LUTs of any number of inputs, $N \geq 2$, to implement the function. *However, all the LUTs you use must be of the same N.*

The LUT delay and LUT chip area are related to N:

$$\Delta t = c_1 log(N), \quad area = c_2 N$$

.

(a) Without reorganizing the above circuit, write an expression for:

   i. the minimum number of LUTs needed to implement the circuit.

   ii. the delay through the resulting LUT implementation.

   iii. the total LUT area.

(b) What value of N would you choose to minimizes the delay through the circuit?

(c) Now assume you can rearrange the parity detector to help minimize delay and/or minimize area. After LUT mapping, using only 4-LUTs, write expressions for the total delay and total area. How do these compare to your answers above?

5. Imagine that you are given an FPGA with the following combinational logic block structure:
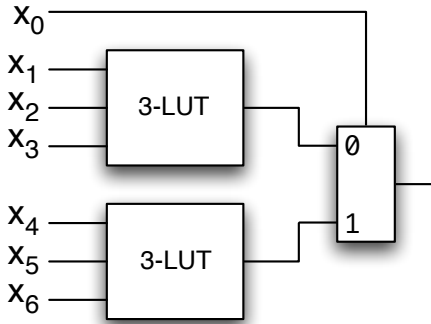

This type of structure is common in FPGAs to easily allow two N-LUTs to be combined to form a (N+1)-LUT. You are asked to implement a *4-input Multiplexor* circuit using this FPGA. How many of the above combinational logic blocks would be needed? Show your implementation.

6. Using only 4-input lookup tables (LUTs), partition the circuit shown below into as few LUTs as possible. *Do not attempt to simplify the gate-level circuit before mapping it to LUTs.* Indicate your answer by filling in the table. Fill in one row for each LUT, assigning node names from the circuit to LUT inputs and outputs. Mark unused LUT inputs with "X" (for unused).
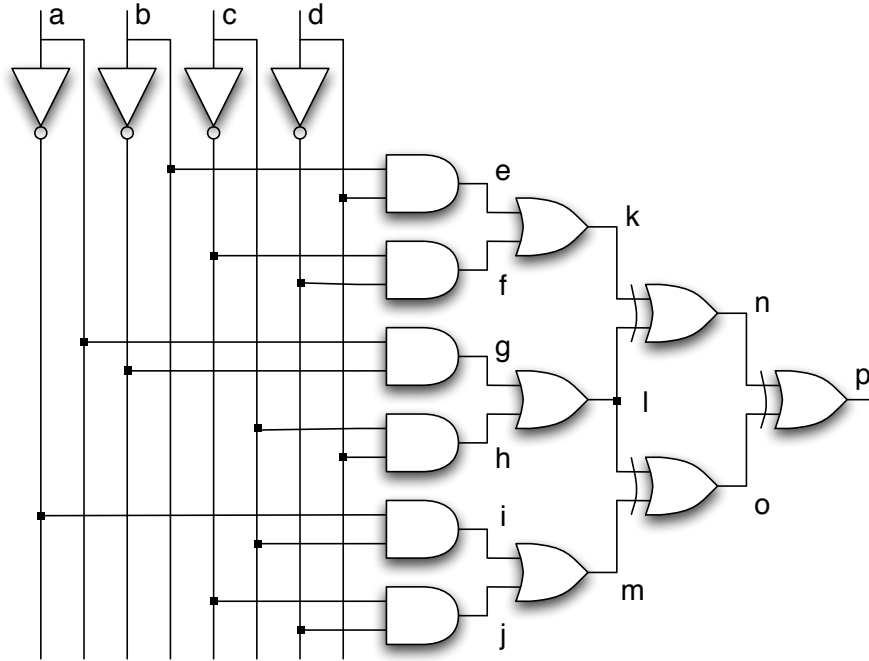


LUT #	input 1	input 2	input 3	input 4	output
1					
2					
3					
4					
5					
6					
7					
8					

7. Given the circuit shown below and the configurable logic block (CLB), partition the circuit so that it can be implemented with a collection of CLBs. Try to use as few a number of CLBs as possible. Indicate your answer by filling in the table: one row per CLB used; for the configuration bit, s, write in a 0 or 1, for all other columns write in the name of the signal wire from the logic circuit that corresponds to the CLB input or output, a 0 or 1, or nc for no connection. You may leave some rows blank or add rows.
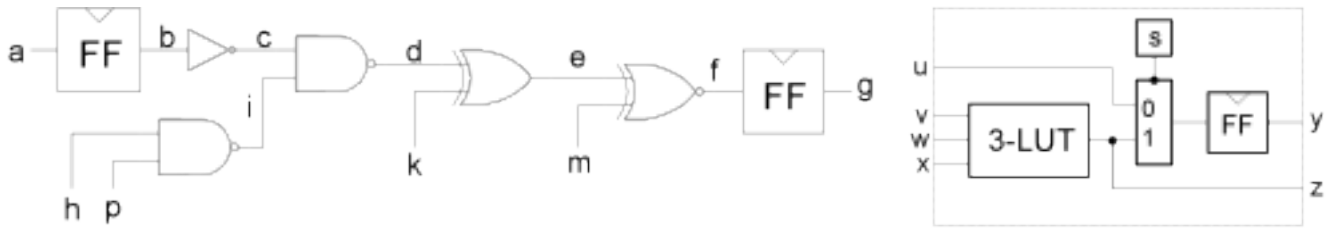
CLB #	u	v	w	x	y	z	s
1							
2							
3							
4							
5							
6							
7							
8							

8. Based on the illustration below detailing the Virtex-5 SLICEL, answer the following:
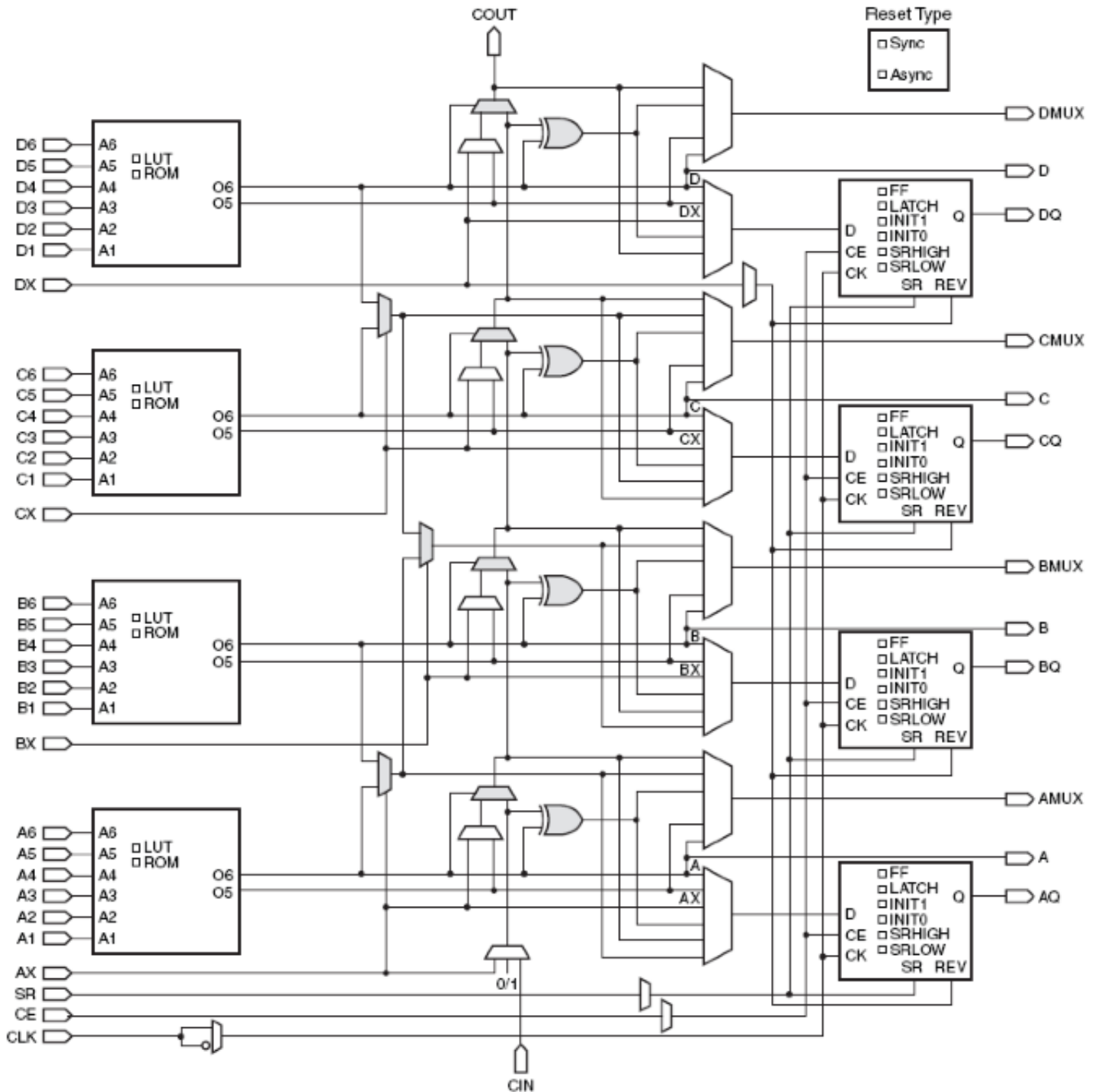
(a) Excluding the configuration bits, what is the total number of usable state bits?

(b) Suppose the slice were a "SLICEM" instead of a SLICEL. How many additional useable state bits would then be available?

(c) Based on the figure, how many bit are need to "configure" this slice?

(d) Illustrate or explain how to implement two 7-LUTs using this slice.

(e) Illustrate or explain how to implement a 12-bit equal comparator circuit using a single slice.
   Hint: You are allowed to use the carry-logic along with the LUTs.

9. For the circuit shown below, describe in words its function. Draw a clock waveform and the wavesforms at nodes x_0 through x_3 for 4 clock cycles. Assume initially x_0 through x_3 are all set to 0.