University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 3: Verilog and Sequential Logic
Due February 10^{th}, 2pm

1. The object of this problem is to design a circuit that converts from a *gray-code* to a normal binary-code.

   - A *gray-code* is a binary encoding where each symbol (word) in a sequence differs from the previous symbol by exactly one bit position. For instance, a three-bit gray-code might have the sequence: 000, 001, 011, 010, 110, 111, 101, 100, 000, ..., whereas
   - a normal 3-bit binary code has the sequence: 000, 001, 010, 011, 100, 101, 110, 111, 000, ...)

   One way to design this circuit is to wire the output of a gray-code *decoder* to a binary-encoder.

   (a) Following this idea, show the design of the two blocks at the logic gate-level and the composite design as a block-diagram.

   (b) Write the Verilog code for this design using structural verilog based on your answer above. Your design should have three module definitions.

   (c) Write a alternative description for the encoder and decoder modules using continuous assignment statements.

   (d) Write a behavioral-level Verilog description with a single module that performs both parts (converts directly from gray-code to straight binary-code.

2. Prove or disprove the following. A 2-input multiplexor circuit is a universal logic element (in the same sense as a NAND or NOR gate).
3. DDCA 4.2
4. DDCA 4.6
5. DDCA 4.8
6. DDCA 4.14
7. DDCA 4.22
8. DDCA 4.30
9. DDCA 4.38
10. DDCA 4.40
11. DDCA 4.44