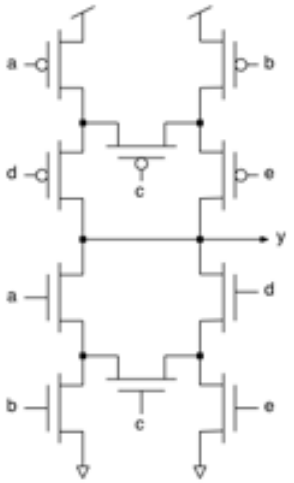
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

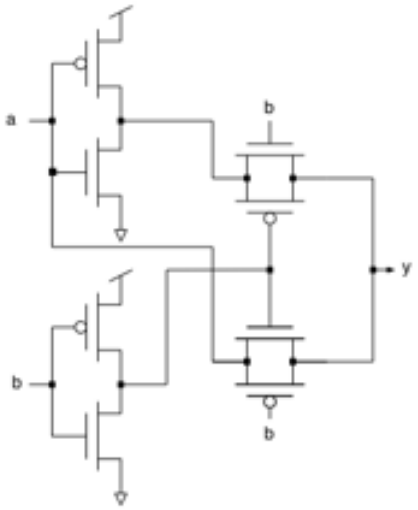
EECS150, Spring 2010

Homework Assignment 4: Verilog Testbenchs and CMOS Circuits
Due February 17^{th}, 2pm

1. DDCA 4.4.
2. DDCA 1.60
3. DDCA 1.62
4. For the CMOS circuit shown below, write a Boolean expression for the corresponding function.



5. For the CMOS circuit shown below, write a Boolean expression for the corresponding function.



6. Using transmission gates, devise a circuit that implements the following function. Try to minimize the total number of transistors.

x_1x_0	y
00	0
01	a
10	b
11	1

7. In class we discussed the idea of building a clock-generation circuit by using a closed-loop with an odd number of inverters.

   (a) Suppose we use a 7 inverters, and the inverters each have an delay of 5ps (this delay is defined as the time from when the input voltage level is $V_{dd}/2$ to when the output voltage level is $V_{dd}/2$). What would you expect to be the oscillation frequency?

   (b) How would you modify the circuit so that you could turn it on and off with a control signal?

   (c) How would you modify the circuit so that you could control the frequency (a few different frequency values is sufficient)?

8. Think about the D-flipflop design shown in class (and in the lecture notes). Is there a way to redesign this circuit to use replace some or all of the inverters and transmission gates with tri-state buffers? If possible, show such a design.

9. Starting from the CMOS edge-triggered flip-flop design shown in class, show modifications to the circuit to add the following. Try to minimize the total number of transistors:

   (a) Synchronous reset.

   (b) Synchronous set.

   (c) Clock enable.

10. Consider the implementation of a 3-LUT using CMOS transistor circuits. Assume the LUT has the following inputs and outputs: data inputs IN0, IN1, & IN2, data output OUT, a special clock signal CCLK used for shifting in configuration bits, and C for accepting configuration bits. The configuration is loaded by clocking the LUT for the appropriate number of clock cycles and feeding the proper bit pattern to the C input.

    Show the transistor level design, attempting to minimize the total number of transistors.