University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 6: SRAM and Memory Hierarchy
Due March 4^{th}, 2pm

1. Consider the organization of a 256K X 4-bit memory. Assume we desire a square internal bit-array (same number of rows as columns).

   (a) How many address bits total are required?

   (b) How many of the address bits are used for the row decoder?

   (c) How many of the address bits are used for the column muxing?

   Now assume that we desire this memory be "configurable", in the sense that with some extra control we could use it as 512K X 2-bit. Briefly, describe what changes would need to be made to the memory block to allow this flexibility.

2. Suppose you are given a collection of configurable memory blocks. Each block can be configured as a 16K X 1, or a 8K X 2, ..., 512K X 32. Your design problem requires a large memory that is 2K X 32. Which collection of smaller memory blocks would you choose and why? Show a block diagram of your design.

3. For the Xilinx device we use in the lab (LX110T), what is the total amount of on-chip SRAM bits available to the user (not configuration bits)? Now counting BlockRAM only, what is the total memory read bandwidth, in bits/second? (*Hint: maximum BlockRAM cycle rate is 400MHz.*)

4. DDCA 8.8

5. DDCA 8.12

6. DDCA 8.14

7. DDCA 8.15 (Just for fun. Will not be graded.)