University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2011

Homework Assignment 7: Midterm 1 Exam Review

Your "homework" for this week is to review for the midterm exam.

The exam will be closed notes and cover material from Lecture 1 through Lecture 12. Problems will be in the style of homework problems, but in some cases more challenging and requiring synthesis of several concepts. A rough outline of important topics follows:

1. Introductory Material:
   (a) Concept of Hierarchy in designs and example hierarchies.
   (b) Concept of cost/performance/power tradeoffs and simple examples.
2. Combinational Logic Basics:
   (a) Function of primitive logic gates. Derivation of truth tables from simple combinational logic circuits.
   (b) Signal restoration and its importance in digital circuits.
   (c) Operation and implementation of multiplexors.
3. FPGAs:
   (a) Idealized FPGA architecture model.
   (b) Details of basic FPGA PIP (programmable interconnection point).
   (c) LUT implementation details. Hierarchical LUT designs.
   (d) Partitioning logic circuits into LUTs and CLBs.
   (e) High-level details of Virtex 5 FPGAs (as presented in class).
4. State Elements and Sequential Circuits:
   (a) Basic flip-flop operation. Flip-flop Input/output/clock timing and constraints. Flip-flop reset types and functions.
   (b) "Register transfer" notion of sequential circuit timing. Waveform diagrams. Pipelining and signal feedback.
   (c) Level-sensitive latch operation. Implementation of flip-flops using level sensitive latches.
   (d) Flip-flop operation of Virtex 5 FPGA.

5. Verilog HDL:

   (a) Concept of *behavior* versus *structural* description.
   (b) Module specification and instantiation.
   (c) Basics of combinational logic and sequential circuit specification.
   (d) Continuous assignment versus procedural assignments (both blocking and non-blocking).
   (e) Specification of Finite State Machines.
   (f) Use of module parameters and "generate" constructs.
   (g) Basic steps of logic synthesis and examples of how Verilog specifications are converted to circuits.
   (h) Case versus nested If-else.
   (i) Differences between HDL for synthesis and for simulation.
   (j) Techniques for writing test-benches in Verilog.

6. Physical Design:

   (a) Chip-level design alternatives and pros and cons of each.
   (b) Economics of FPGAs versus ASICs.
   (c) CMOS circuits for basic logic gates, multiplexors, and flip-flops. CMOS transmission gates.
   (d) Implementation of tri-state buffers and their use for bidirectional communication.

7. CPU microarchitecture:

   (a) Implementation of a single-cycle processor from ISA description.
   (b) Processor pipelining: impact on performance, hazard types and resolution.
   (c) Detailed operation of 5 and 3-stage MIPS pipeline.
   (d) Serial communication and UART basics.
   (e) Memory mapped CPU I/O and polling implementation.

8. Memory Blocks:

   (a) Naming conventions.
   (b) Internal organization.
   (c) SRAM Cell implementation.
   (d) Multiported memory internal organization.
   (e) Cascading memory blocks to increase width/depth/number of ports.
   (f) Virtex 5 block-RAM and LUT-RAM details and differences.
   (g) Verilog patterns for inferring RAMs
   (h) Operation and implementation of FIFO memories.
   (i) Cache organizations and operation. Cache design options and tradeoffs with respect to performance and cost.