University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2010

Homework Assignment 8: DRAM, Video, Enet, Timing
Due March 17^{th}, 2pm

1. DRAM.

   (a) Common practice in most computer systems is to use SRAM for caches and DRAM for main memory. Briefly explain why this is so. Why, for instance, wouldn't we choose SRAM for main memory and DRAM for caches?

   (b) What is the largest capacity DRAM chips currently available? Approximately what is their price per chip?

   (c) Based on the timing diagrams in the lectures slides for DRAM access, what would be the DRAM read bandwidth for a long string of "unit stride" accesses. Unit stride means the accesses are to consecutive memory addresses.

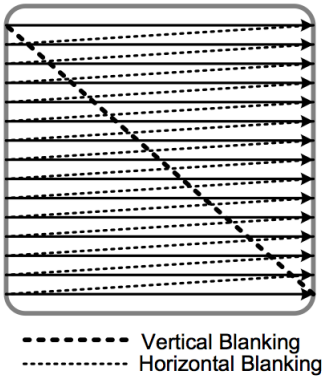
   (d) What would be the read bandwidth for a long string of accesses to random addresses?

2. Video Display. Suppose we are using a 1024x768 display at 75Hz, meaning 75 frames are sent to the display every second.

   (a) What is the pixel rate? (On average how many pixels are sent to the display per second?)

   (b) For 24-bit color, what is the data rate?

   (c) The display has blanking intervals where the beam must go across the screen to start the next line or frame. Each horizontal line is scanned left-to-right, from top line to bottom line. The horizontal blanking interval is like writing additional invisible pixels to the end of the line, and the vertical blanking interval is like writing additional invisible lines to the end of the frame.



   It turns out that the horizontal blanking interval, which occurs after each line, is 3.65μs. The vertical blanking interval, which occurs after each frame, is 0.533ms. What is the pixel frequency (clock used by display) for sending pixels to the 1024x768 @ 75Hz display?

(d) What is the horizontal blanking interval in terms of number of pixels? What is the vertical blanking interval in terms of number of lines?

3. Ethernet. Given a 10/100 Ethernet link operating at a line rate of 100Mb/s (Assume the producer is able to supply data at arbitrary high rates), how much time would a transfer of 10 million bytes of raw data take (no protocol embedded into the Ethernet frames)?

   Assume that no inter-frame gap is needed, and "Jumbo" frames are disallowed.

4. Video and DRAM. You are an engineer at AcmeVideo, Inc. Your current display system has the following specifications:

   - 30 frames/second
   - black & white display (only one color component for each pixel)
   - 8 bits per pixel
   - 600 pixels/line
   - 600 lines/frame

   The display system uses a frame buffer based on a SDRAM with the following specifications:

   - 8-bit data interface
   - 4+L cycles per read or write access, where L = burst length (consecutive memory accesses, 1 per cycle)
   - Maximum L = 6
   - 48 MHz clock frequency

   Your marketing department would like to bring out a new product based on your current display system. It will have a display monitor that can be rotated 90 degrees and a mechanical switch to detect when the monitor is rotated. When the monitor is rotated, the display system must rotate the video output by 90 degrees to compensate. Your VP of engineering has decided that the cheapest way to achieve this compensation is to transform the image using the frame-buffer; it will be written to the frame buffer row-by-row, but read out column-by-column.

   (a) Using the existing frame buffer and changing the control logic, is it possible to support the rotation operation and maintain the display specifications? Show your work.

   (b) Adhering to all other specs, what is the maximum display refresh rate when rotated?

Before starting the problems below, please read sections 3.5.1-3.5.3 of DDCA.

5. DDCA, Problem 3.30

6. DDCA, Problem 3.32

7. Timing. Consider a CMOS AND gate implemented as a NAND gate followed by an inverter. Assume the inverter propagation delay is defined as follows (units in picoseconds):

$$\tau_p = 50 + 100 \cdot f$$

Where **f** is the fanout of the inverter, expressed in number of transistor gate inputs. For example, inverters contribute 2 to **f** and one input of a 2-input NOR gate contributes 2. **Note to people who have taken EE141: this is not the $f = \frac{C_{out}}{C_{in}}$ definition of fanout used in EE141**. Assume this inverter has the same propagation delay for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions.

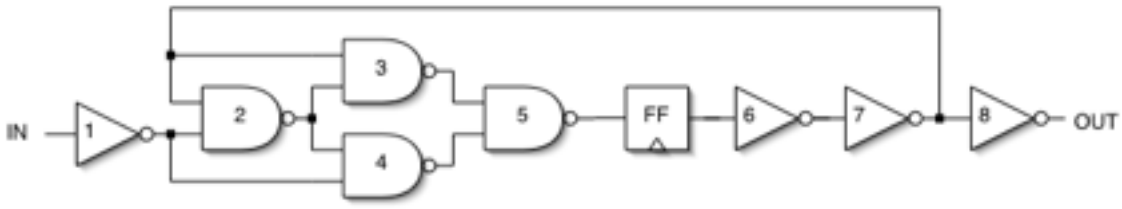
The NAND gate propagation delay is expressed as (in ps):

$$\tau_{p0\rightarrow1} = 100 + 75 \cdot f$$

$$\tau_{p1\rightarrow0} = 100 + 125 \cdot f$$

For the $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, respectively. Write the expressions for the $0 \rightarrow 1$ and $1 \rightarrow 0$ propagation delays of the AND gate.

8. Timing. Consider the circuit show here:



- The propagation delay (for both high-to-low and low-to-high transitions) of the inverters are $\tau_p = 50 + 100 \cdot f$ (in ps).
- The propagation delay (for both kinds of transitions) of the NAND gates are $\tau_p = 100 + 150 \cdot f$ (in ps).
- The flip-flop $t_{setup} = t_{clk-q} = 50ps$.
- There is no clock skew.
- Assume there are three instances of this circuit cascaded together, we are focusing our analysis on the middle one.

(a) Mark the critical path in the diagram.

(b) List the gates of the critical path (by gate number) in the order of signal propagation and their associated delays. Remember to account for the fanout.

(c) What is the minimum clock period **T** for correct operation of this circuit?