
CS 150

Digital Design

Lecture 13 – DRAM

2011-3-1

John Wawrzynek

today's lecturer: John Lazzaro

TAs: Michael Eastham and Austin Douppnik

www-inst.eecs.berkeley.edu/~cs150/

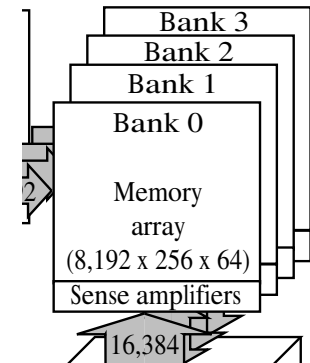


Today's Lecture: DRAM

* DRAM, Xilinx, and You

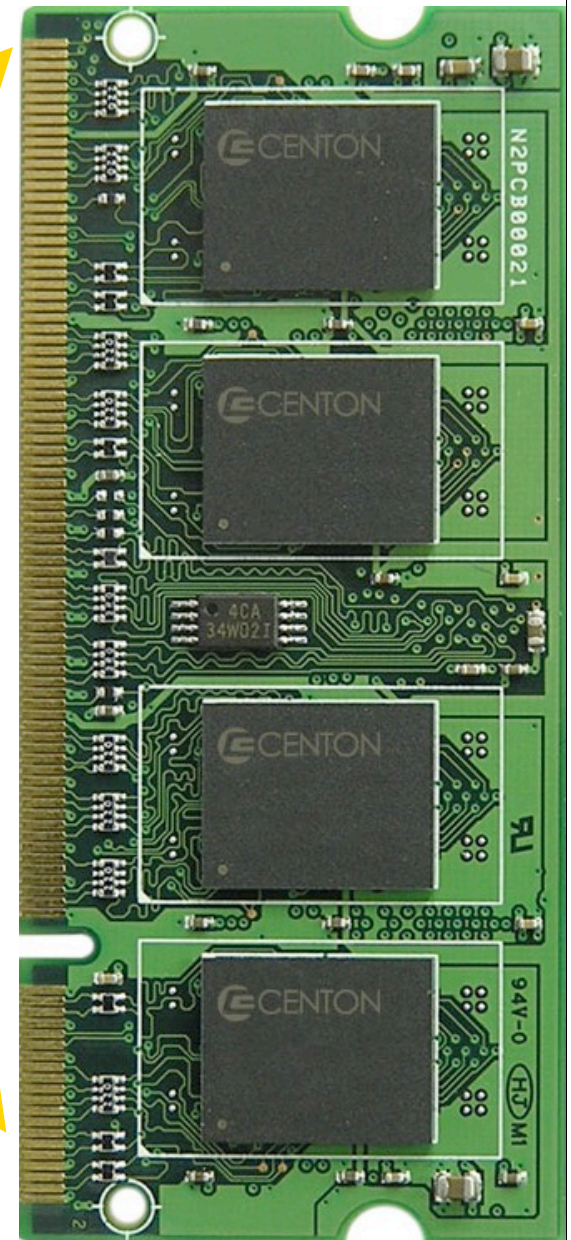
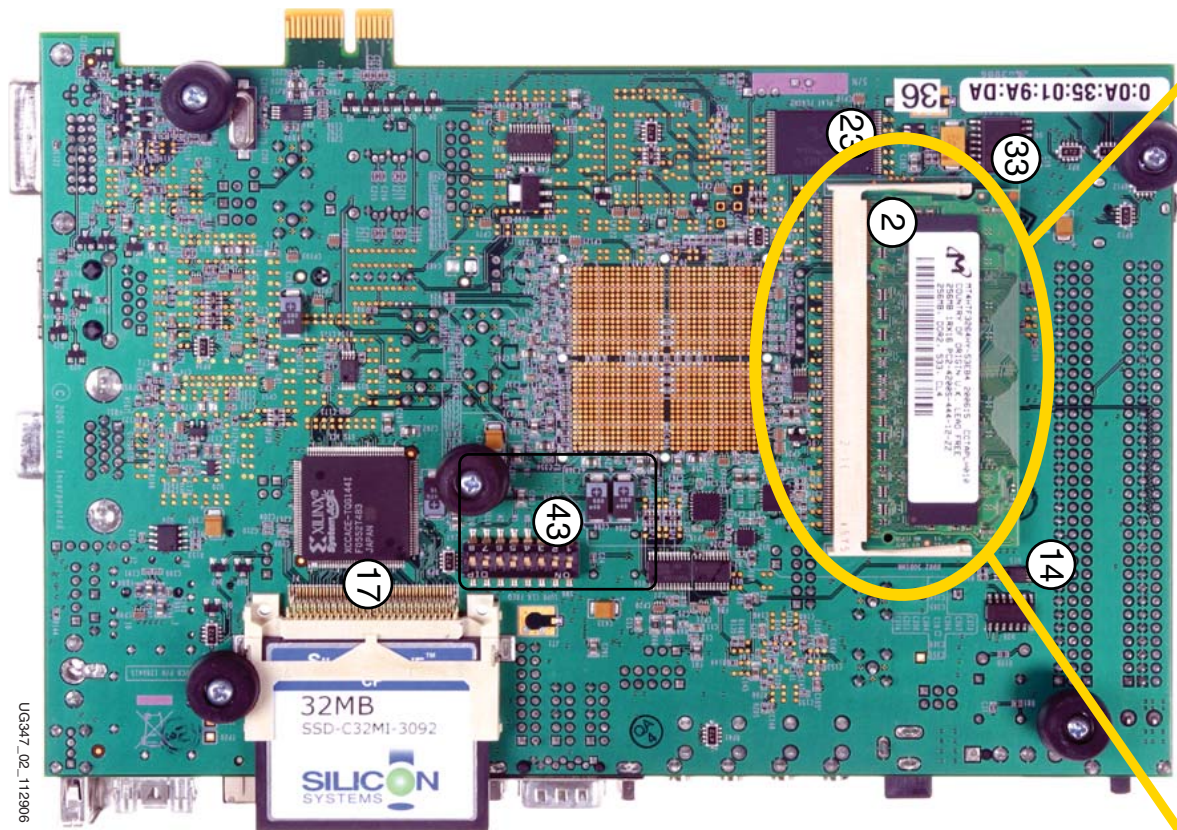
* DRAM: Bottom-up

* DRAM: Top-down



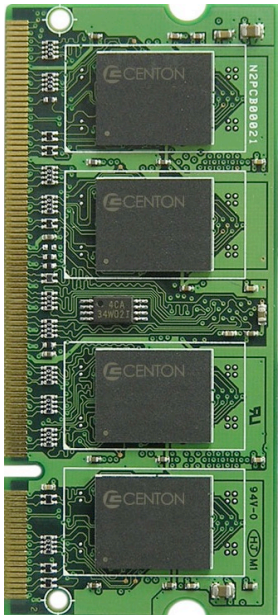
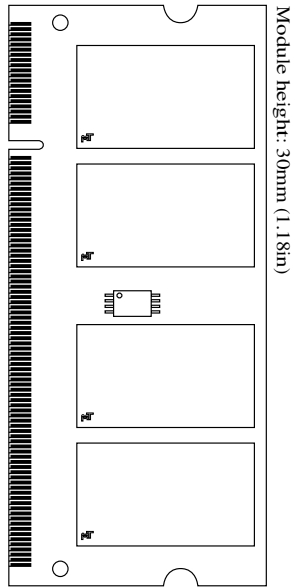
DDR2 SO-DIMM on ML505 Board

DDR2: Double-Data Rate, 2nd generation

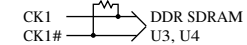
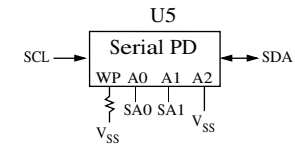
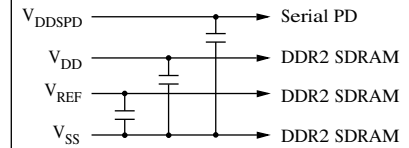
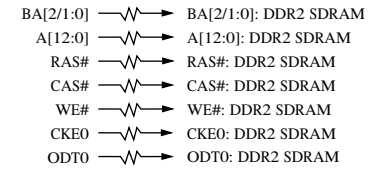
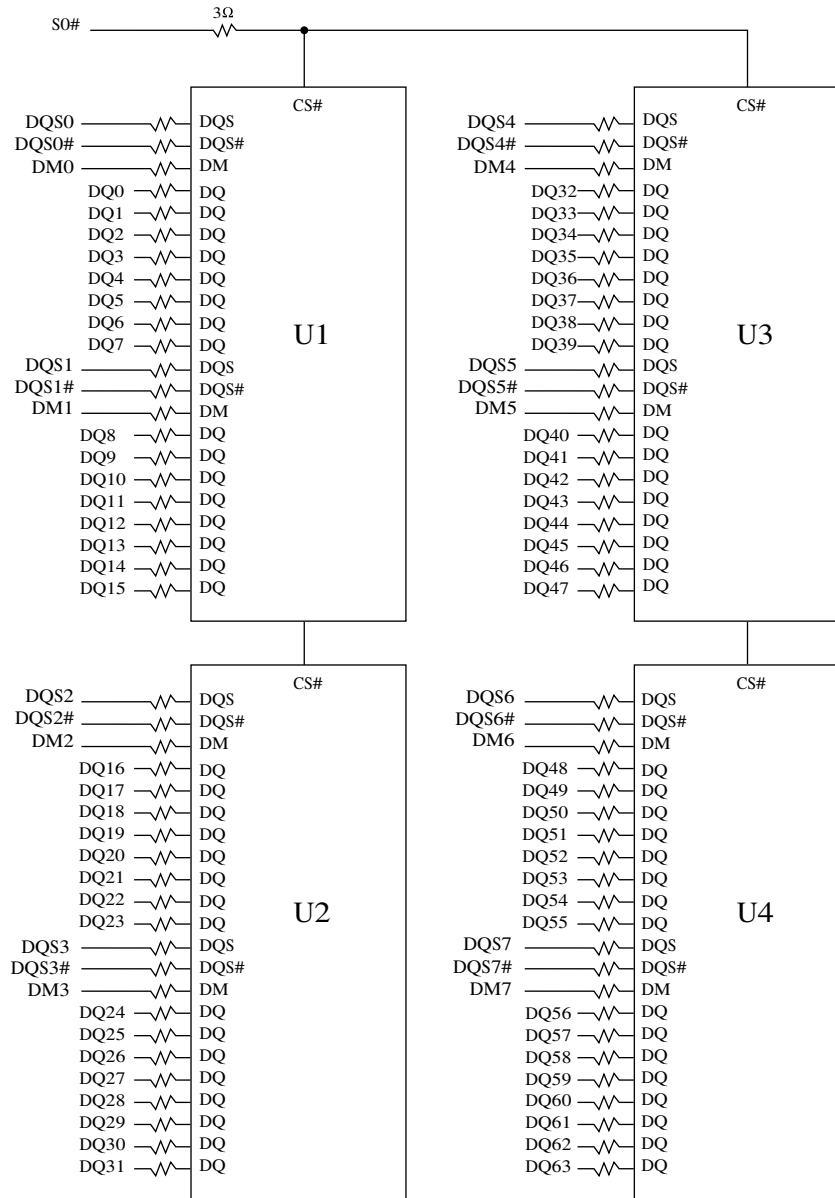


SO-DIMM: Small-Outline,
Dual Inline Memory Module

DDR2 SO-DIMM Module



CS 150 L13: DRAM



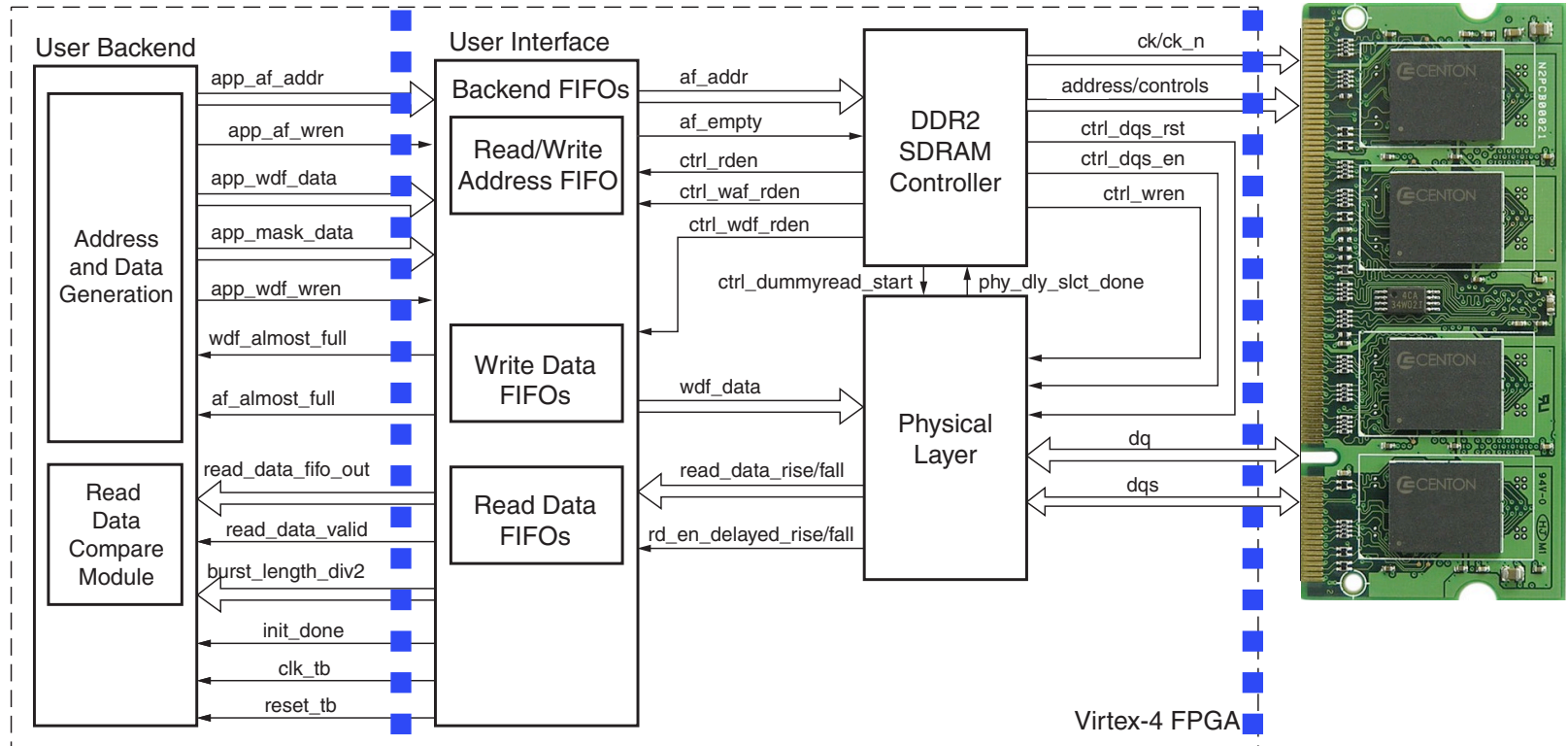
DRAM chips are wired in parallel and run in lockstep.

Project controller: Xilinx-supplied IP

Your project's Verilog code sees a FIFO R/W interface.

Xilinx IP translates FIFO requests to DRAM commands.

DDR2 SO-DIMM



UG086_c3_07_091508

Today's Lecture: DRAM

* DRAM, Xilinx, and You

* **DRAM: Bottom-up** To understand the DRAM controller, you need to understand how a DRAM chip works. Otherwise, it just seems like **magic.**

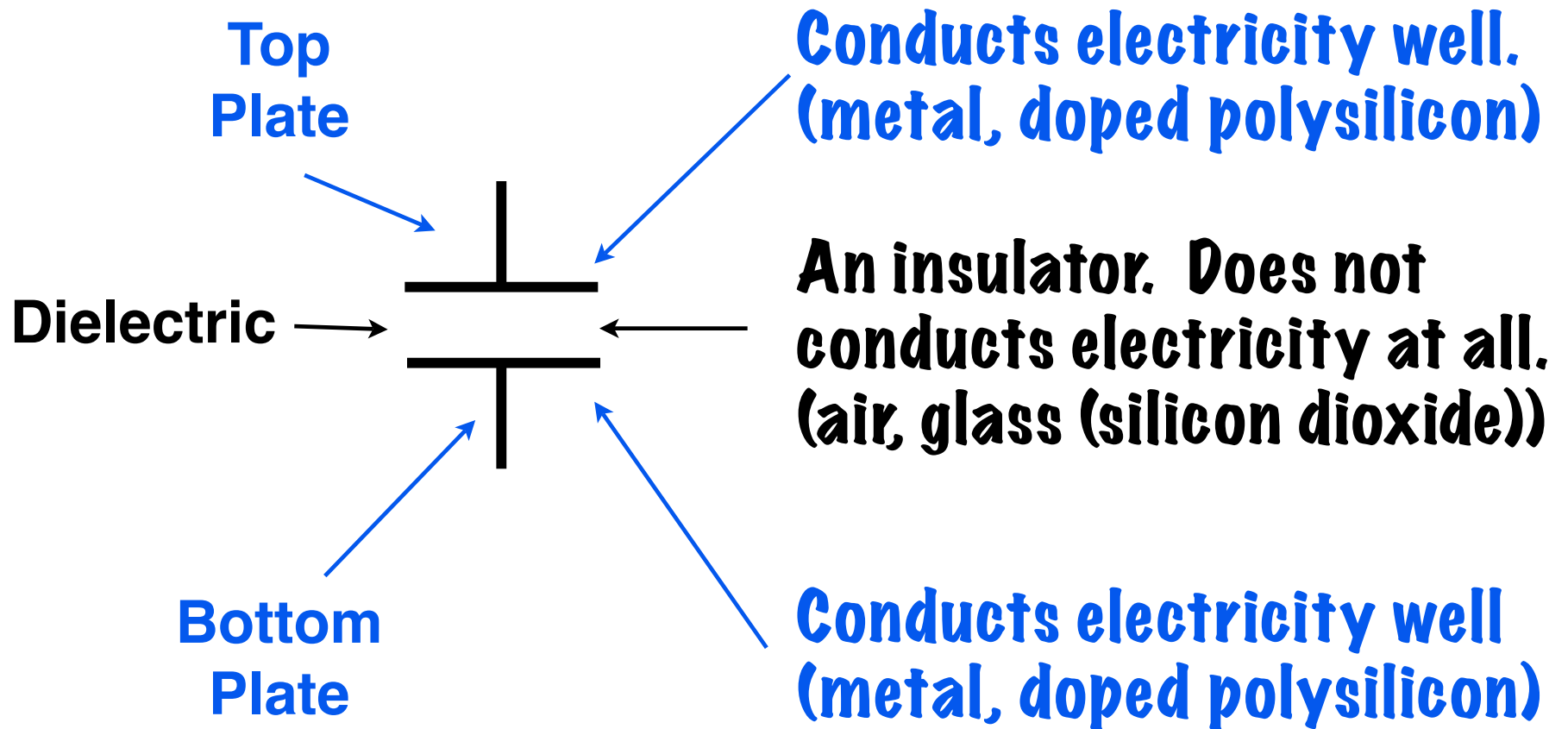
* DRAM: Top-down



Capacitance

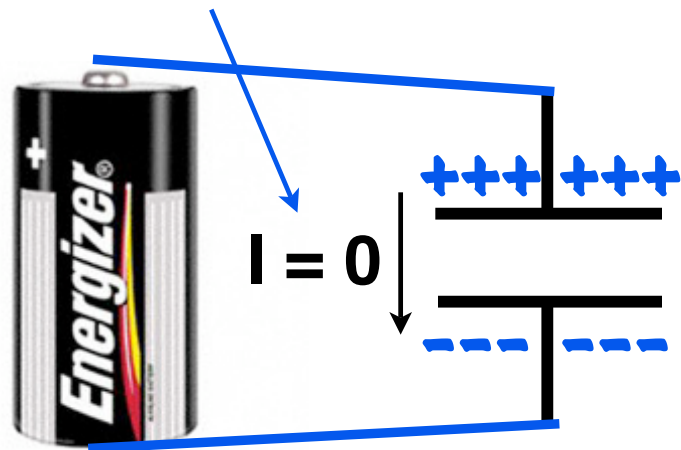


Recall: Building a capacitor



Recall: Capacitors in action

Because the dielectric is an insulator, and does not conduct.



After circuit “settles” ...

$$Q = C V = C * 1.5 \text{ Volts (D cell)}$$

Q: Charge stored on capacitor

C: The capacitance of the device: function of device shape and type of dielectric.

After battery is removed:

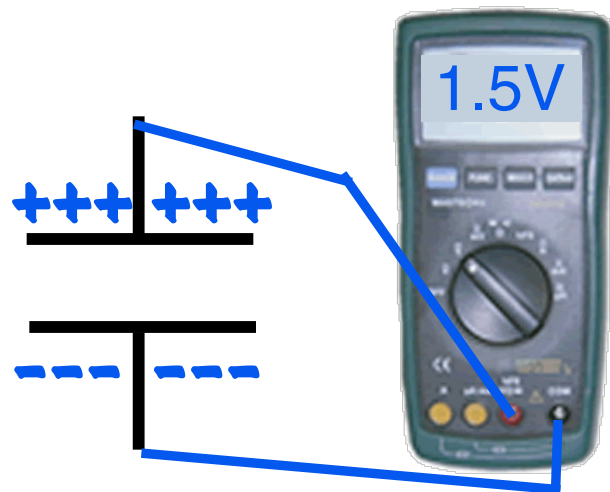
$$\text{Still, } Q = C * 1.5 \text{ Volts}$$

Capacitor “remembers” charge



Storing computational state as charge

State is coded as the amount of **energy** stored by a device.



State is read by **sensing** the amount of energy

Problems: **noise** changes Q (up or down), **parasitics** leak or source Q . Fortunately, Q **cannot change instantaneously**, but that only gets us in the ballpark.

MOS Transistors

Two diodes and a capacitor in an interesting arrangement. So, we begin with a diode review ...

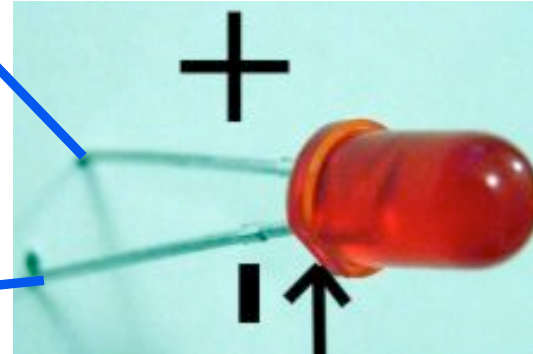
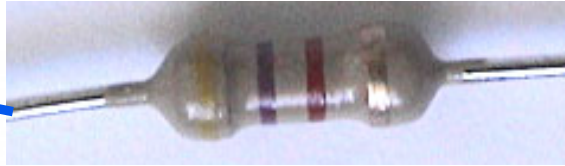


Diodes in action ...

Resistor

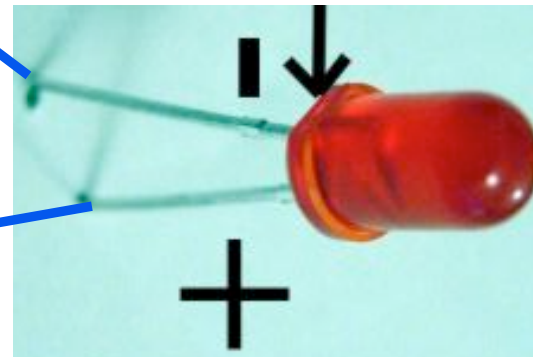
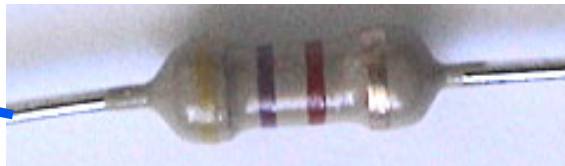
Light emitting diode (LED)

Light on?



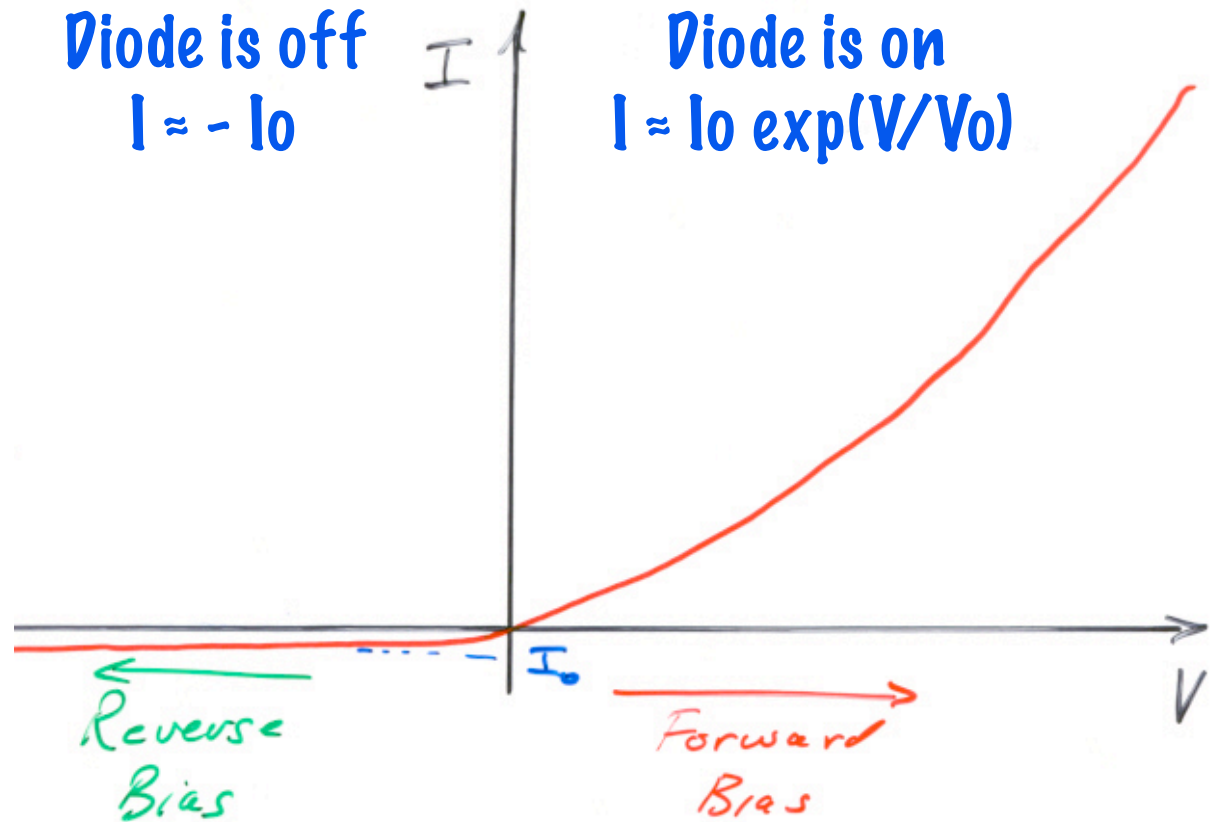
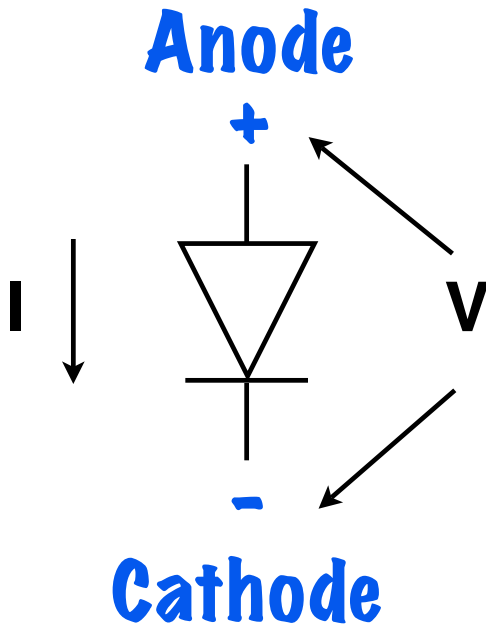
Yes!

Light on?



No!

Diodes: Current vs Voltage

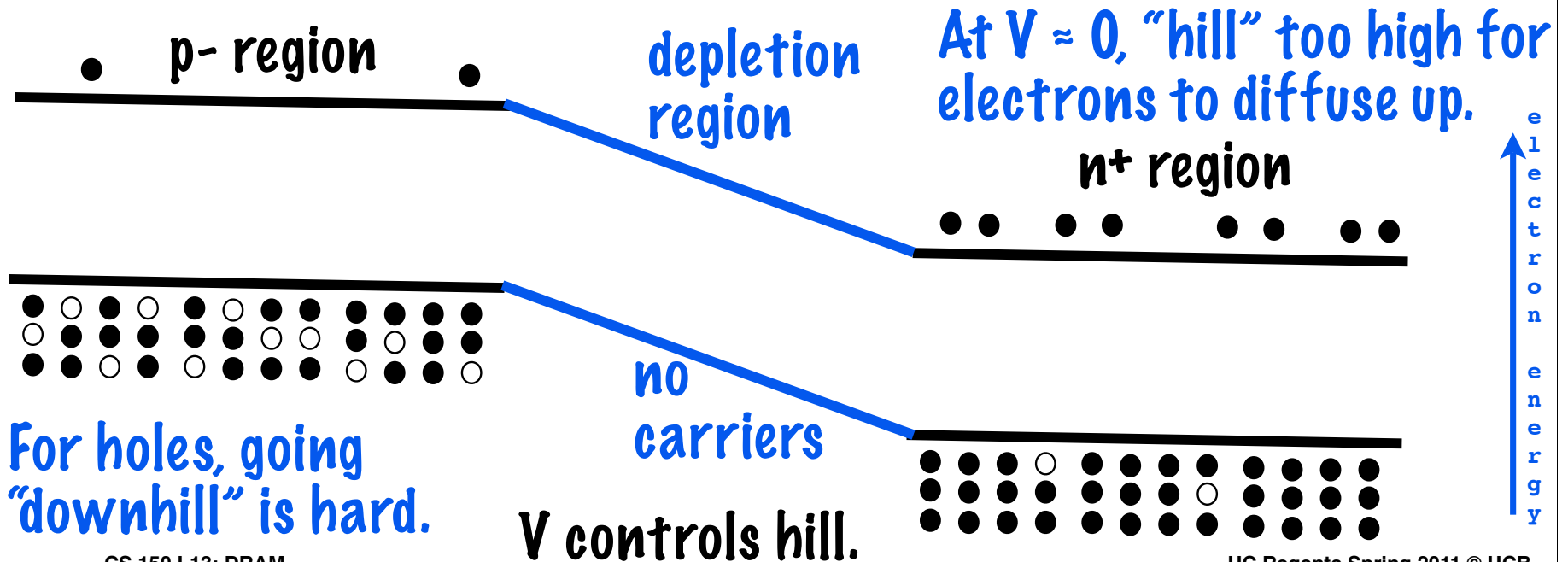
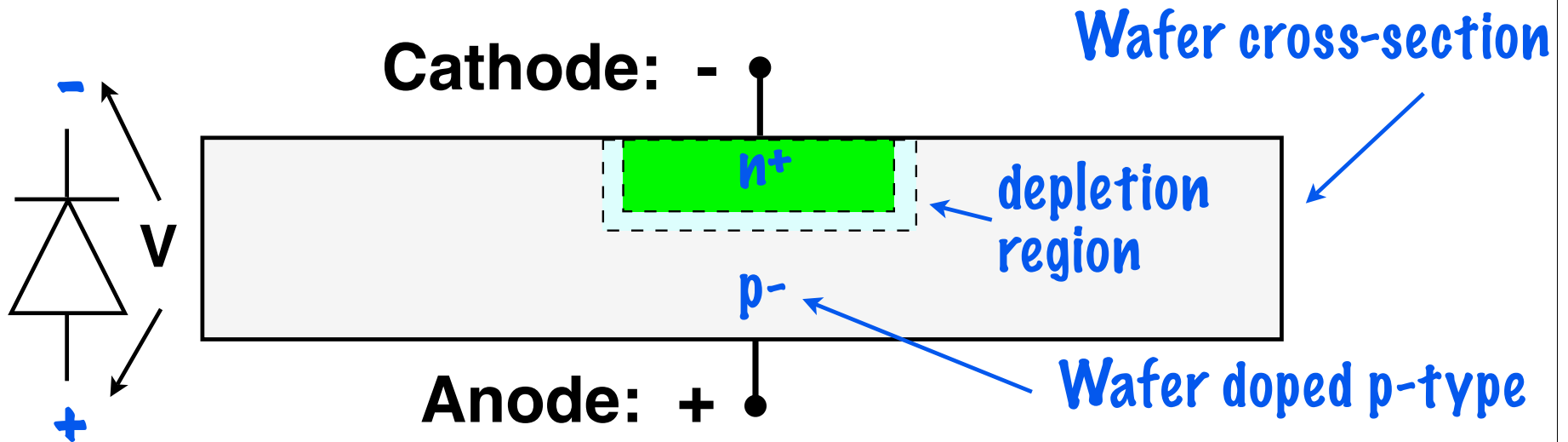


$$I = I_0 [\exp(V/V_0) - 1]$$

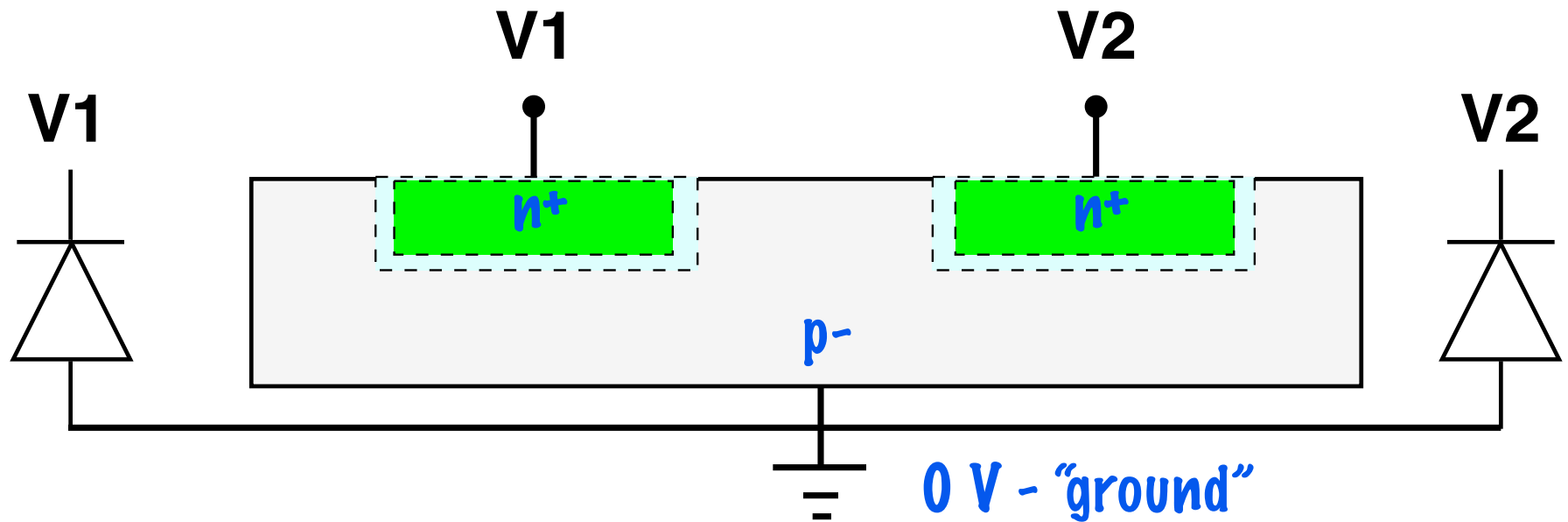
I_0 range: fA to nA

V_0 range: 25mV to 60 mV

How to make a silicon diode ...



Note: IC Diodes are biased “off”!



$V1, V2 > 0V$. Diodes “off”, only current is I_0 “leakage”.

$$I = I_0 [\exp(V/V_0) - 1]$$

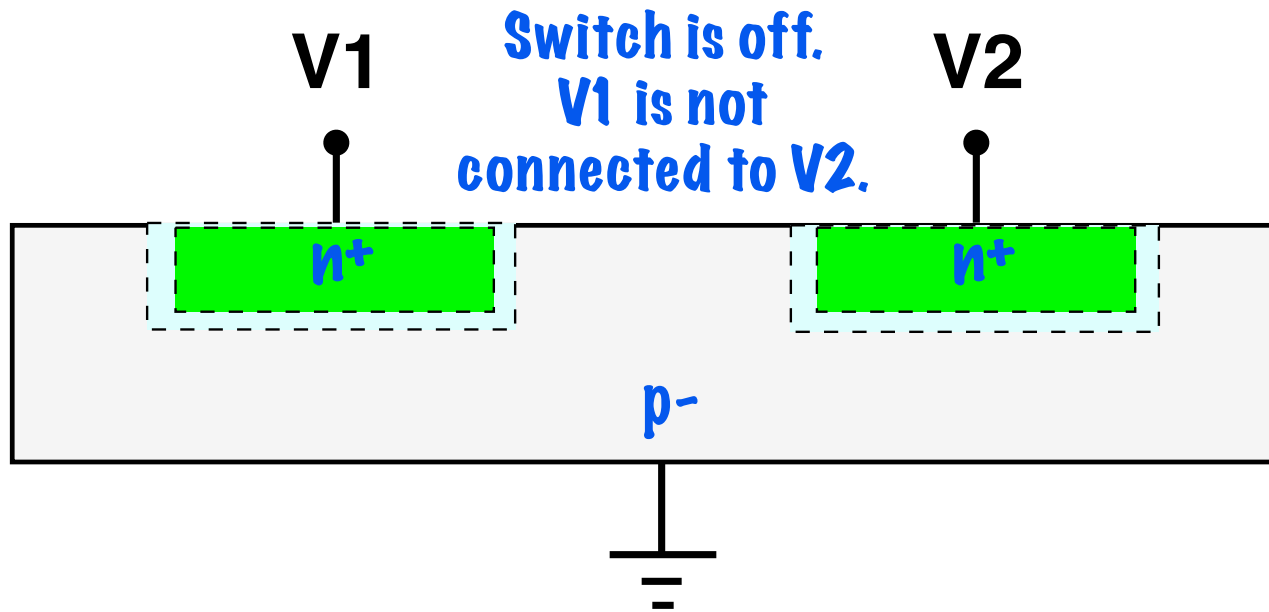
Anodes of all diodes on wafer connected to ground.

MOS Transistors

Two diodes and a capacitor in an interesting arrangement ...

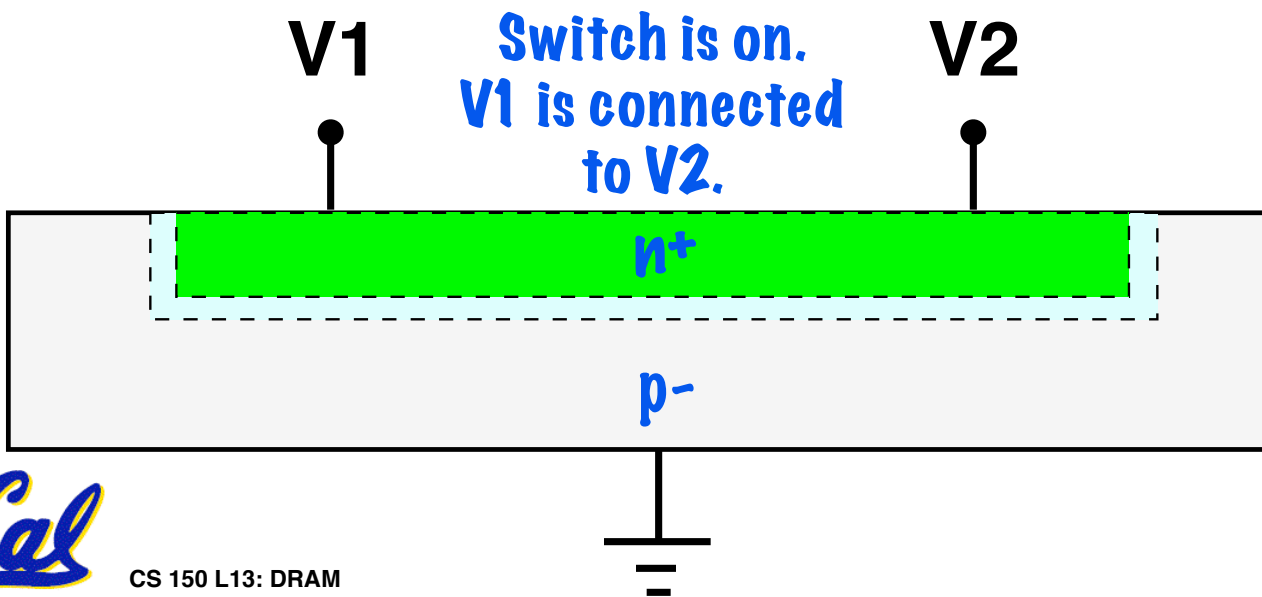
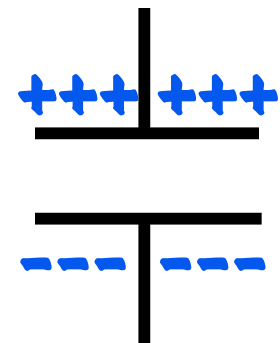


What we want: the perfect switch.

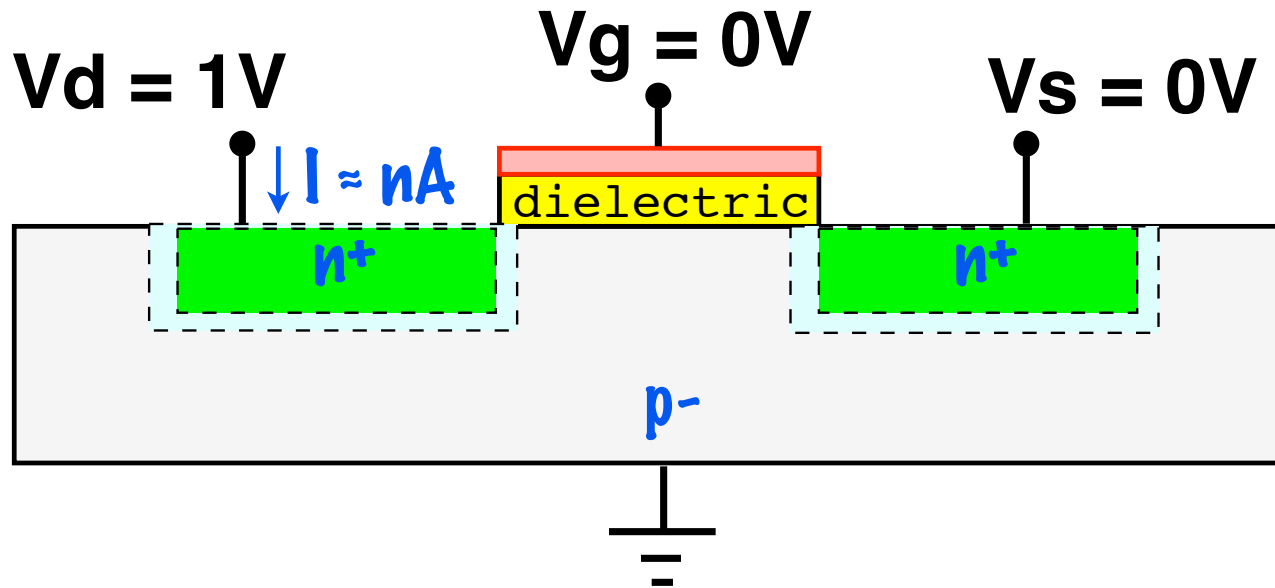


We want to turn a p-type region into an n-type region under voltage control.

We need electrons to fill valence holes and add conduction band electrons

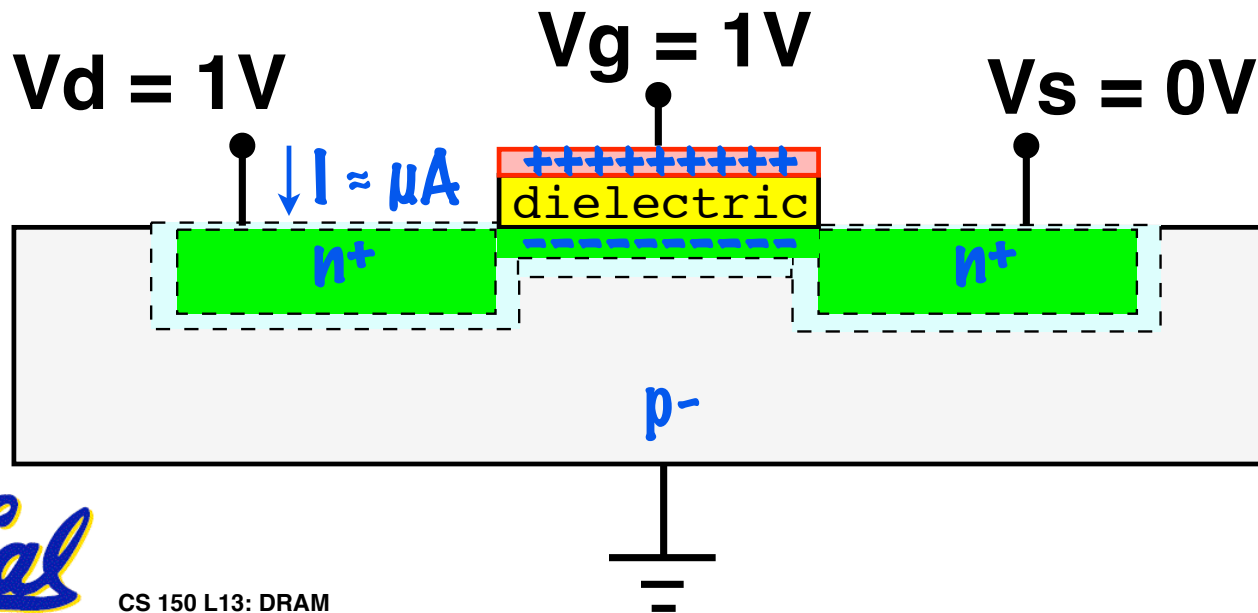


An n-channel MOS transistor (nFET)



Polysilicon gate, dielectric, and substrate form a capacitor.

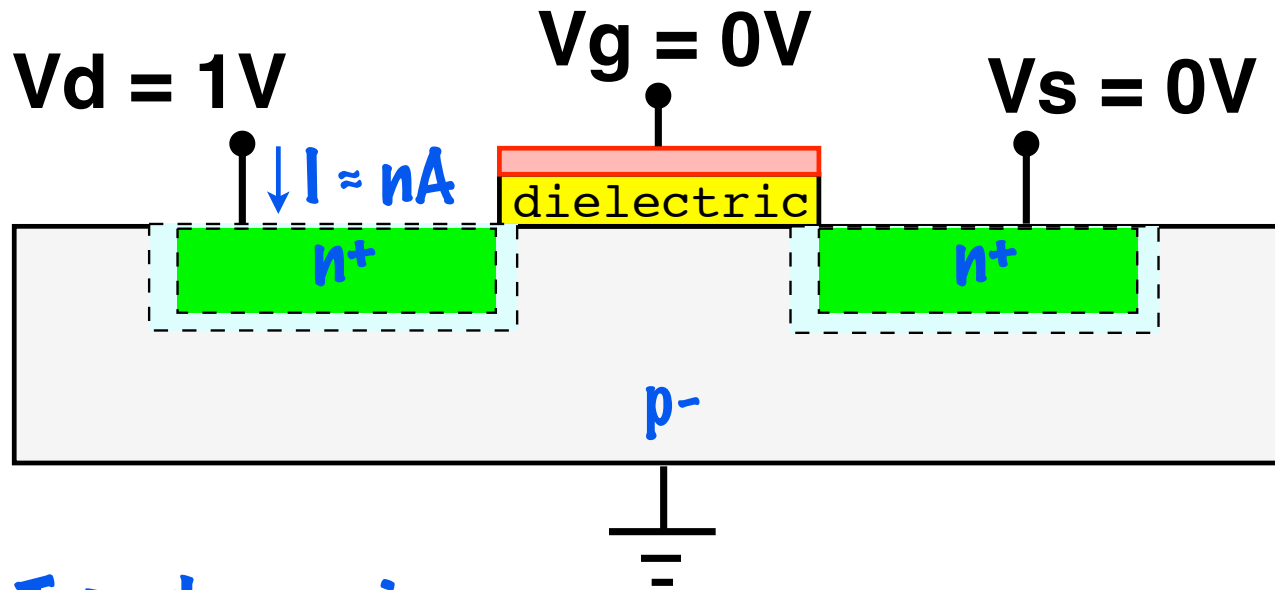
nFet is off
(I is "leakage")



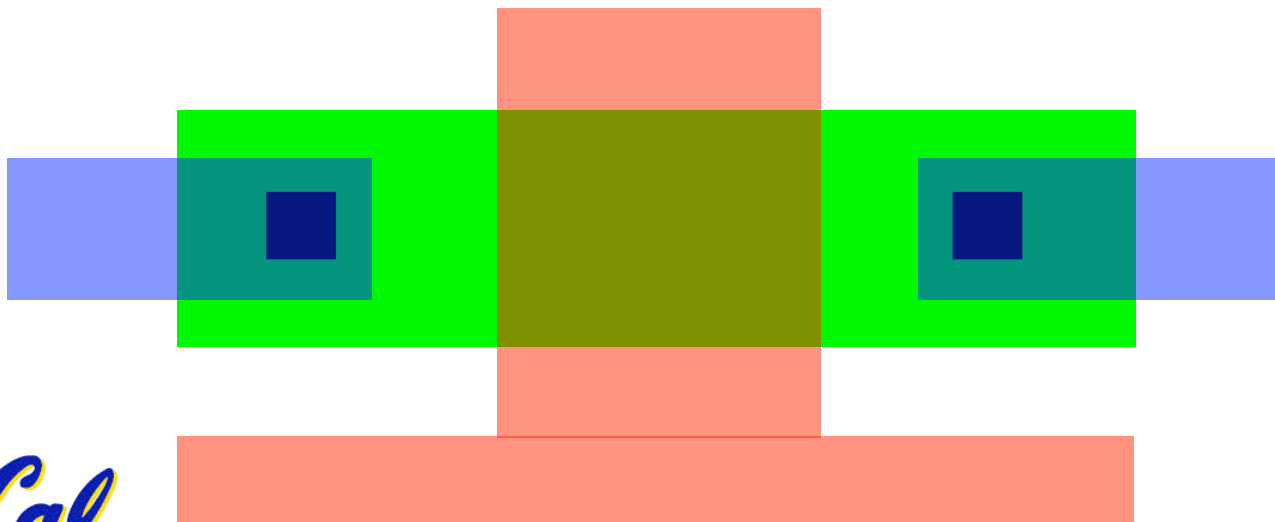
$V_g = 1V$, small region near the surface turns from p-type to n-type.

nFet is on.

Mask set for an n-Fet (circa 1986)



Top-down view:



Masks

- #1: n^+ diffusion
- #2: poly (gate)
- #3: diff contact
- #4: metal

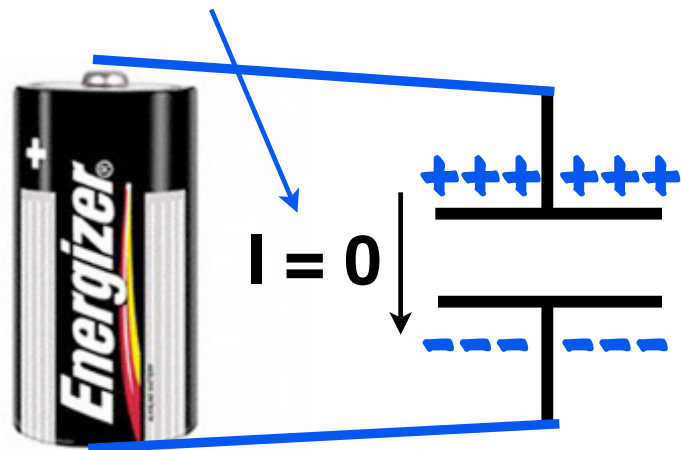
Layers to do
p-Fet not
shown. Modern
processes have
6 to 10 metal
layers (or more)
(in 1986: 2).

Dynamic Memory Cells



Recall: Capacitors in action

Because the dielectric is an insulator, and does not conduct.



After circuit “settles” ...

$$Q = C V = C * 1.5 \text{ Volts (D cell)}$$

Q: Charge stored on capacitor

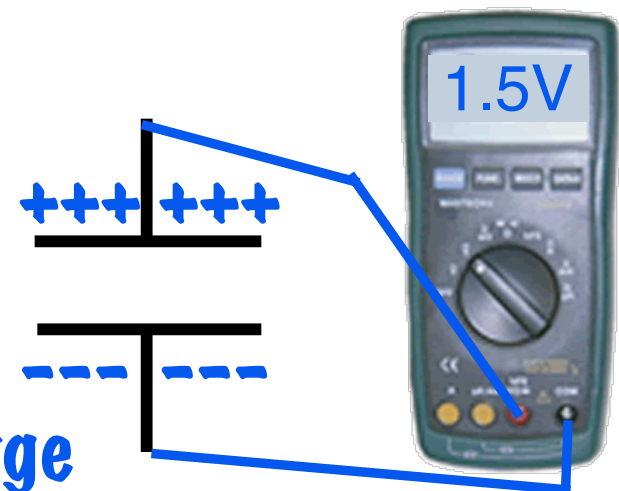
C: The capacitance of the device: function of device shape and type of dielectric.

After battery is removed:

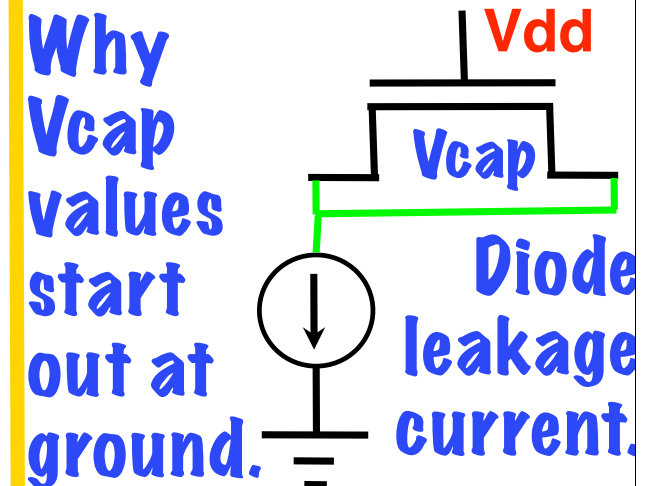
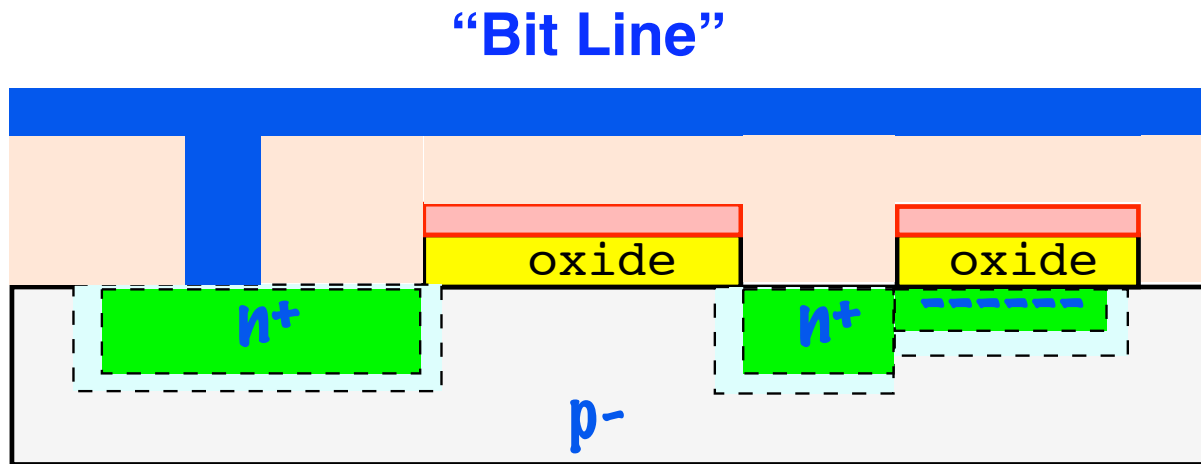
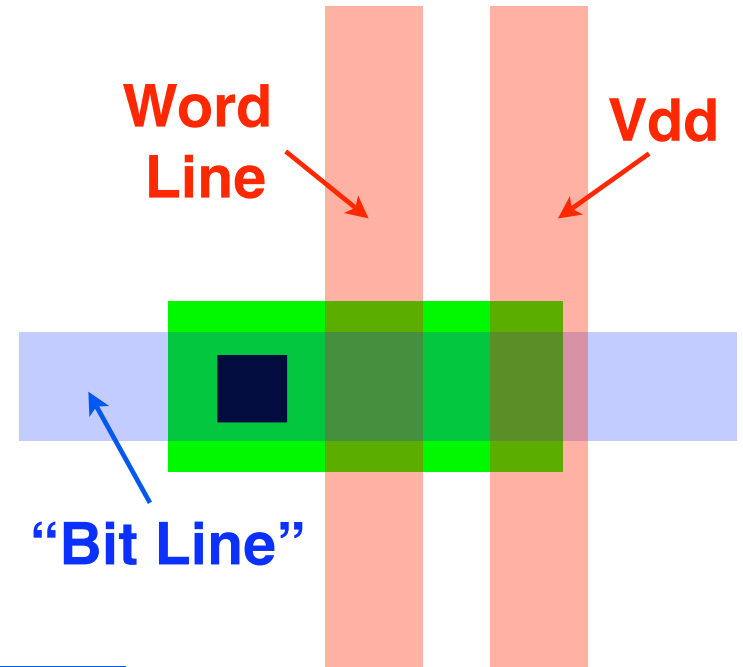
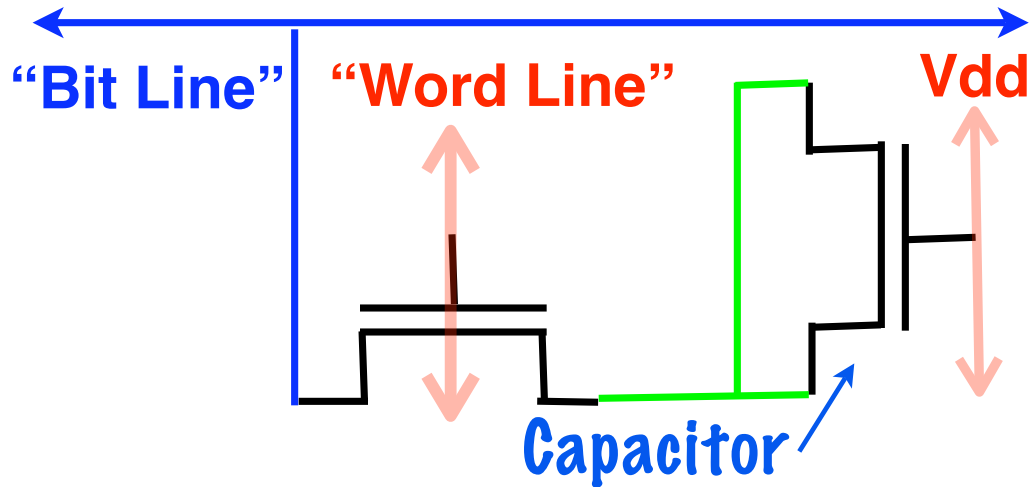
$$\text{Still, } Q = C * 1.5 \text{ Volts}$$



Capacitor “remembers” charge

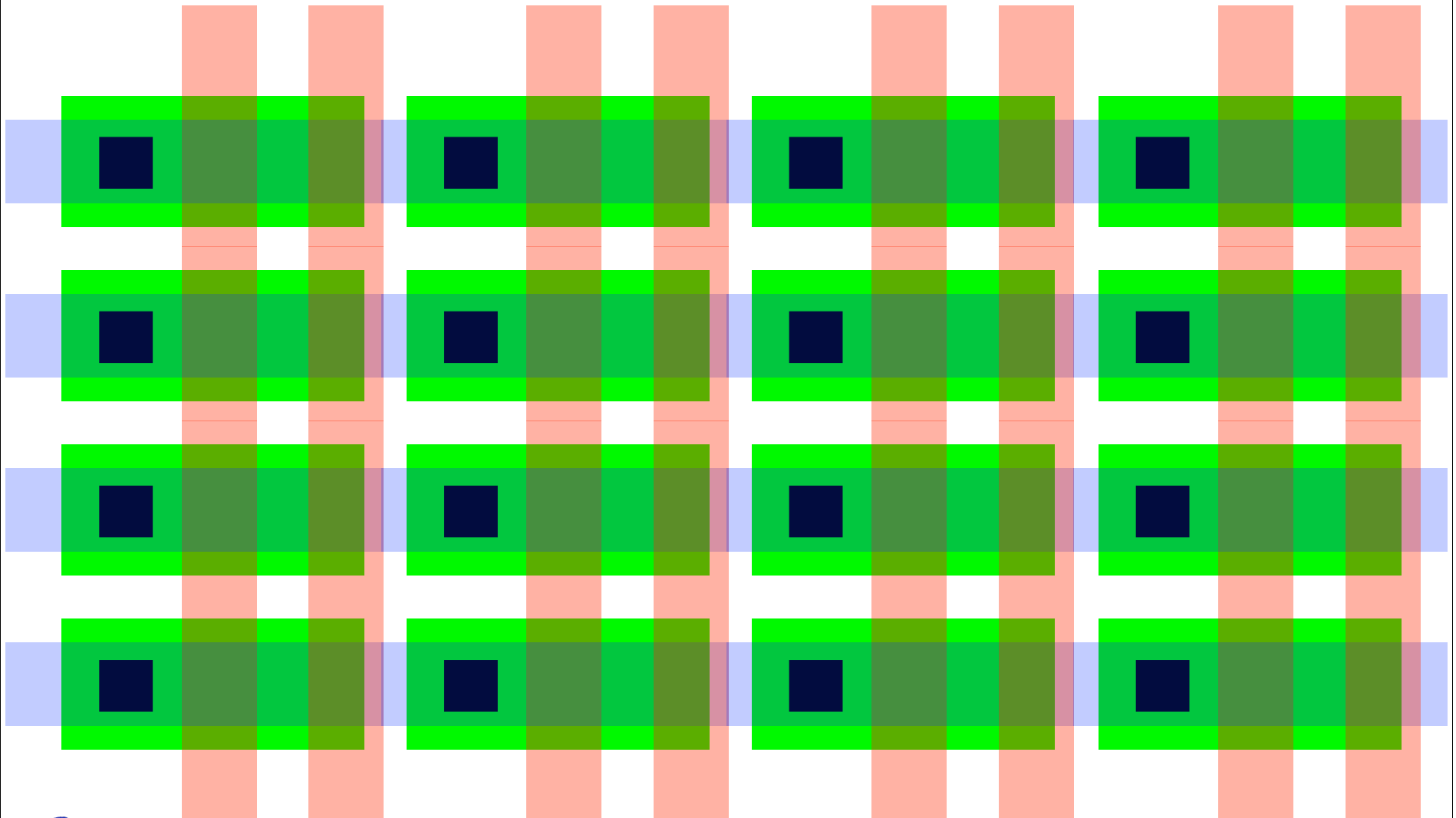


DRAM cell: 1 transistor, 1 capacitor



Word Line and Vdd run on "z-axis"

A 4 x 4 DRAM array (16 bits)



Invented after SRAM, by Robert Dennard

United States Patent Office

3,387,286

Patented June 4, 1968



1

3,387,286

FIELD-EFFECT TRANSISTOR MEMORY

Robert H. Dennard, Croton-on-Hudson, N.Y., assignor to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

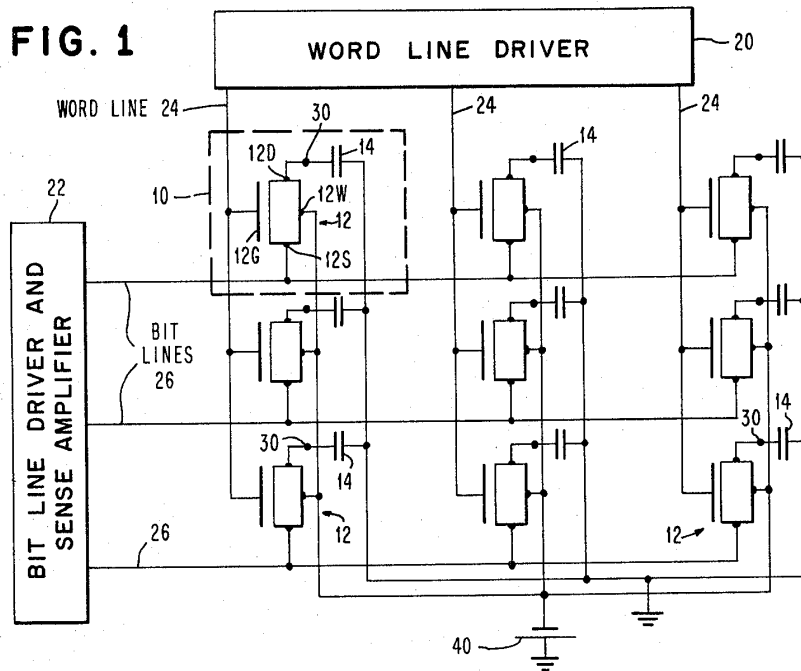
Filed July 14, 1967, Ser. No. 653,415

21 Claims. (Cl. 340-173)

2

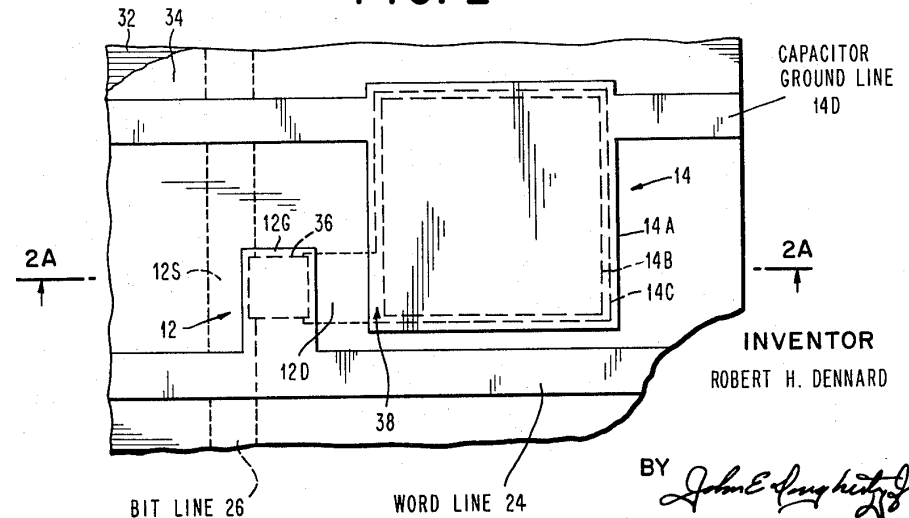
5
 tinent in disclosing various concepts and structures which have been developed in the application of field-effect transistors to different types of memory applications, the primary thrust up to this time in conventional read-write random access memories has been to connect a plurality of field-effect transistors in each cell in a latch configuration. Memories of this type require a large number of active devices in each cell and therefore each cell re-

FIG. 1



CS 150 L13: DRAM

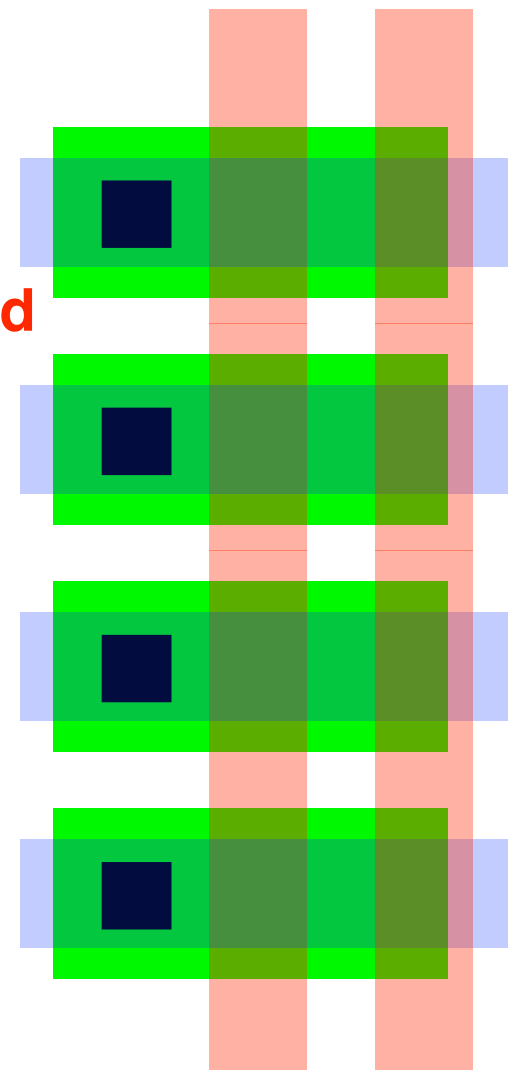
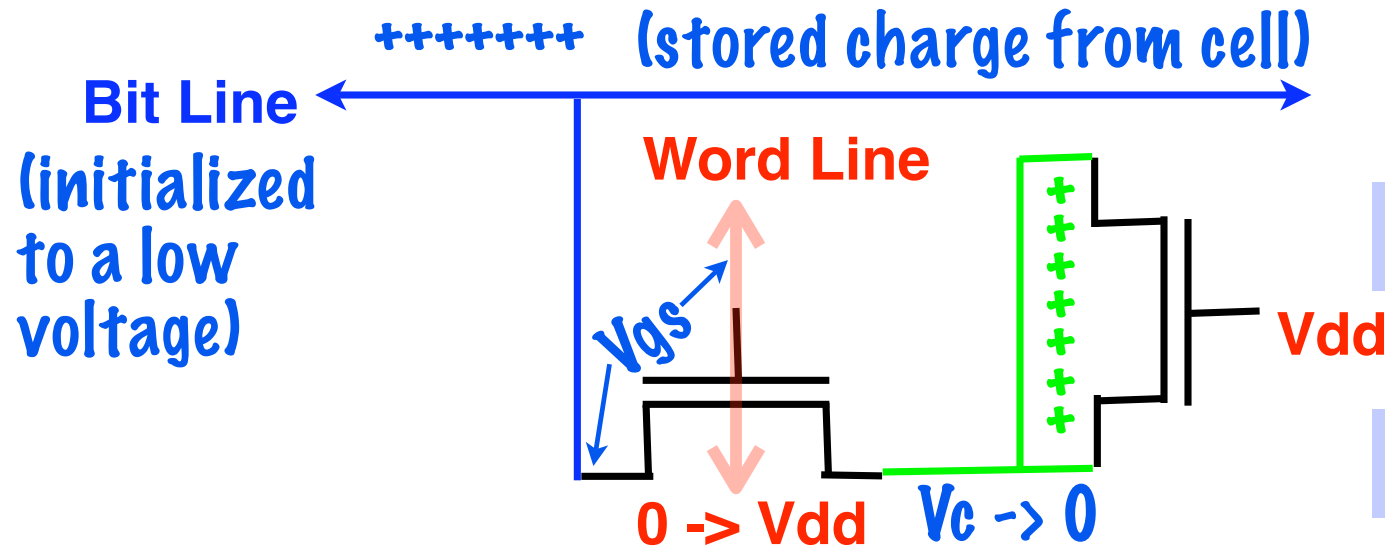
FIG. 2



INVENTOR
 ROBERT H. DENNARD

BY *John E. Long*
 ATTORNEY

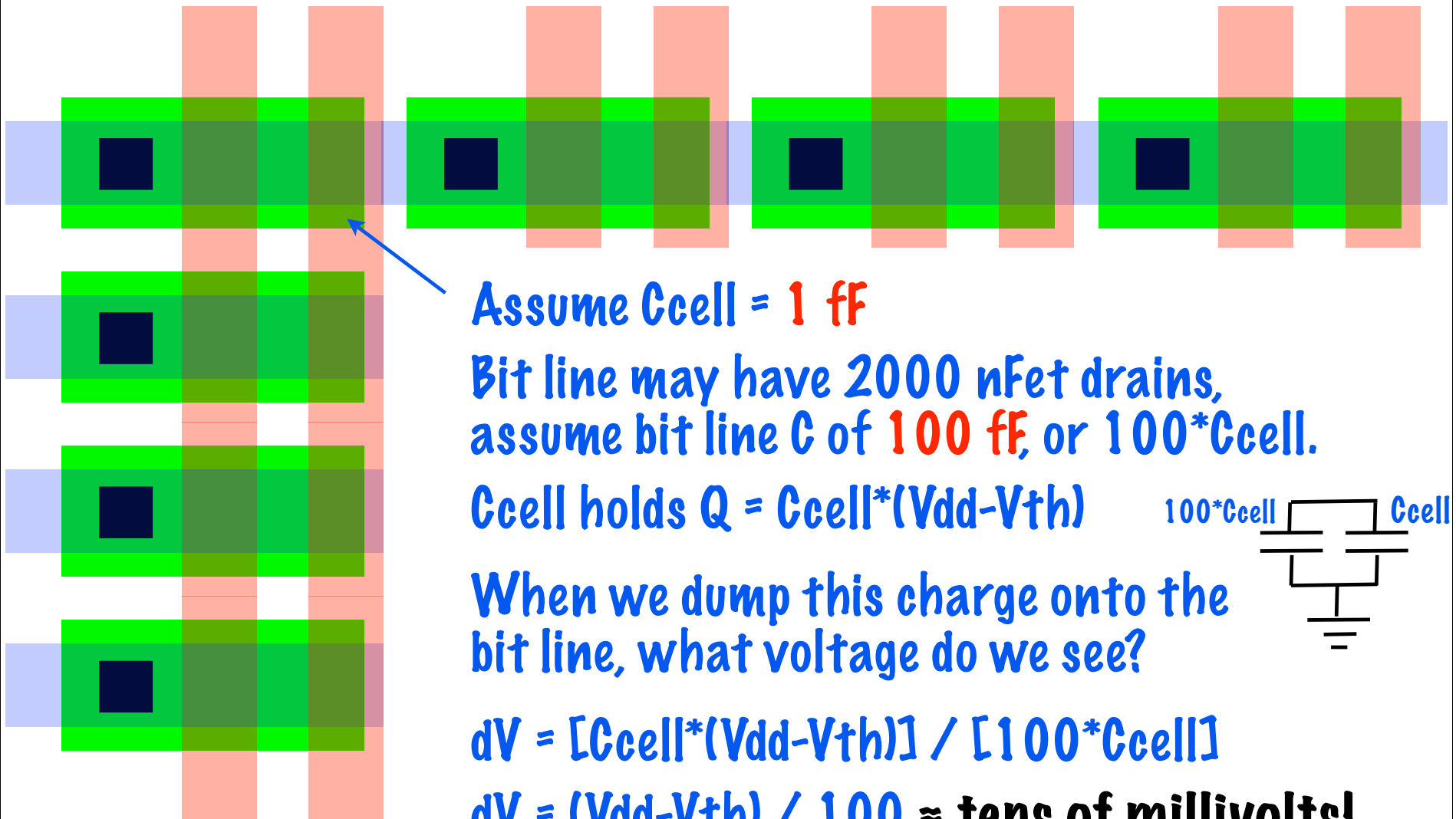
DRAM Challenge #2: Destructive Reads



Raising the word line removes the charge from every cell it connects to!

Must write back after each read.

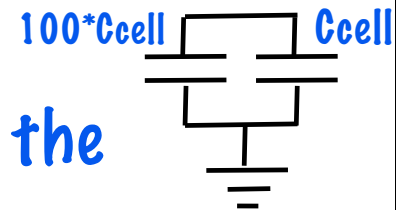
DRAM Circuit Challenge #3a: Sensing



Assume $C_{cell} = 1 \text{ fF}$

Bit line may have 2000 nFet drains,
assume bit line C of 100 fF , or $100 * C_{cell}$.

Ccell holds $Q = C_{cell} * (V_{dd} - V_{th})$



When we dump this charge onto the
bit line, what voltage do we see?

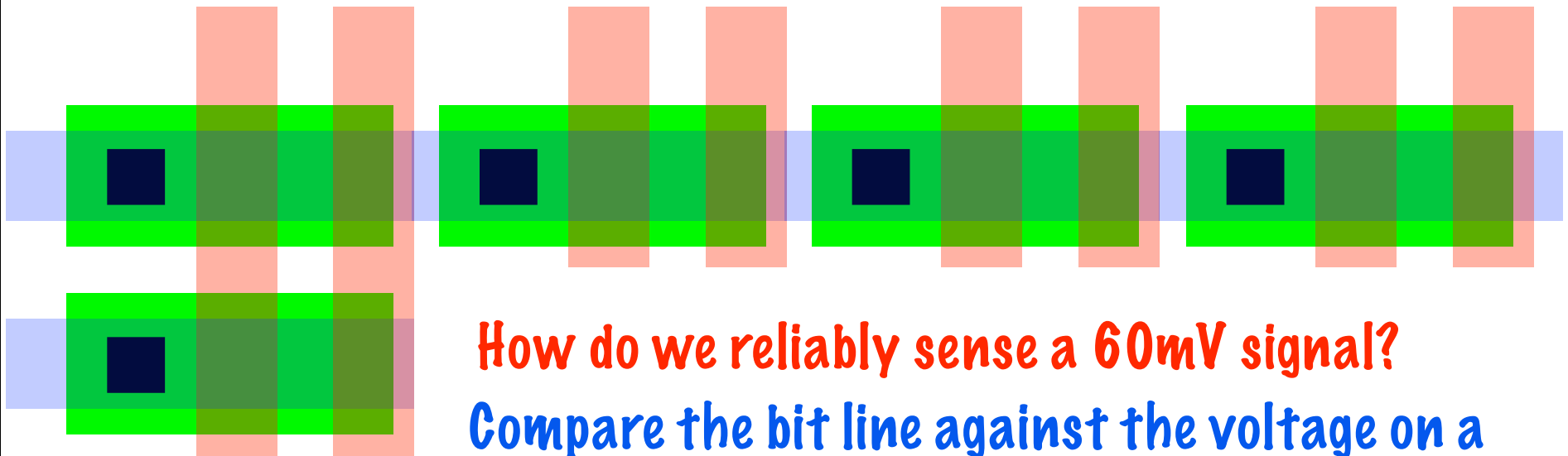
$$dV = [C_{cell} * (V_{dd} - V_{th})] / [100 * C_{cell}]$$

$$dV = (V_{dd} - V_{th}) / 100 \approx \text{tens of millivolts!}$$



In practice, scale array to get a 60mV signal.

DRAM Circuit Challenge #3b: Sensing



[...]

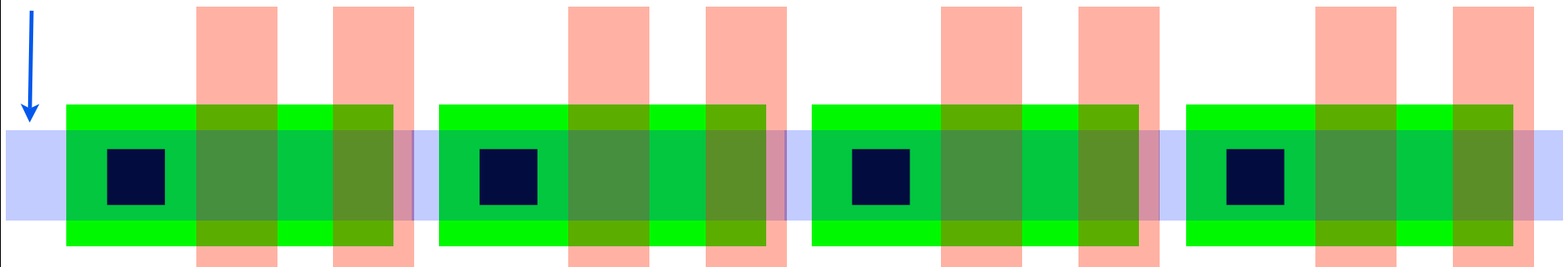
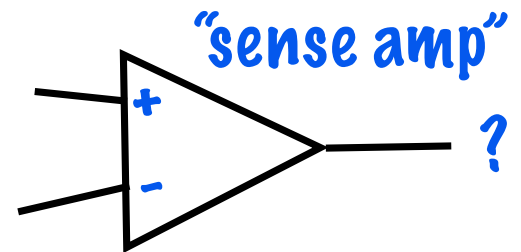
How do we reliably sense a 60mV signal?

Compare the bit line against the voltage on a "dummy" bit line.

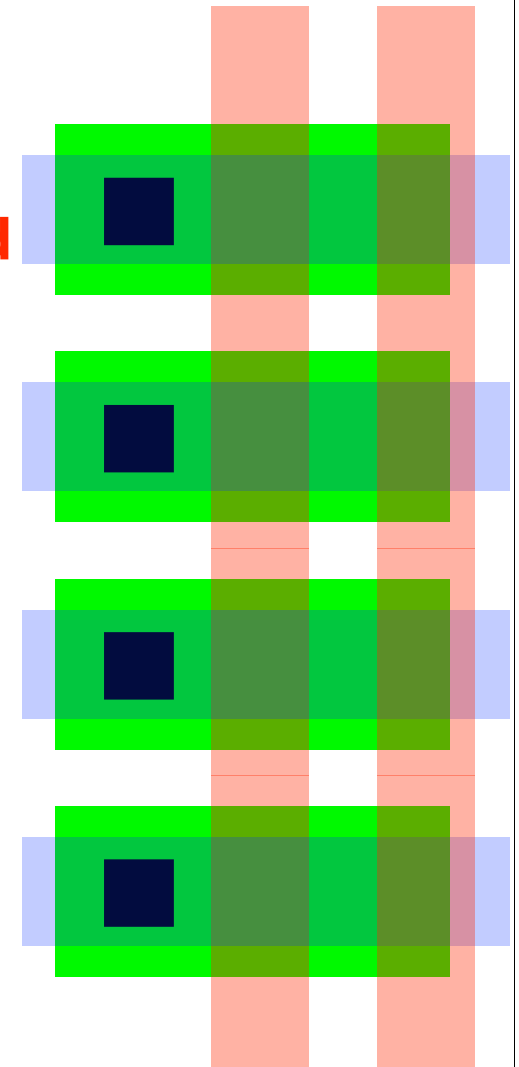
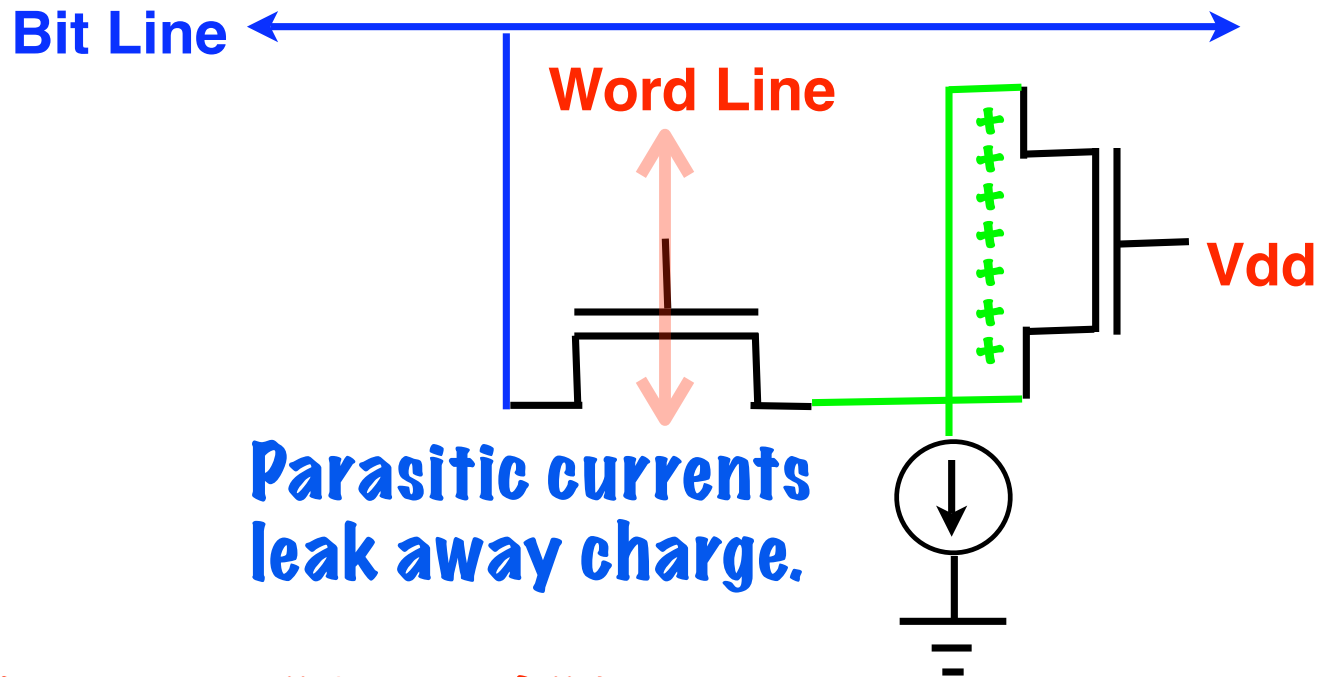
"Dummy" bit line.
Cells hold no charge.

Bit line to sense

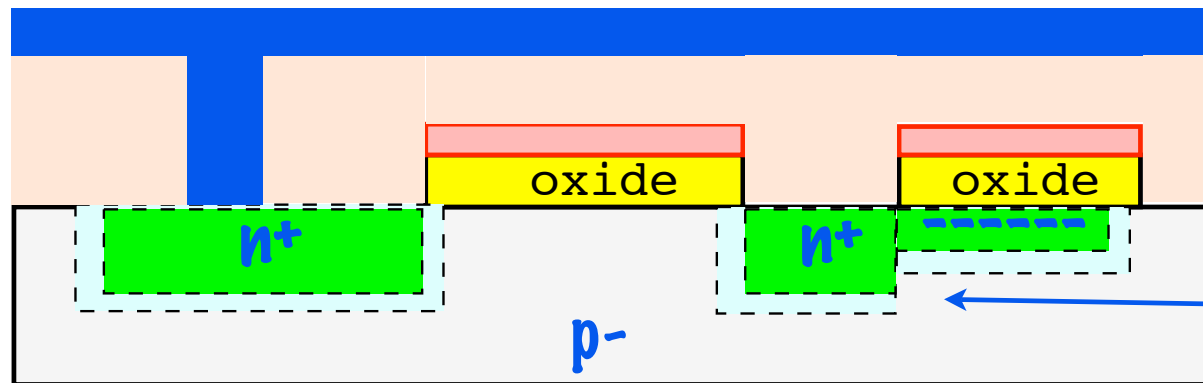
Dummy bit line



DRAM Challenge #4: Leakage ...

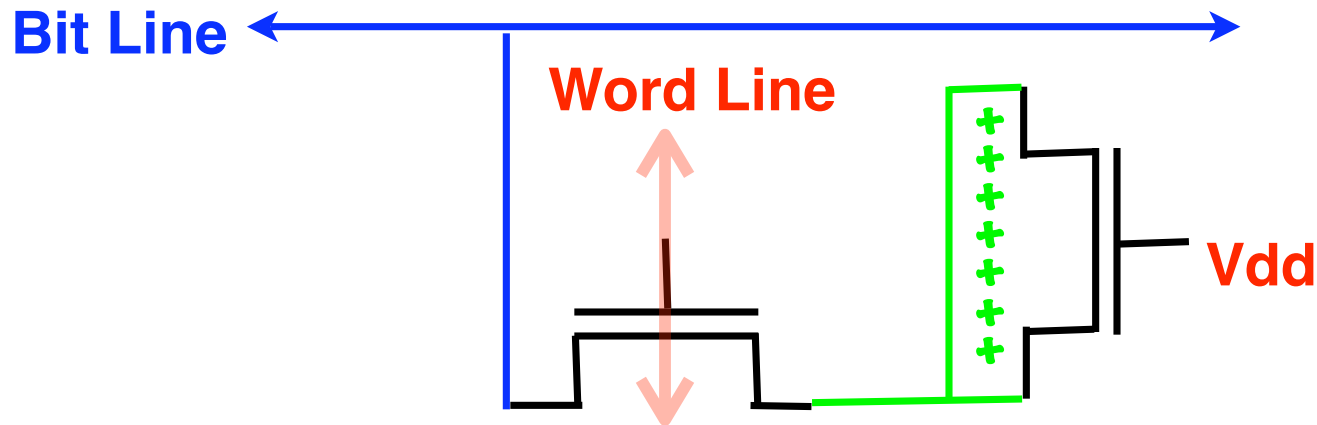


Solution: "Refresh", by rewriting cells at regular intervals (tens of milliseconds)



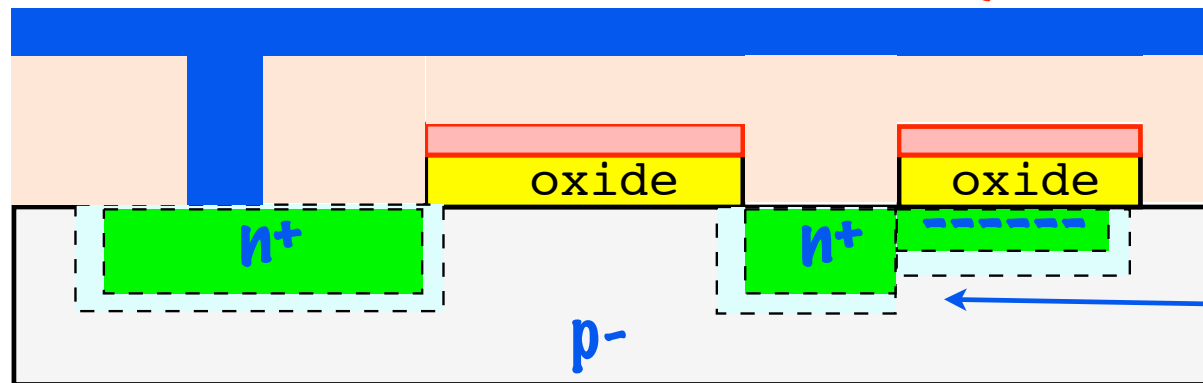
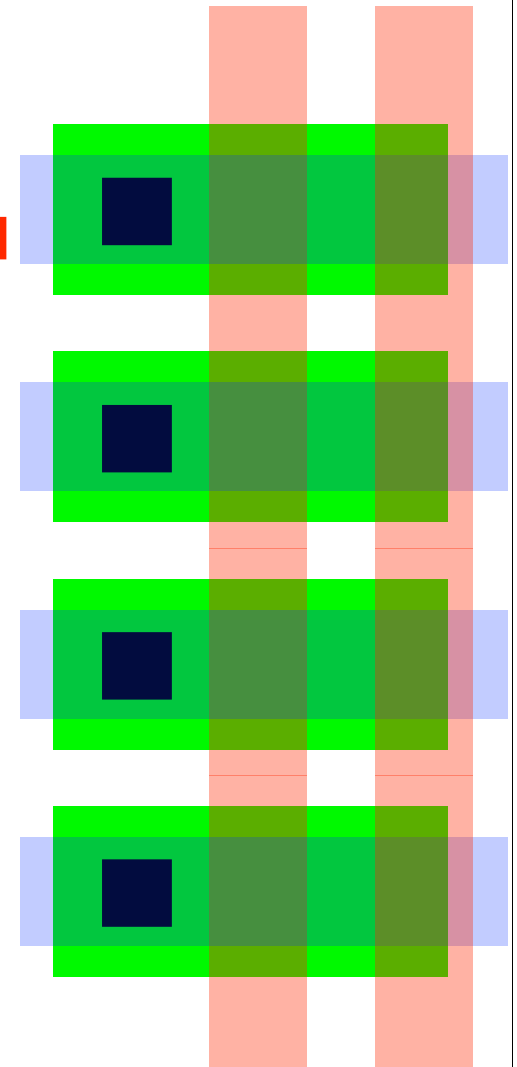
Diode leakage ...

DRAM Challenge #5: Cosmic Rays ...



Cell capacitor holds **25,000** electrons (or less). Cosmic rays that constantly bombard us can release the charge!

Solution: Store extra bits to detect and correct random bit flips (ECC).



DRAM Challenge 6: Yield

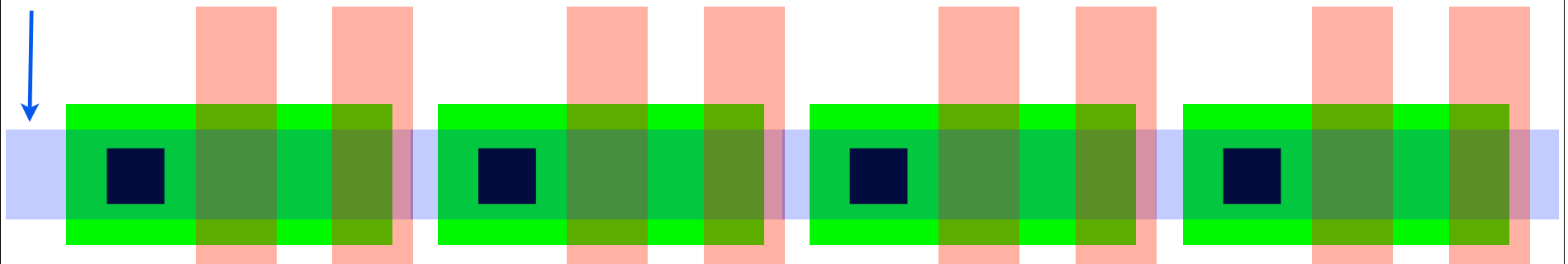


[...]

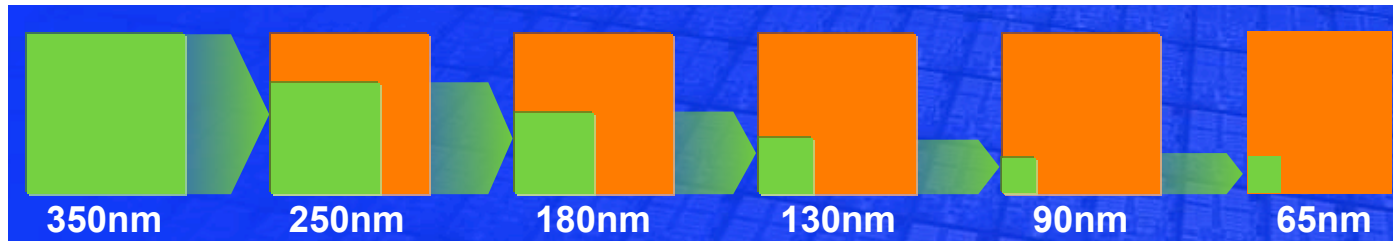
If one bit is bad, do we throw chip away?

Solution: add extra bit lines (i.e. 80 when you only need 64). During testing, find the bad bit lines, and use high current to burn away "fuses" put on chip to remove them.

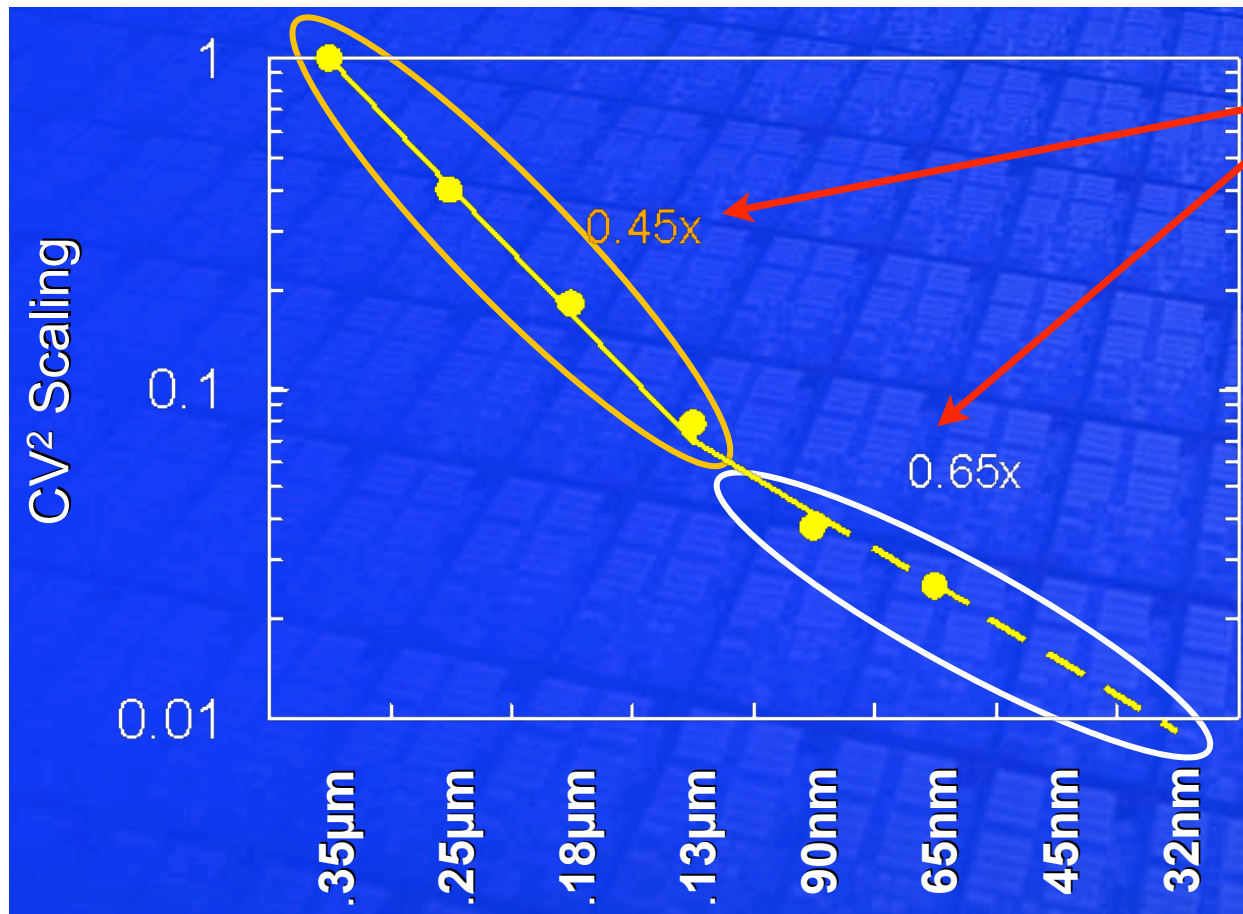
Extra bit lines.
Used for "sparing".



Recall: Process Scaling



Recall process scaling ("Moore's Law")

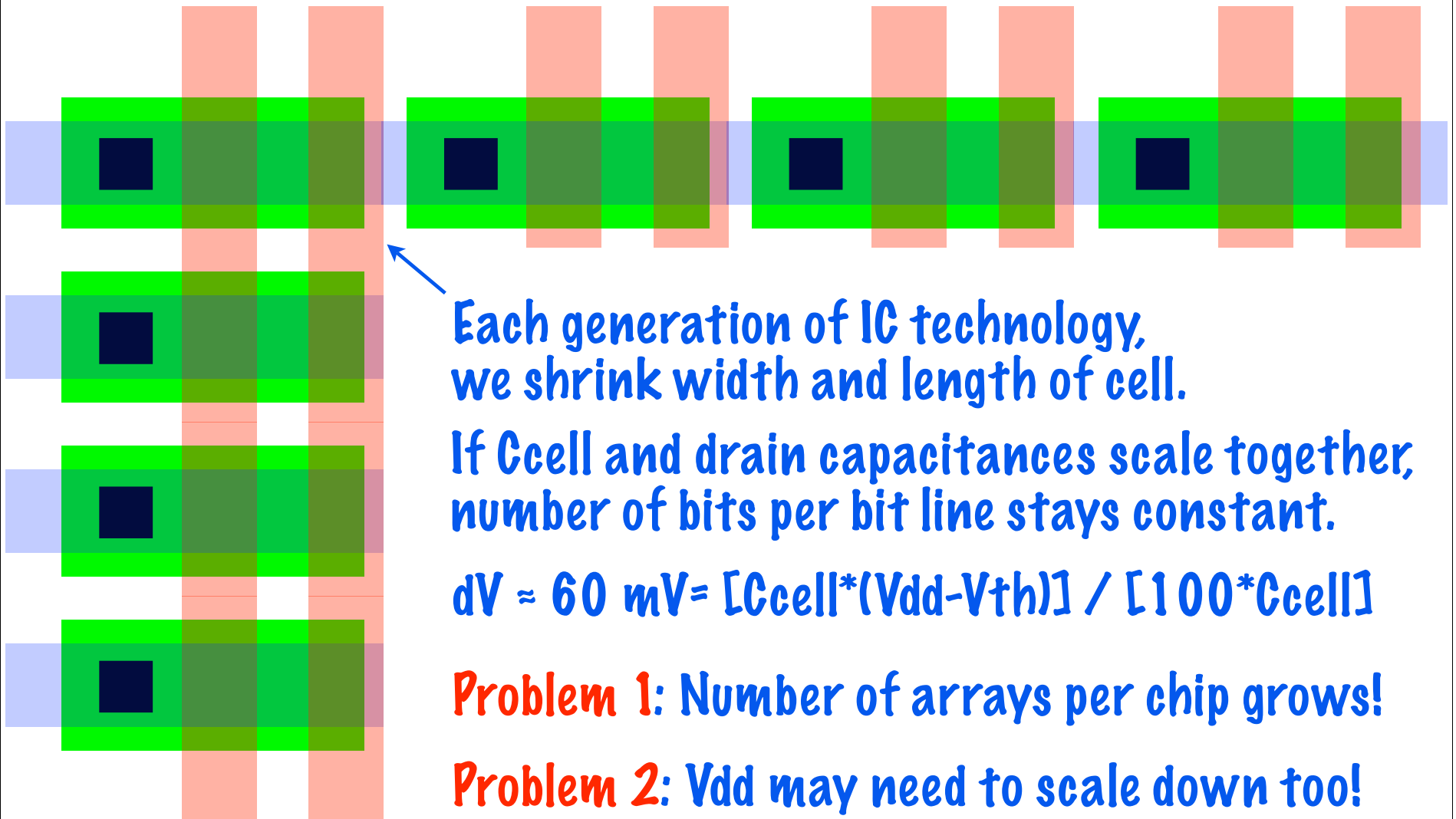


Due to reducing V and C (length and width of C s decrease, but plate distance gets smaller).

Recent slope more shallow because V is being scaled less aggressively.

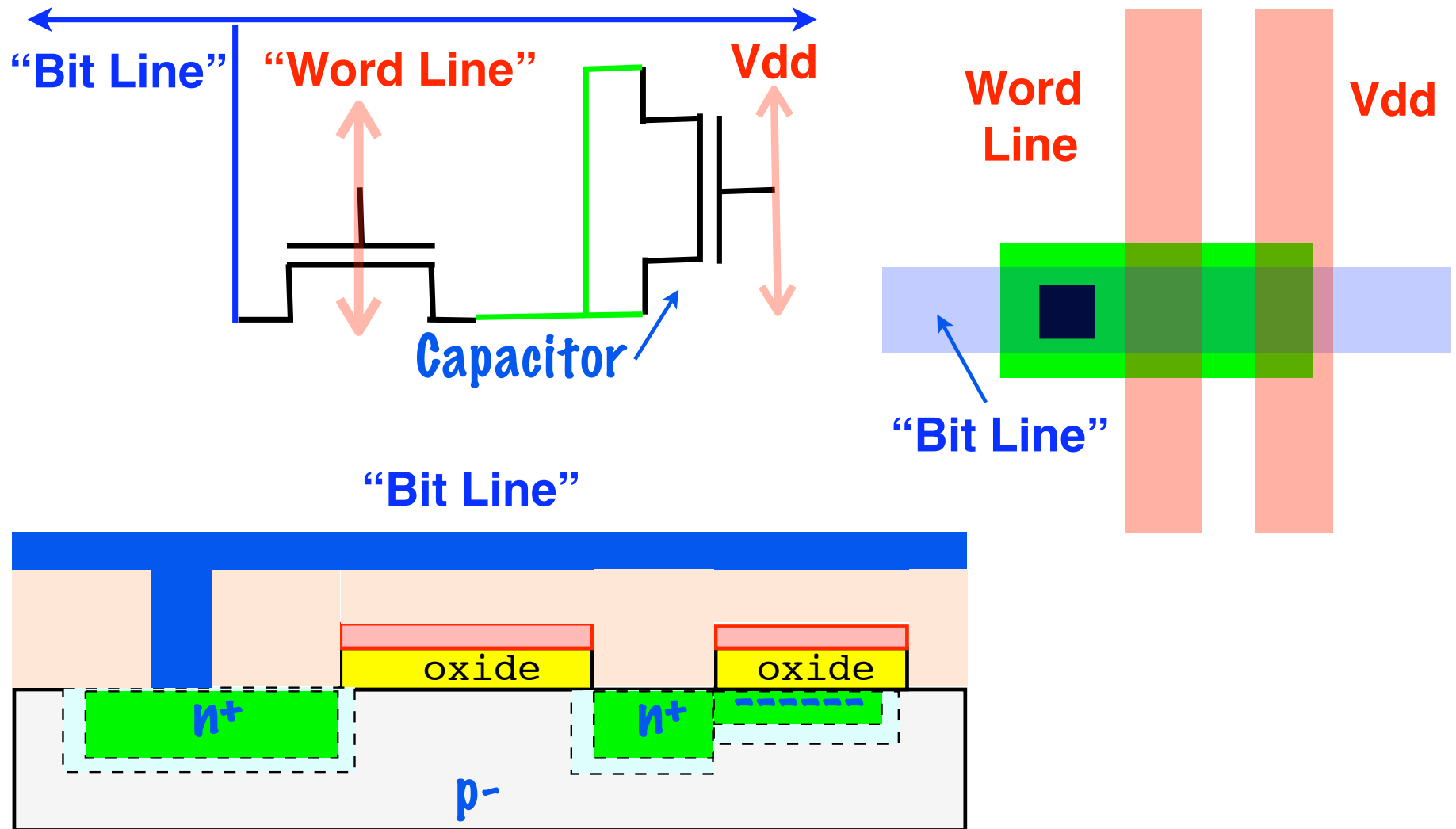
From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.

DRAM Challenge 7: Scaling



Solution: Constant Innovation of Cell Capacitors!

Poly-diffusion Ccell is ancient history



Word Line and Vdd run on "z-axis"

Early replacement: “Trench” capacitors

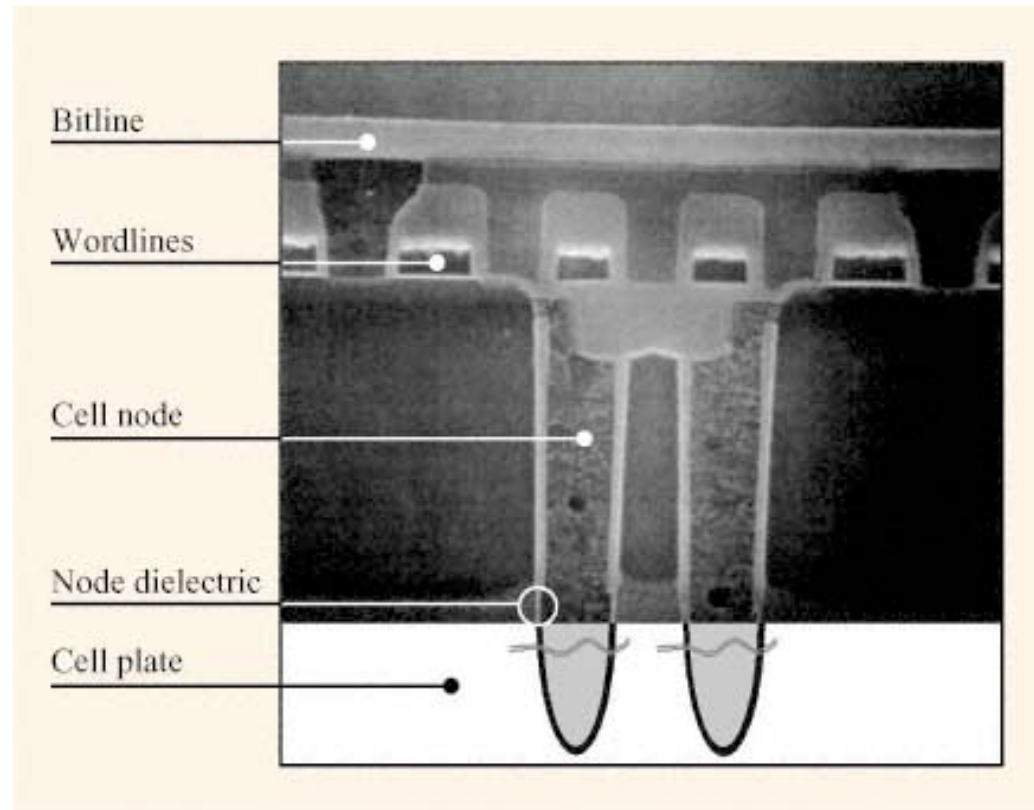
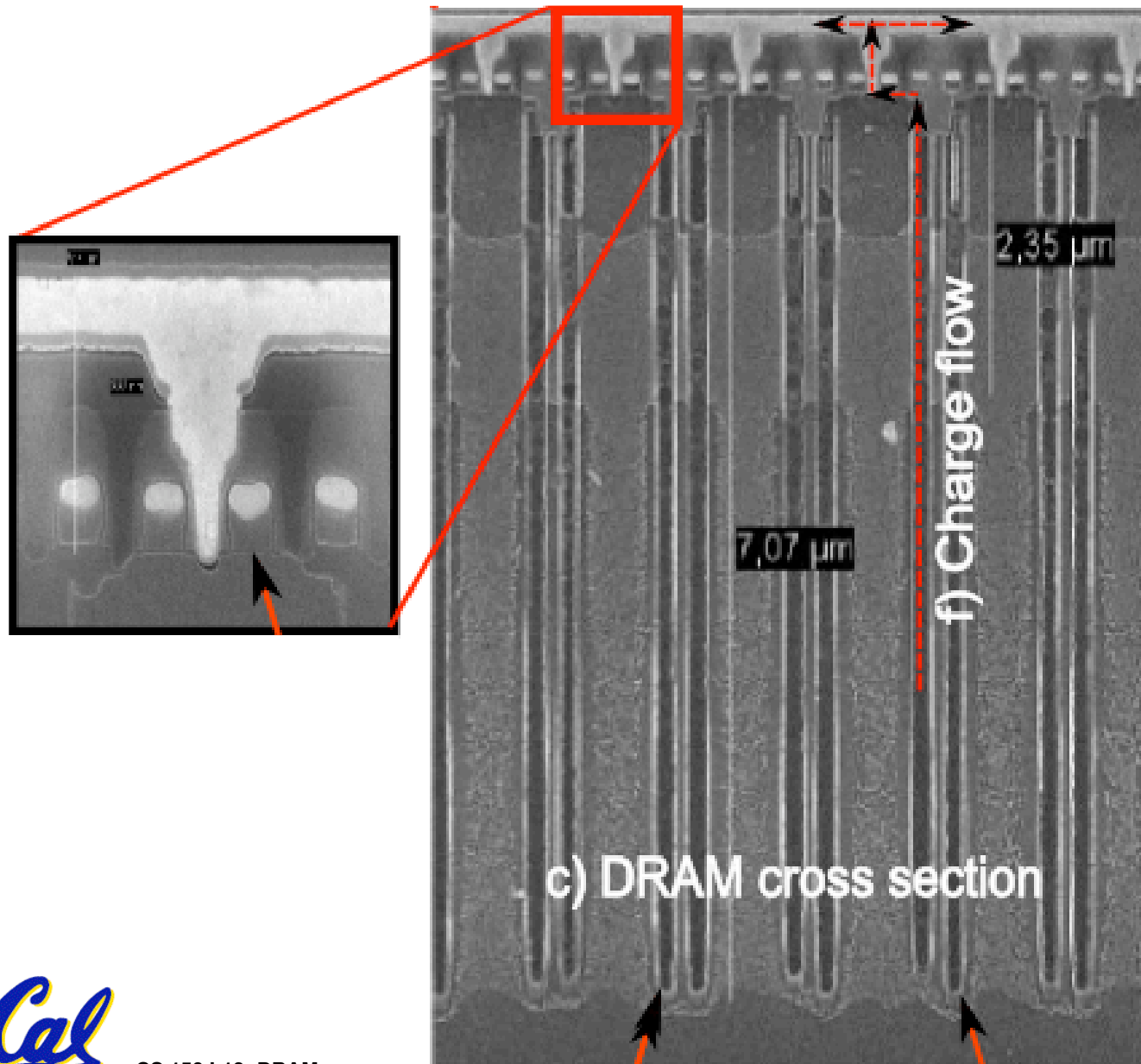


Figure 4

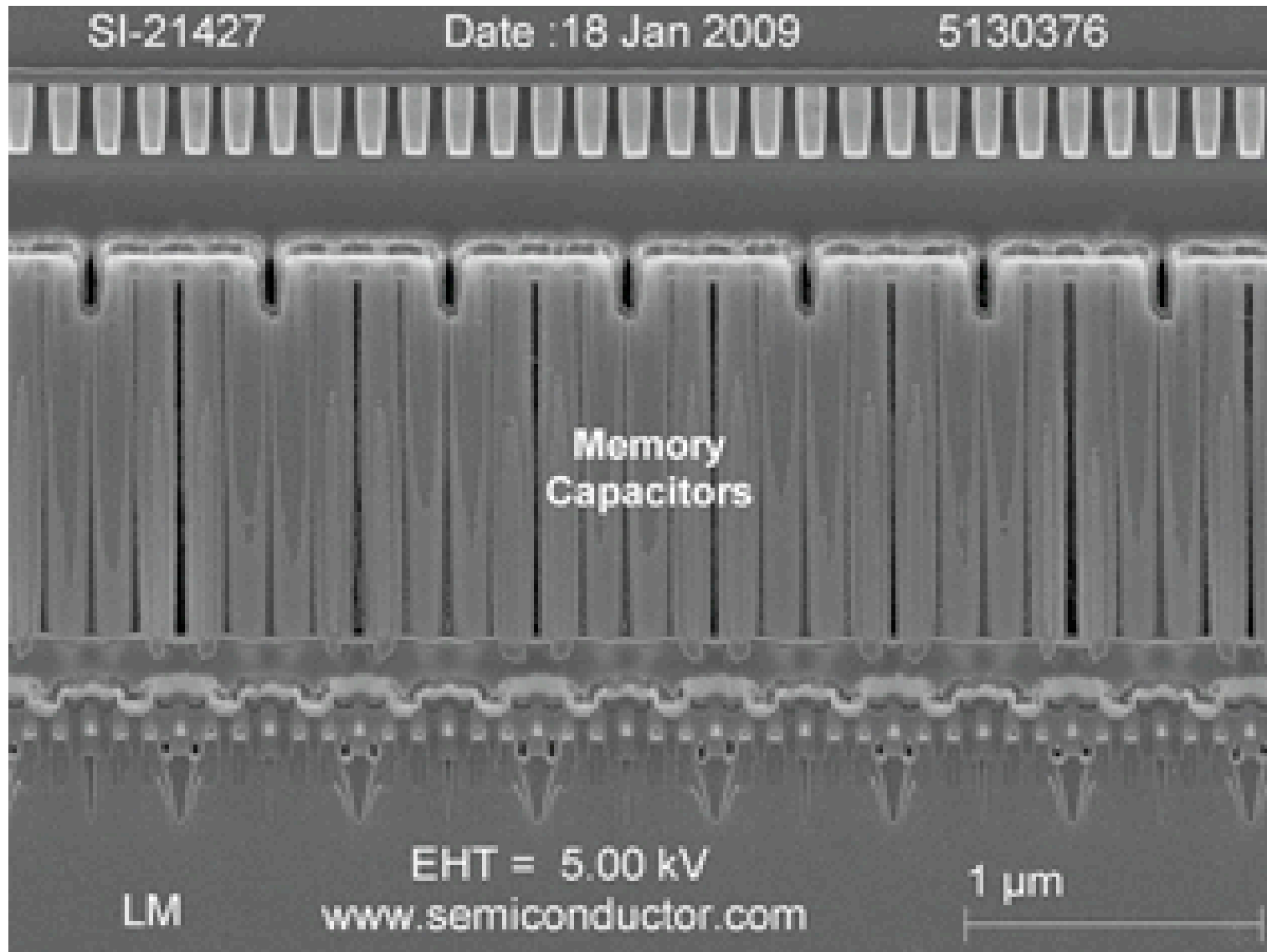
SEM photomicrograph of 0.25- μm trench DRAM cell suitable for scaling to 0.15 μm and below. Reprinted with permission from [17]; © 1995 IEEE.

Final generation of trench capacitors

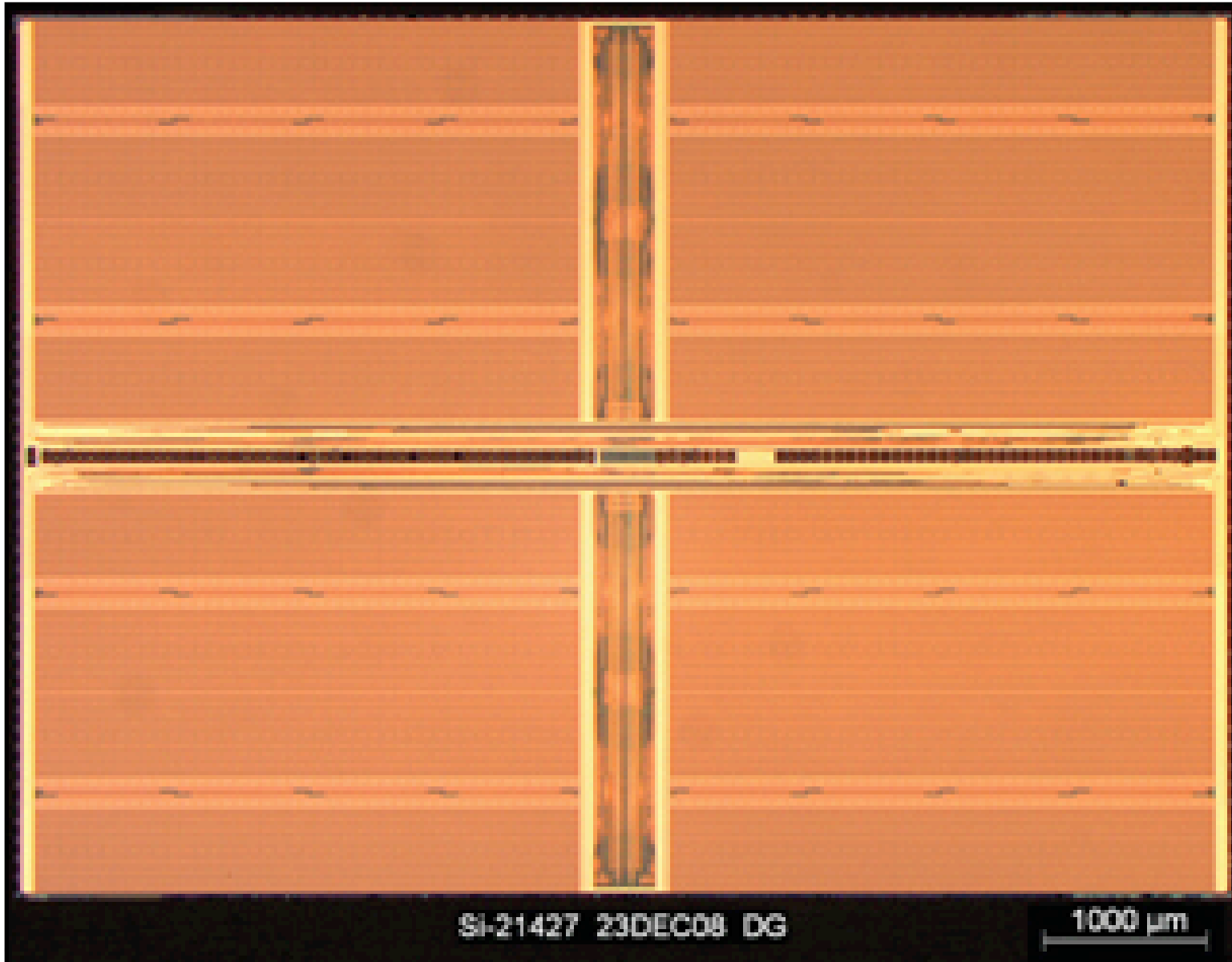


The companies that kept scaling trench capacitors for commodity DRAM chips went out of business.

Modern cells: “stacked” capacitors



Micron 50nm 1-Gbit DDR2 die photo

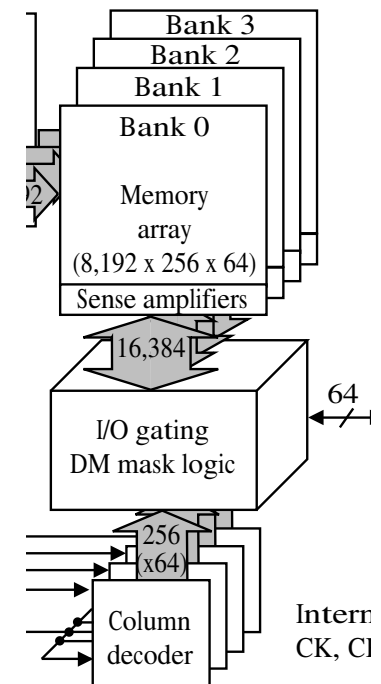


Today's Lecture: DRAM

* DRAM, Xilinx, and You

* DRAM: Bottom-up

* DRAM: Top-down



Memory Arrays



512Mb: x4, x8, x16 DDR2 SDRAM
Features



“Word Line”
“Row”

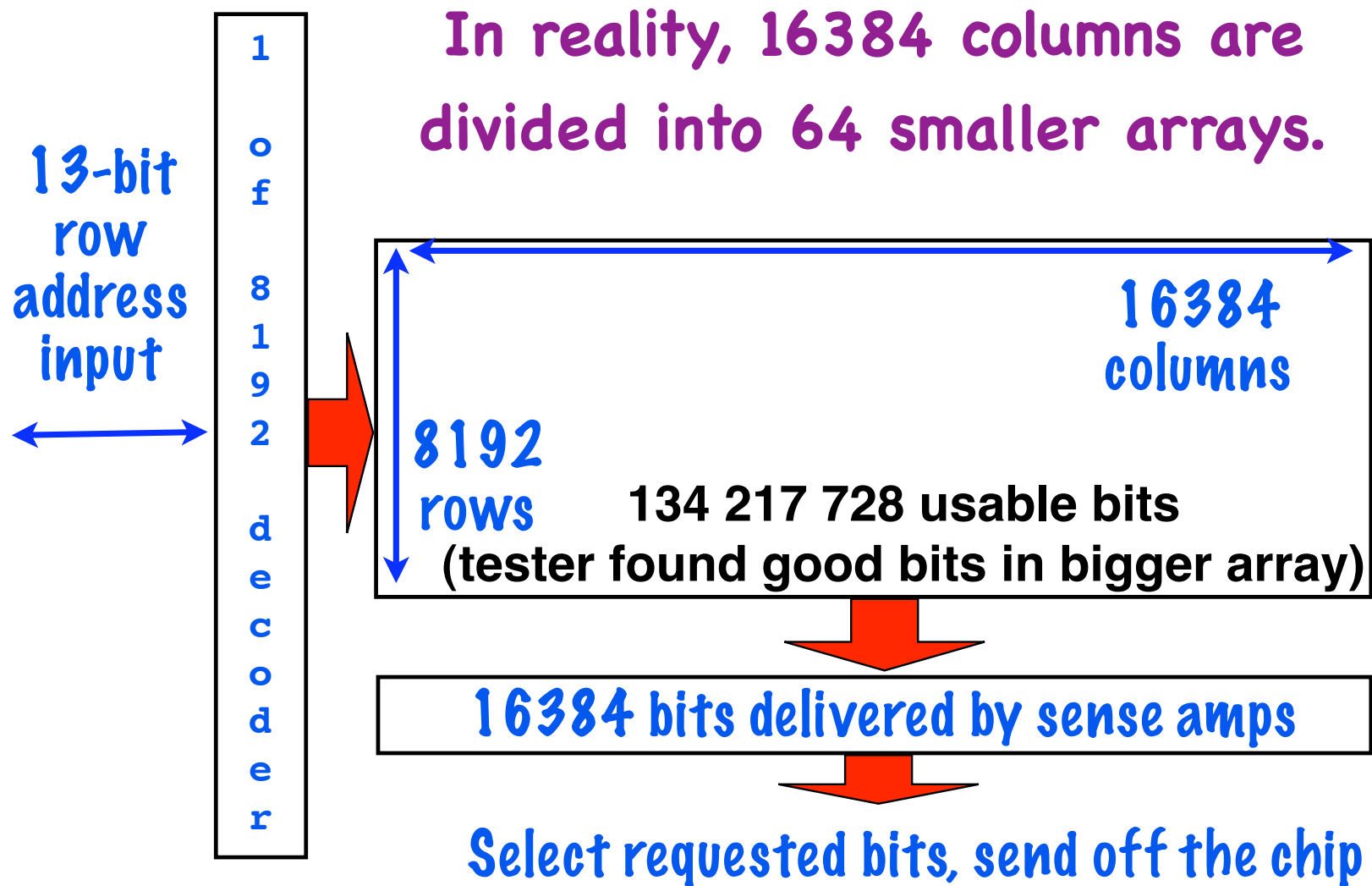
Bit Line
“Column”

People
buy
DRAM for
the bits.
“Edge”
circuits
are
overhead.

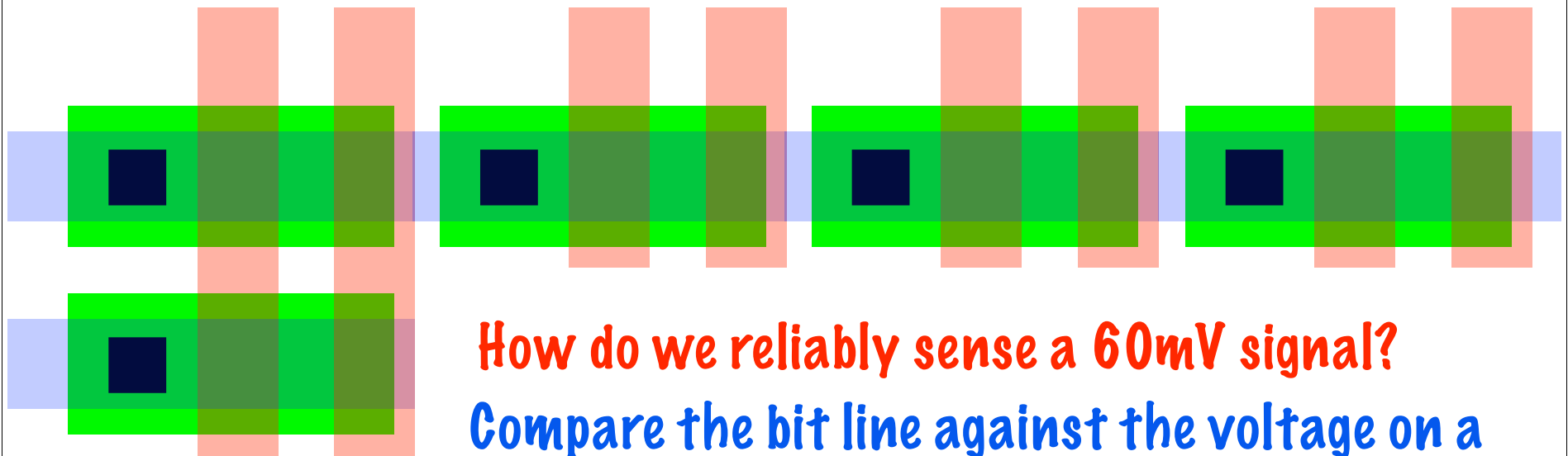
So, we
amortize
the edge
circuits
over big
arrays.



A “bank” of 128 Mb (512Mb chip -> 4 banks)



Recall DRAM Challenge #3b: Sensing



[...]

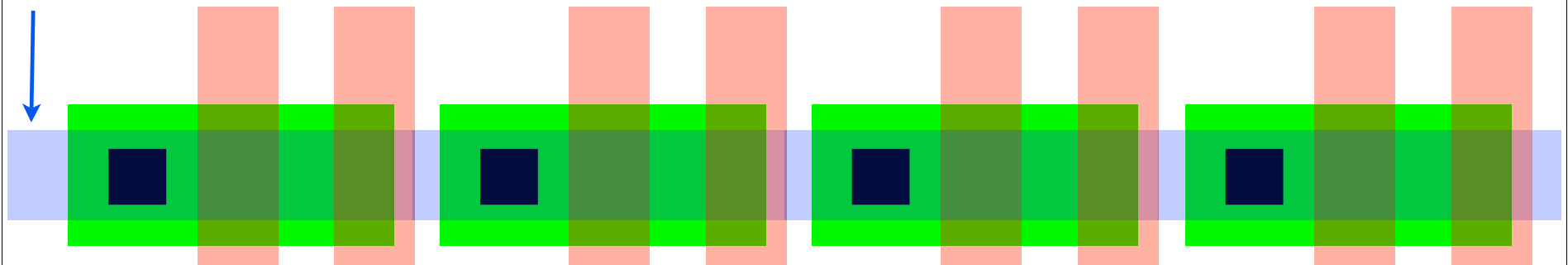
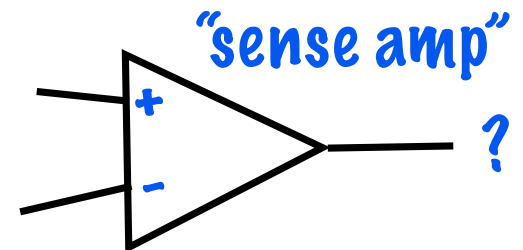
How do we reliably sense a 60mV signal?

Compare the bit line against the voltage on a "dummy" bit line.

"Dummy" bit line.
Cells hold no charge.

Bit line to sense

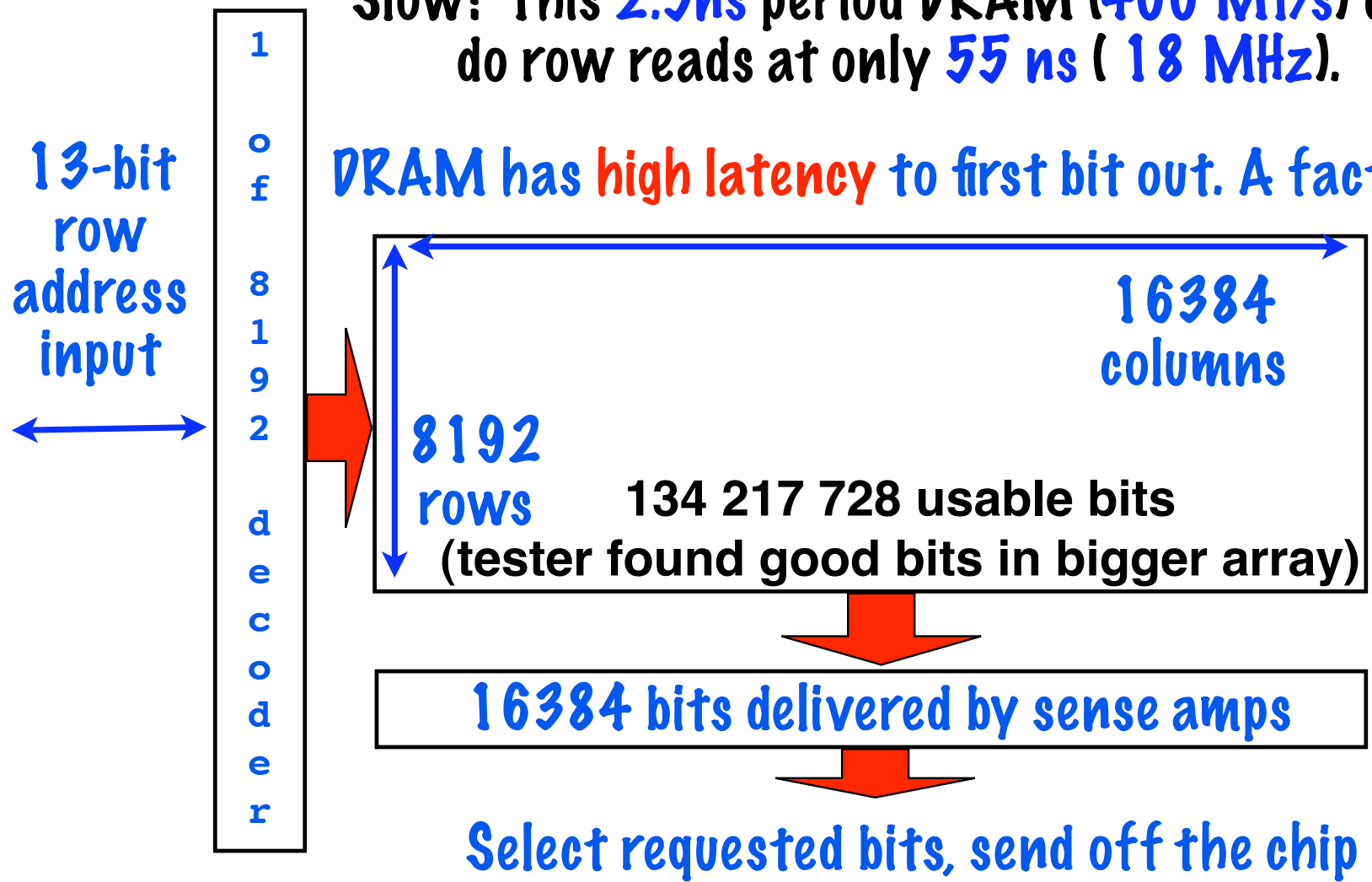
Dummy bit line



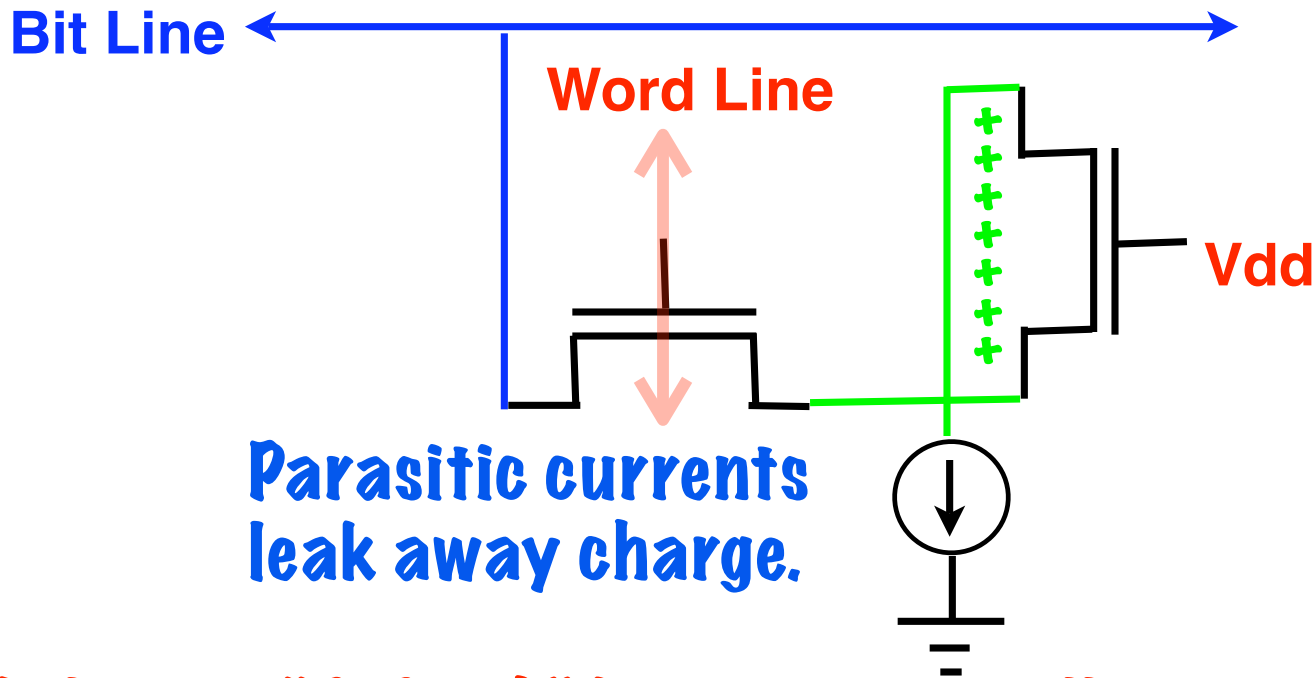
“Sensing” is row read into sense amps

Slow! This 2.5ns period DRAM (400 MT/s) can do row reads at only 55 ns (18 MHz).

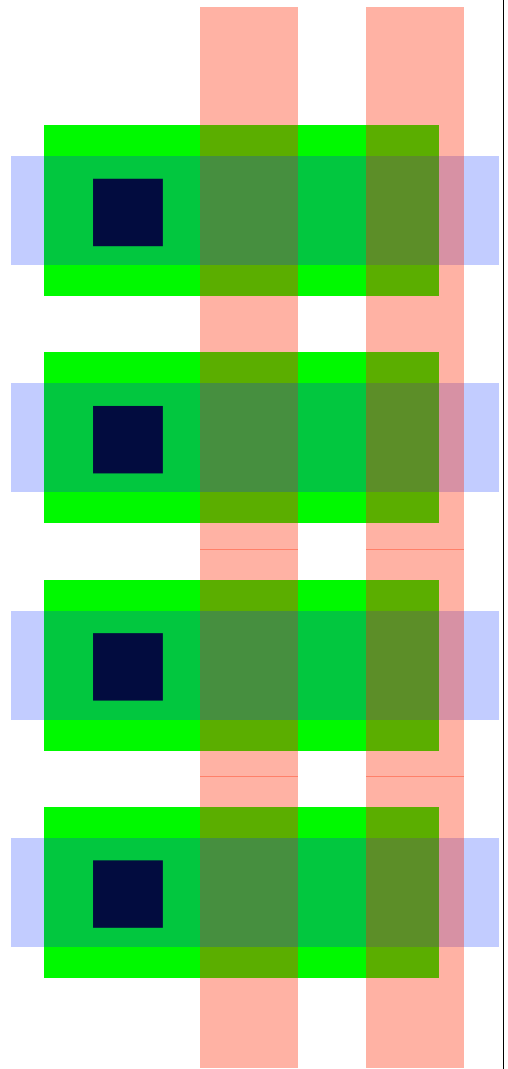
DRAM has high latency to first bit out. A fact of life.



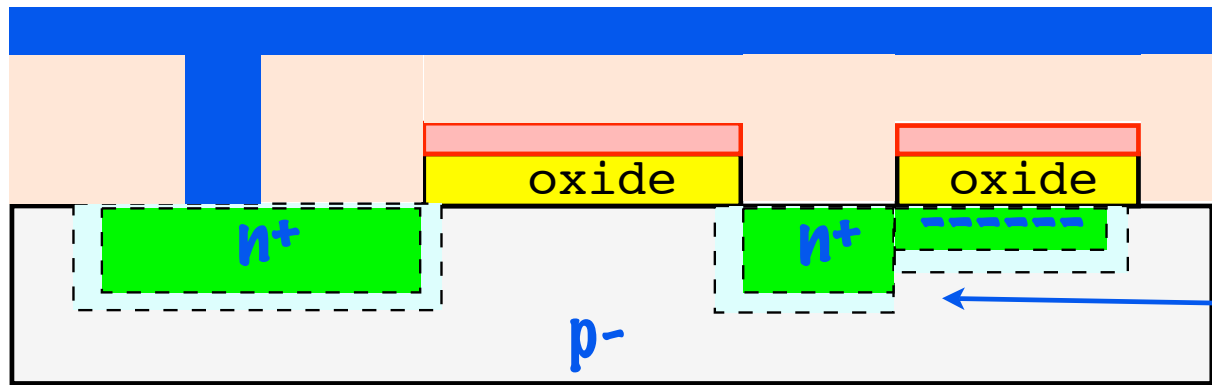
An ill-timed refresh may add to latency



Parasitic currents leak away charge.



Solution: "Refresh", by rewriting cells at regular intervals (tens of milliseconds)



Diode leakage ...

Latency is not the same as bandwidth!

Thus, push to faster DRAM interfaces

What if we want all of the 16384 bits?

In row access time (55 ns) we can do

22 transfers at 400 MT/s.

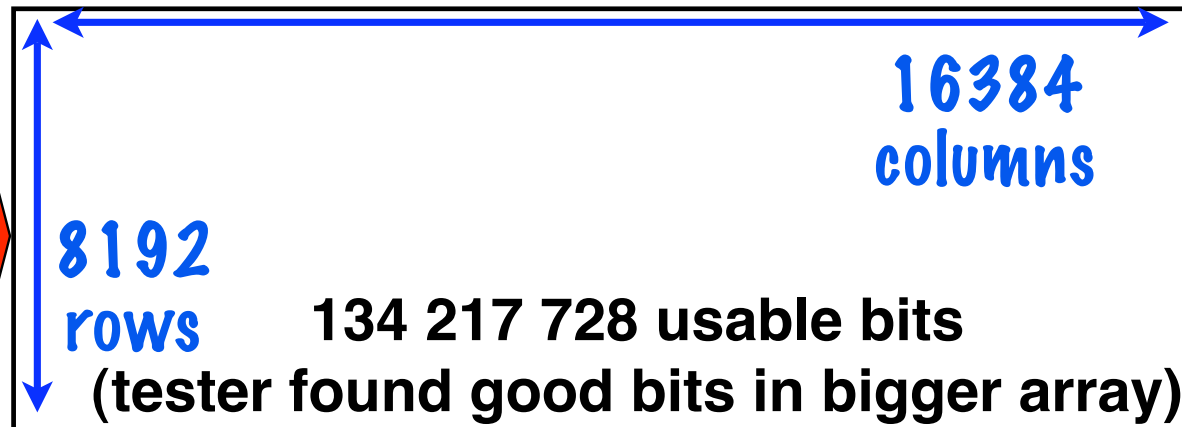
16-bit chip bus $\rightarrow 22 \times 16 = 352 \text{ bits} \ll 16384$

Now the row access time looks fast!

13-bit row address input



1
o
f
8
1
9
2
d
e
c
o
d
e
r



16384 bits delivered by sense amps



Select requested bits, send off the chip

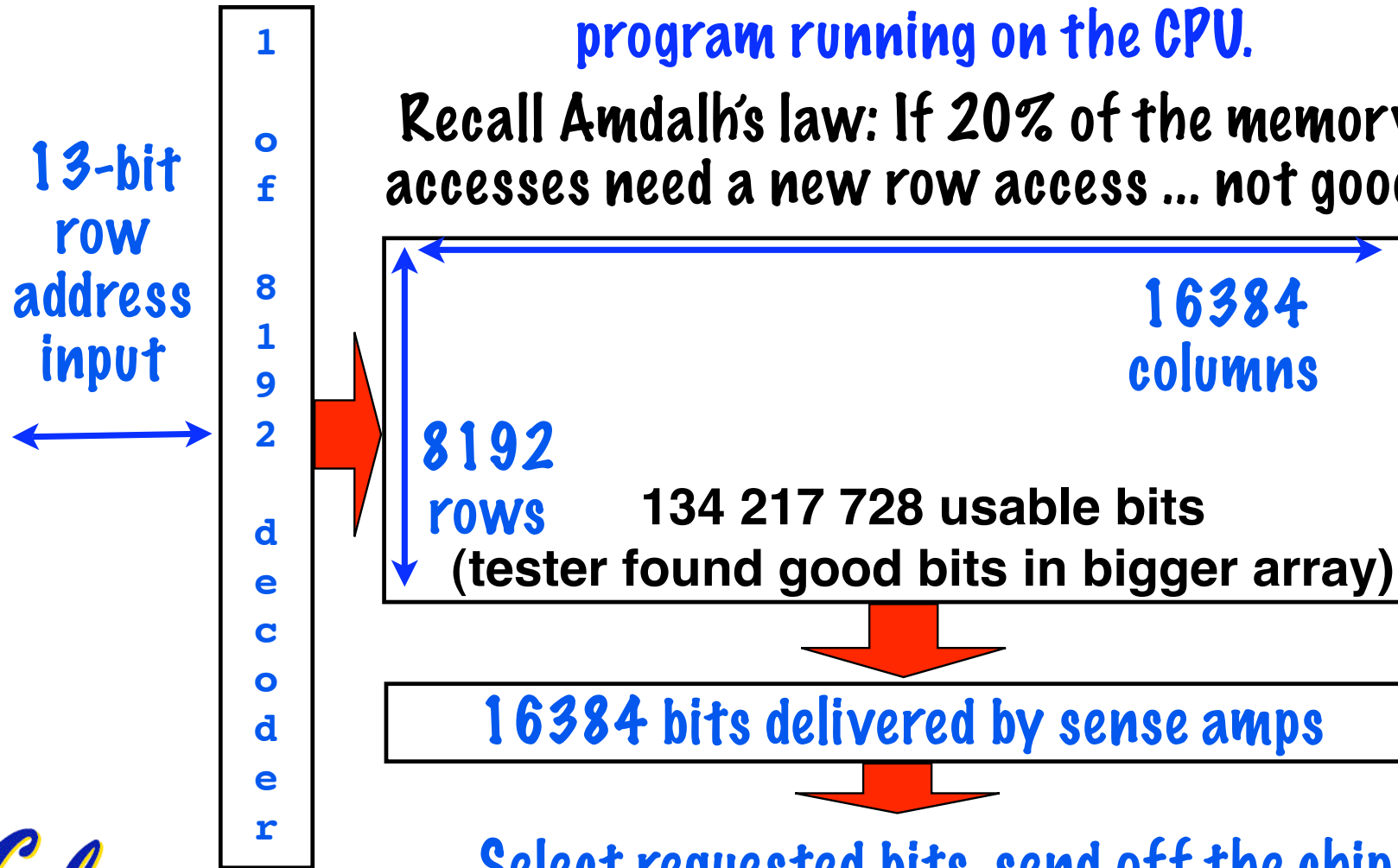


Sadly, it's rarely this good ...

What if we want all of the 16384 bits?

The "we" for a CPU would be the program running on the CPU.

Recall Amdahl's law: If 20% of the memory accesses need a new row access ... not good.



DRAM latency/bandwidth chip features



Columns: Design the right interface for CPUs to request the subset of a column of data it wishes:

16384 bits delivered by sense amps



Select requested bits, send off the chip



Interleaving: Design the right interface to the 4 memory banks on the chip, so several row requests run in parallel.

Bank 1

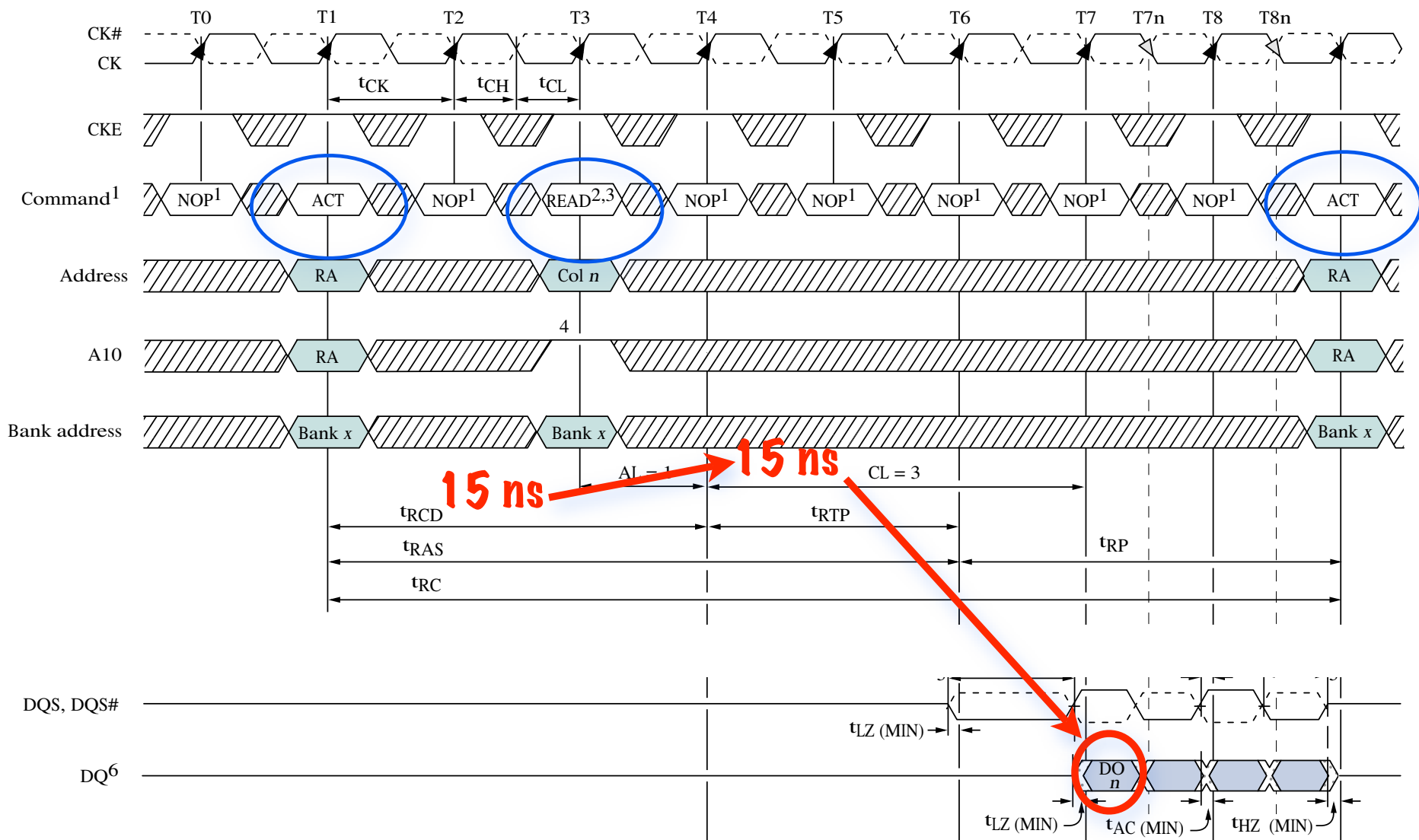
Bank 2

Bank 3

Bank 4

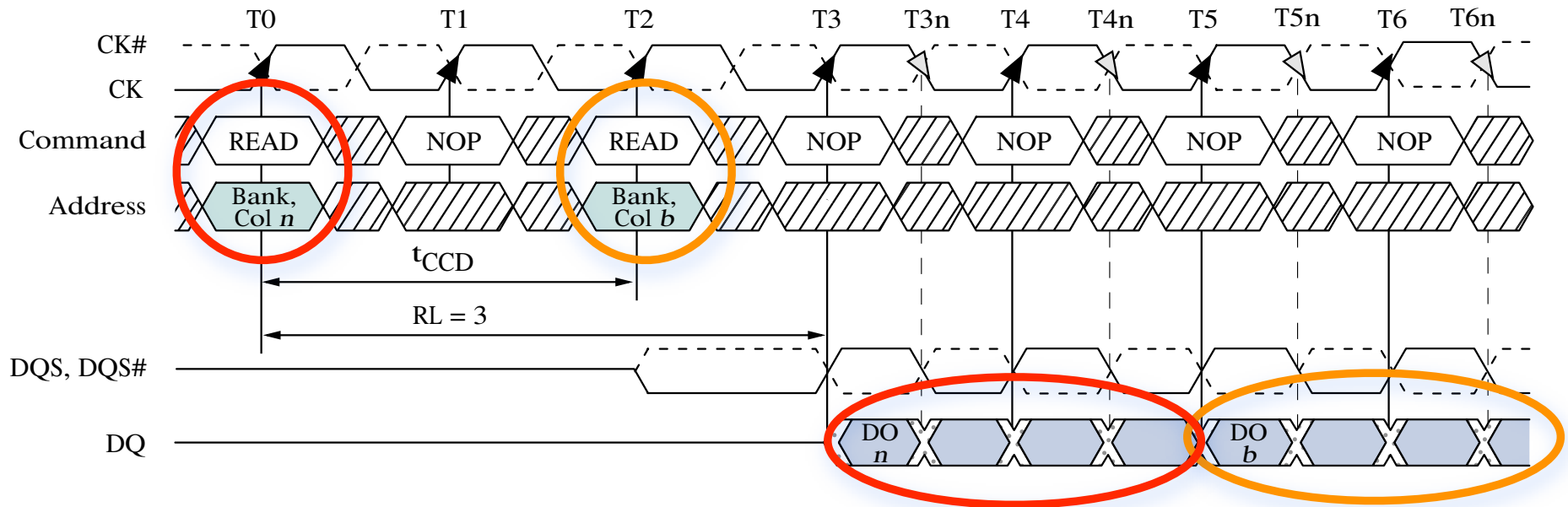


Opening a row before reading ... **Auto-Precharge READ**



55 ns between row opens.

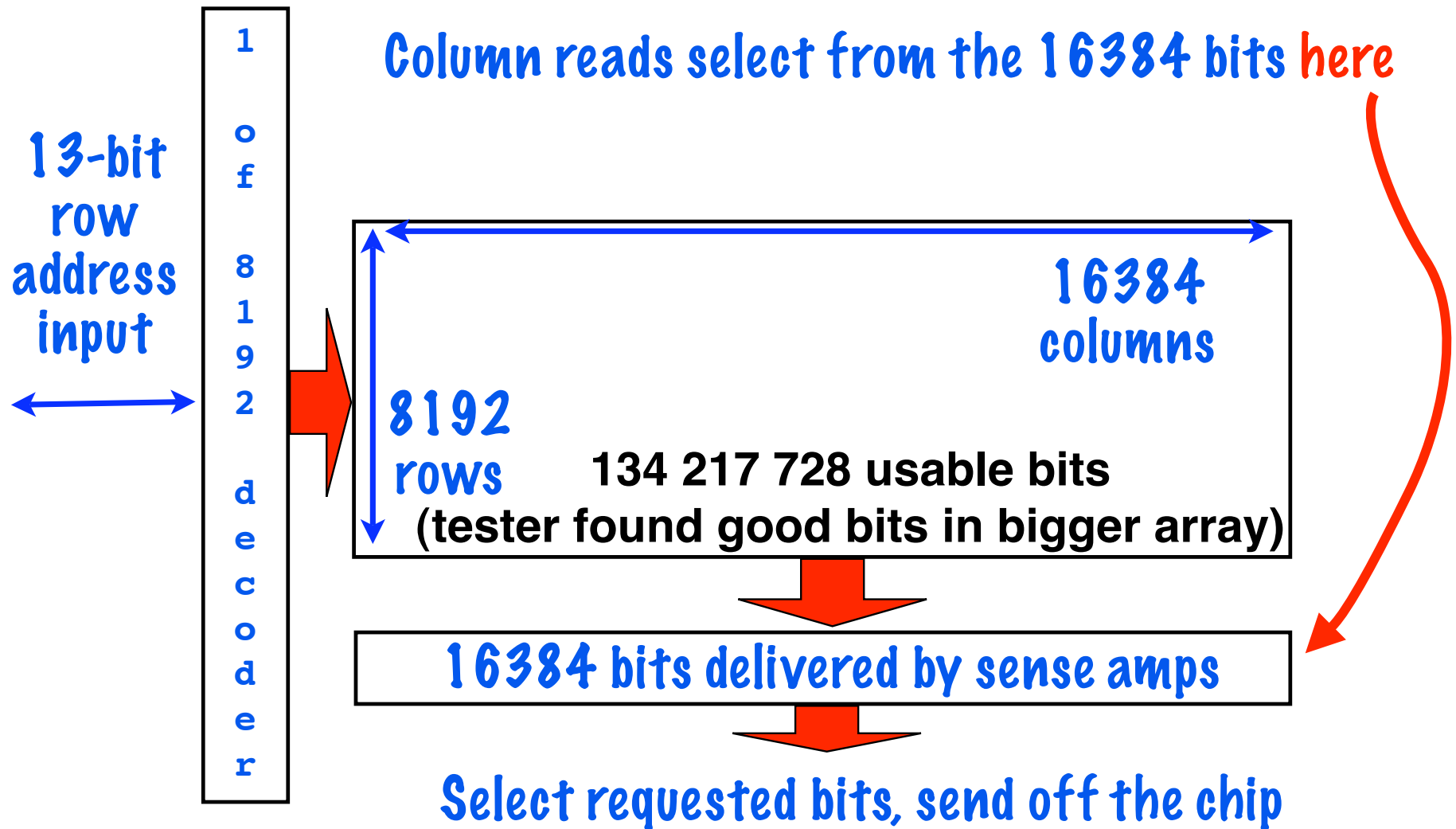
However, we can read columns quickly



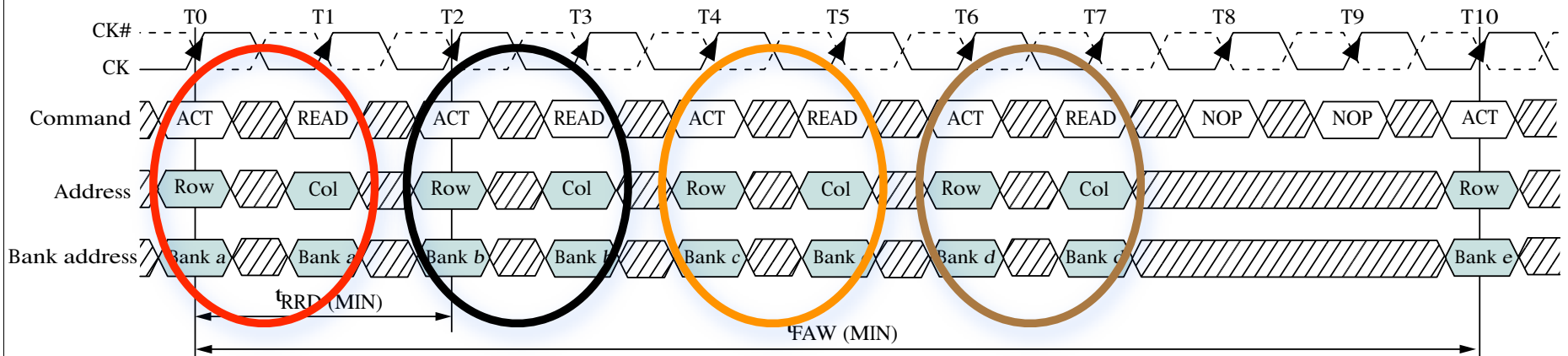
**Note: This is a “normal read” (not Auto-Precharge).
Both READs are to the same bank, but different columns.**



Why? Reading “delivered bits” is fast.



Interleave: Access all 4 banks in parallel



Interleaving: Design the right interface to the 4 memory banks on the chip, so several row requests run in parallel.

Bank a

Bank b

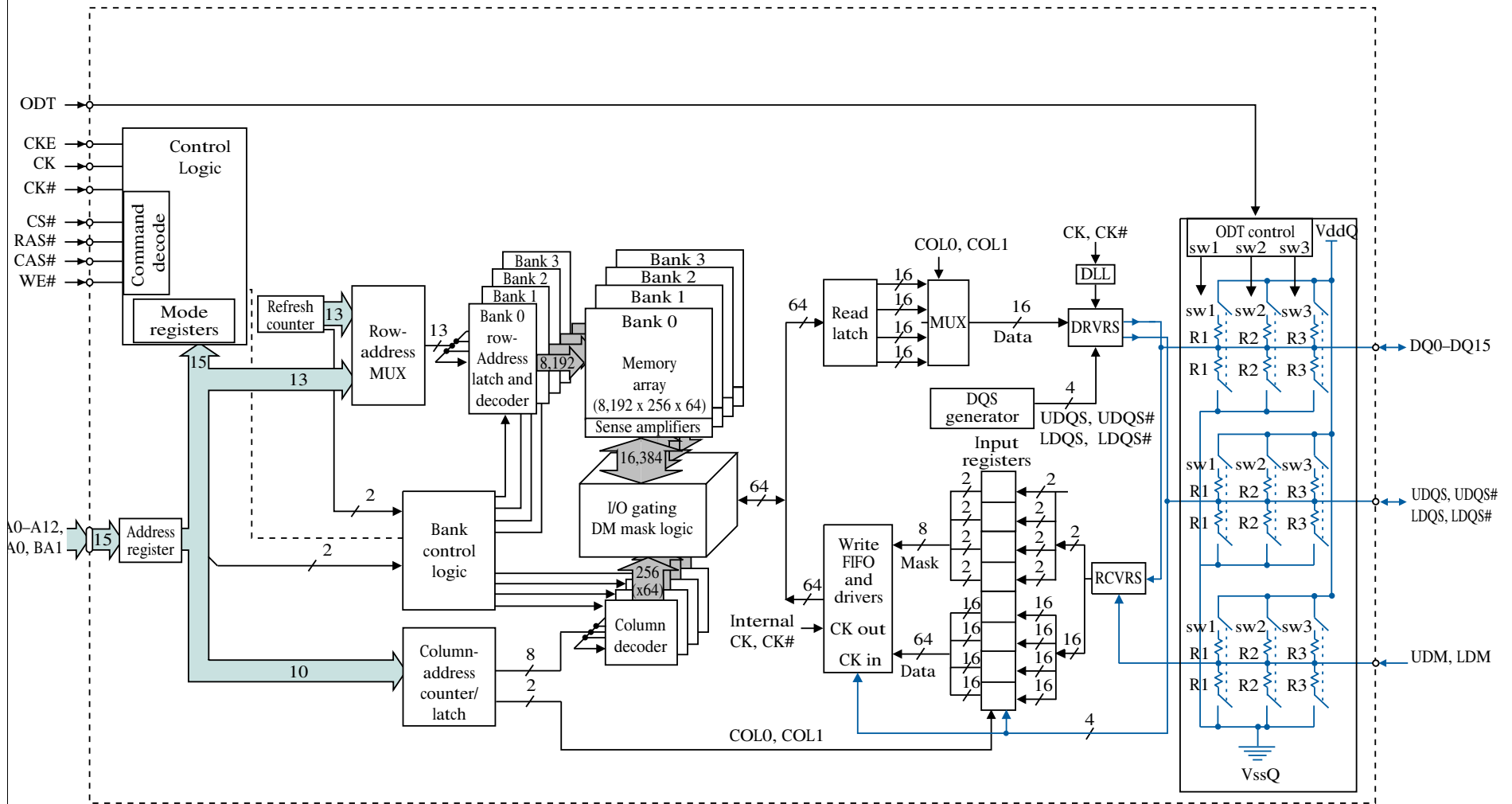
Bank c

Bank d

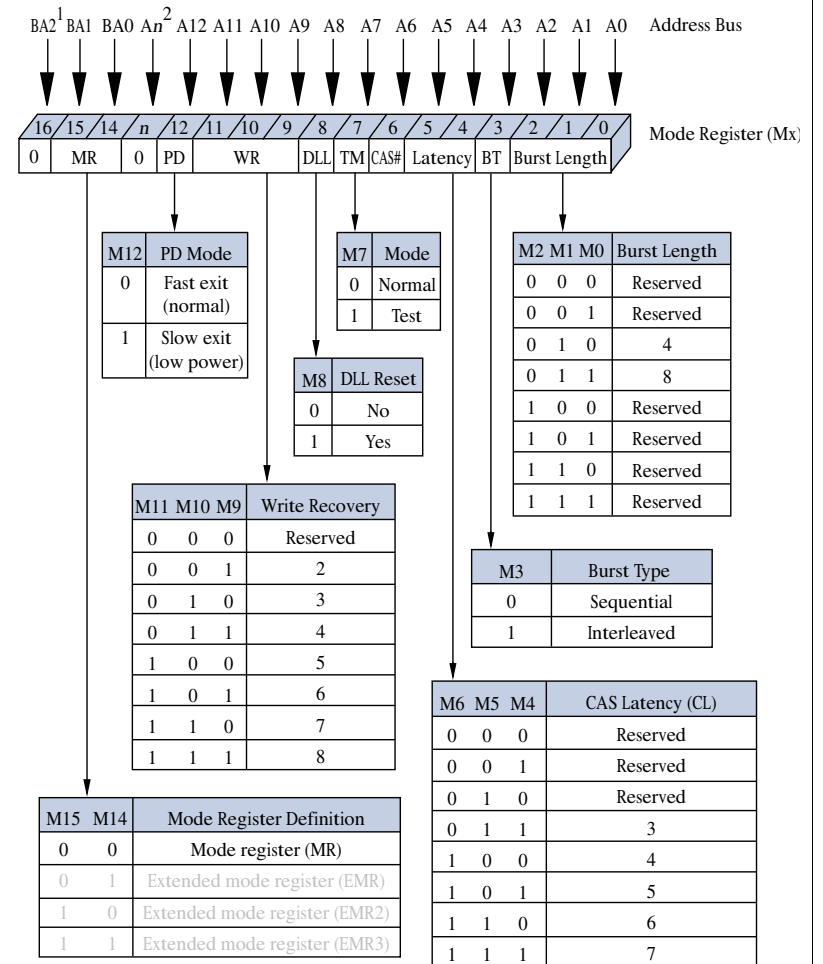
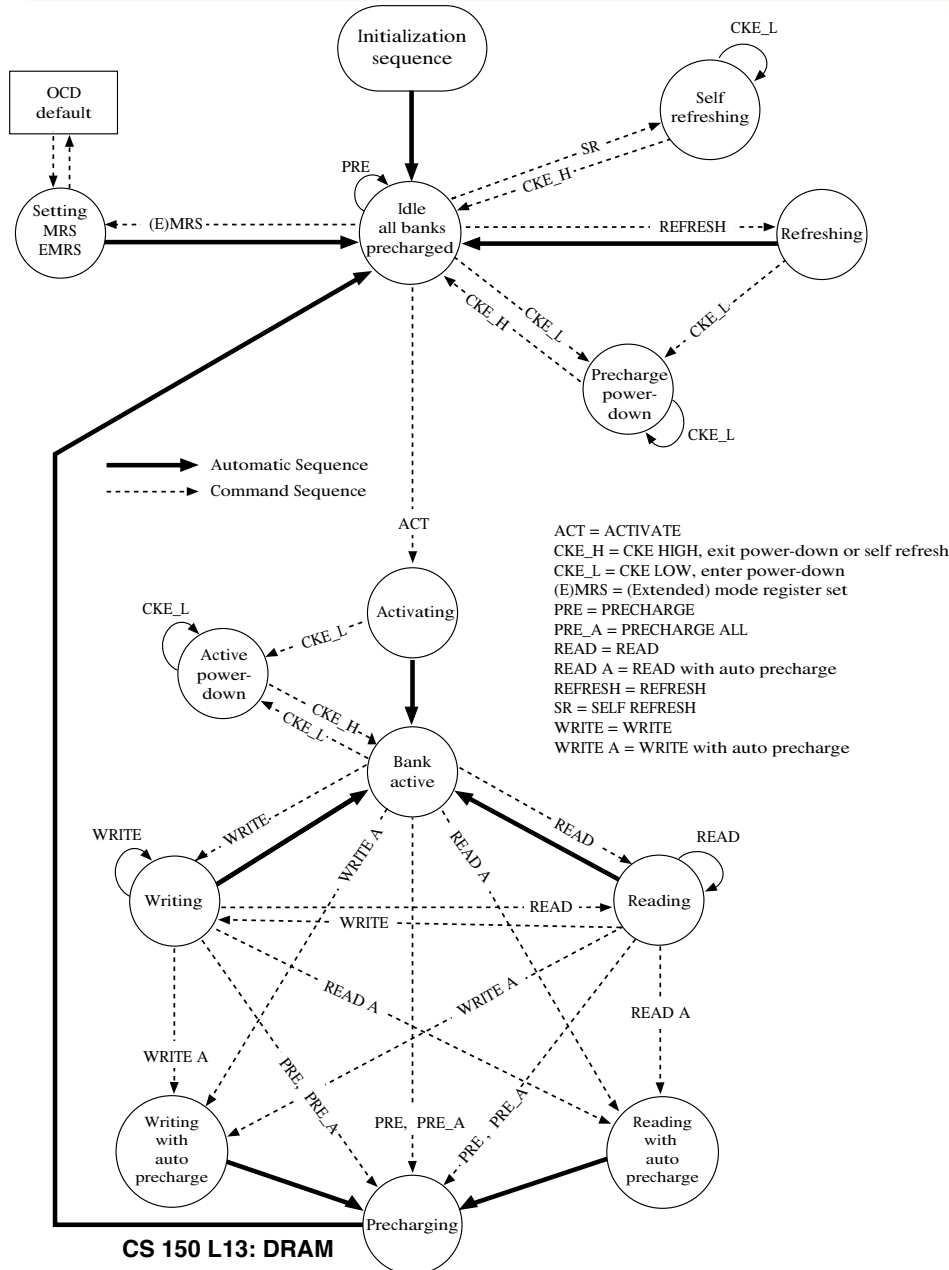
Can also do other commands on banks concurrently.



Only part of a bigger story ...

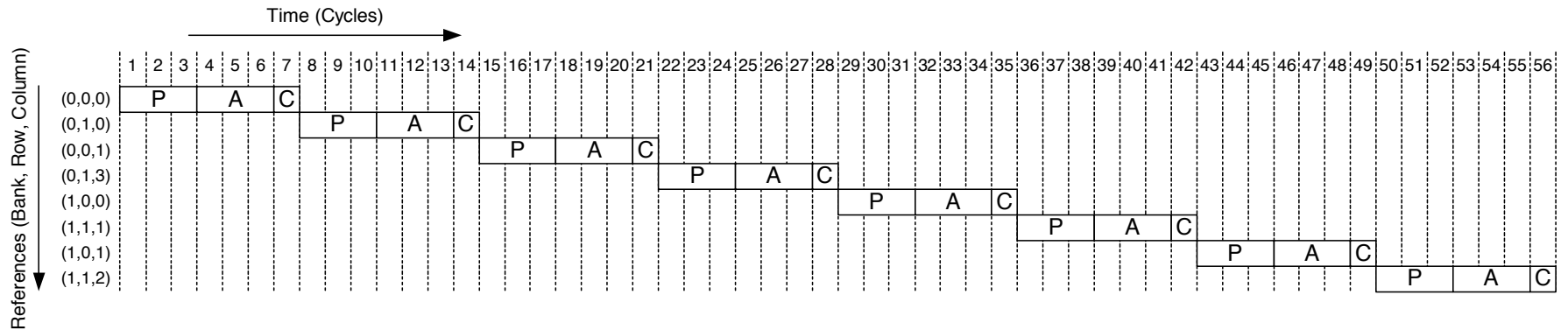


Only part of a bigger story ...

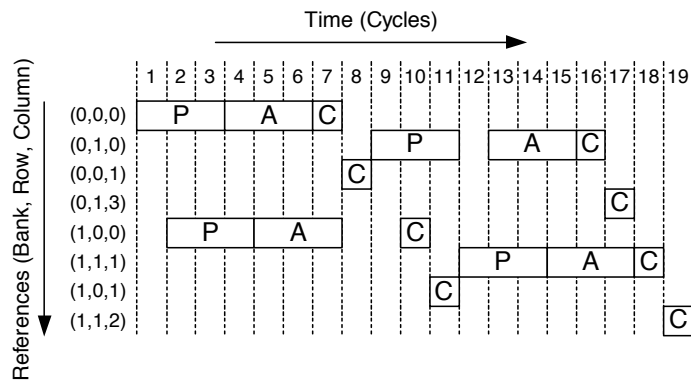


DRAM controllers: reorder requests

(A) Without access scheduling (56 DRAM Cycles)



(B) With access scheduling (19 DRAM Cycles)



DRAM Operations:

- P:** bank precharge (3 cycle occupancy)
- A:** row activation (3 cycle occupancy)
- C:** column access (1 cycle occupancy)



Present and Future ...



Intel Sandy Bridge: IDF 2010

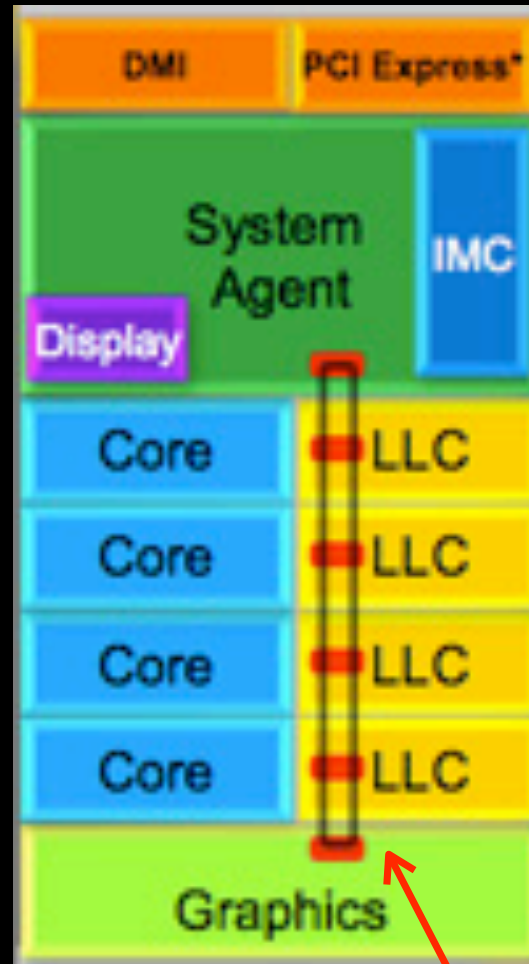
All on chip:

4 x86
cores

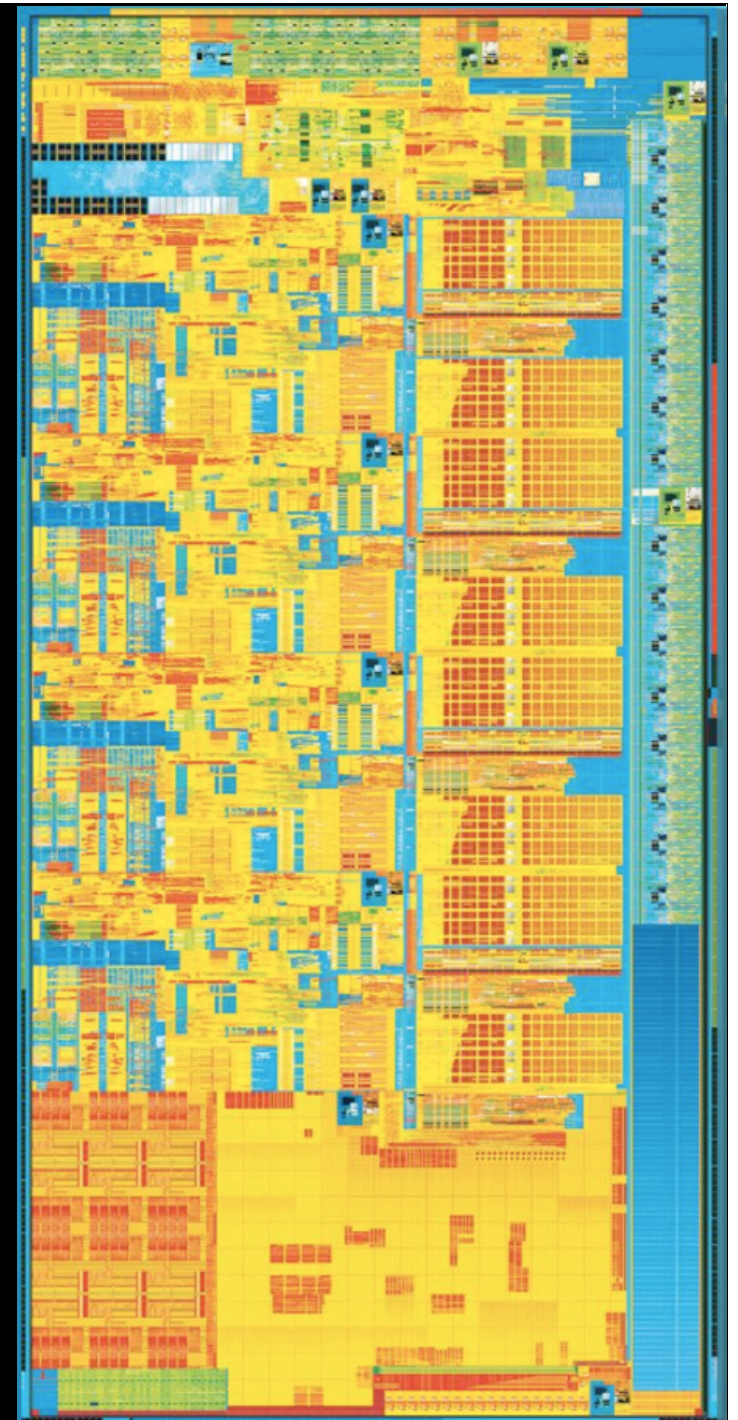
GPU

North
Bridge

DRAM
controller

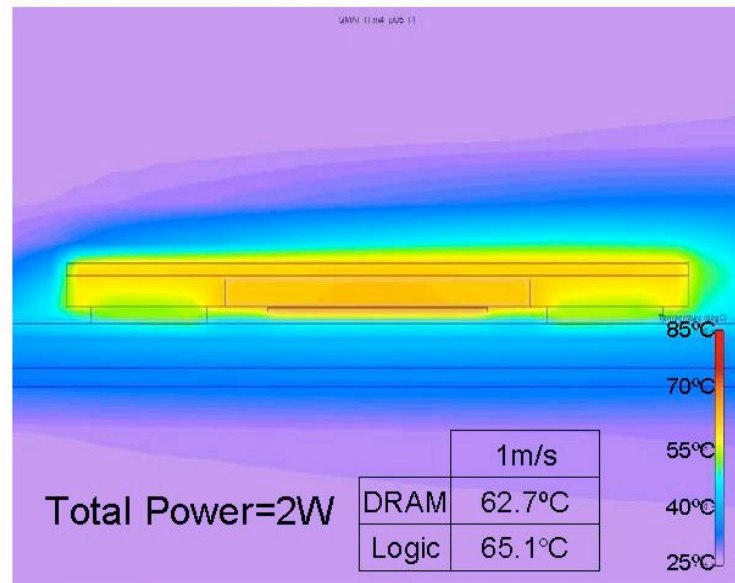
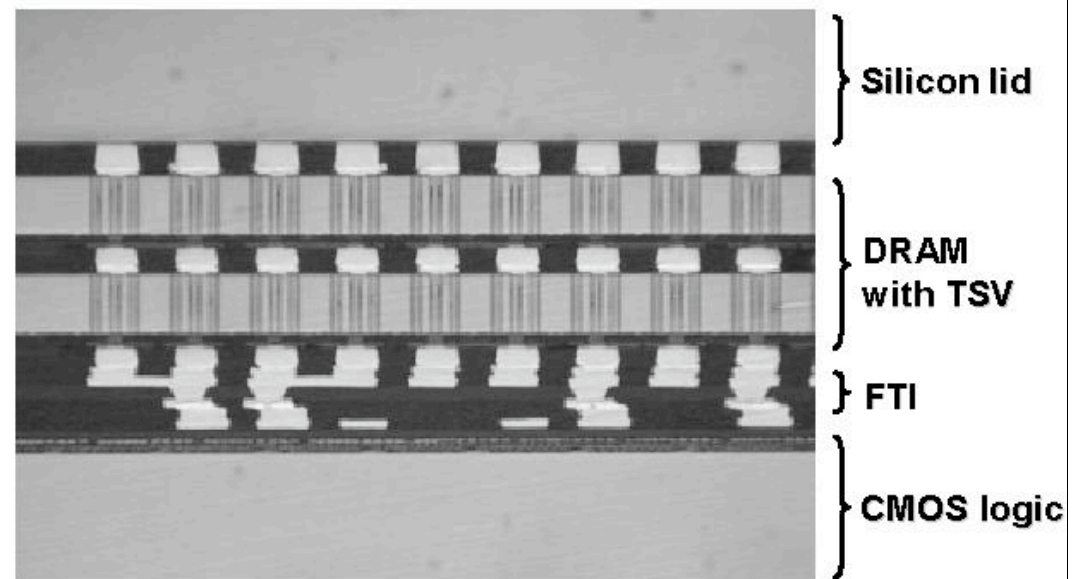
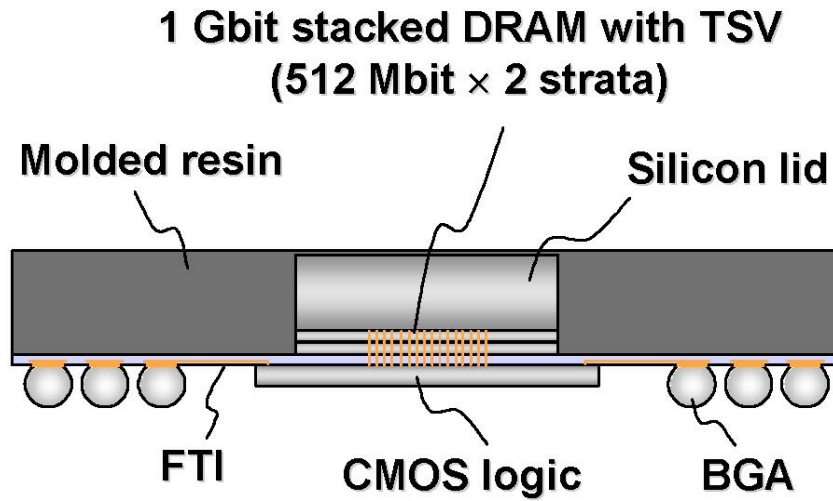


On chip ring
network



The end of DIMM

DRAM die size	10.7 mm × 13.3 mm
DRAM die thickness	50 μm
TSV count in DRAM	1,560
DRAM capacity	512 Mbit/die × 2 strata
CMOS logic die size	17.5 mm × 17.5 mm
CMOS logic die thickness	200 μm
CMOS logic bump count	3,497
CMOS logic process	0.18 μm CMOS
DRAM-logic FTI via pitch	50 μm
Package size	33 mm × 33 mm
BGA terminal	520 pin / 1mm pitch



A 3D Stacked Memory Integrated on a Logic Device Using SMAFTI Technology

Yoichiro Kurita¹, Satoshi Matsui¹, Nobuaki Takahashi¹, Koji Soejima¹, Masahiro Komuro¹, Makoto Itou¹, Chika Kakegawa¹, Masaya Kawano¹, Yoshimi Egawa², Yoshihiro Saeki², Hidekazu Kikuchi², Osamu Kato², Azusa Yanagisawa², Toshiro Mitsuhashi², Masakazu Ishino², Kayoko Shibata², Shiro Uchiyama², Junji Yamada², and Hiroaki Ikeda³

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y.kurita@necel.com

Thursday: JohnW returns ...

Thu 3/3	Lec #14: Video interface and framebuffers
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