True/False

1. If there is very high CPU utilization, then it is likely that thrashing is occurring.
   False. Thrashing is when the CPU is underutilized, but pages are being swapped out of memory aggressively.

2. If a particular IO device implements a blocking interface, then you will need multiple threads to have concurrent operations which use that device.
   True. Only with non-blocking IO can you have concurrency without multiple threads.

3. For IO devices which receive new data very frequently, it is more efficient to interrupt the CPU than to have the CPU poll the device.
   False. IT is more efficient to poll, since the CPU will get overwhelmed with interrupts.

Short Answer

4. Two-level Page Tables:

   i) Give a two to three sentence description of a two-level page table.
   Split the virtual address into an offset and two page table indices instead of just one. The first page table's result points to a second page table. The second page table's result points to the actual location of the data in physical memory.

   ii) Briefly (2 sentences) state one advantage AND one disadvantage of two-level page tables.
   + Better for sparse address spaces, easier memory sharing between processes, easier memory allocation
   - 2 lookups per reference, use 1 extra page table of memory in the worst case

5. What is Belady's anomaly and which page replacement algorithm(s) could display it?
   Belady's anomaly refers to having more page faults when increasing the amount of memory a system has. FIFO is subject to this, as contents of memory with X pages is not a subset of contents with X+1 pages.

6. We looked at disabling CPU interrupts as a simple way to create a critical section in the kernel. Name two drawbacks of this approach. One of them should be a problem that is exacerbated by trends in modern computer hardware.

One issue is that you can't receive interrupts from devices or timers within a critical section, which may be desired. For instance, what if you accidentally have an infinite loop in the kernel critical section? A second issue is that it is difficult to disable interrupts on multiple cores.

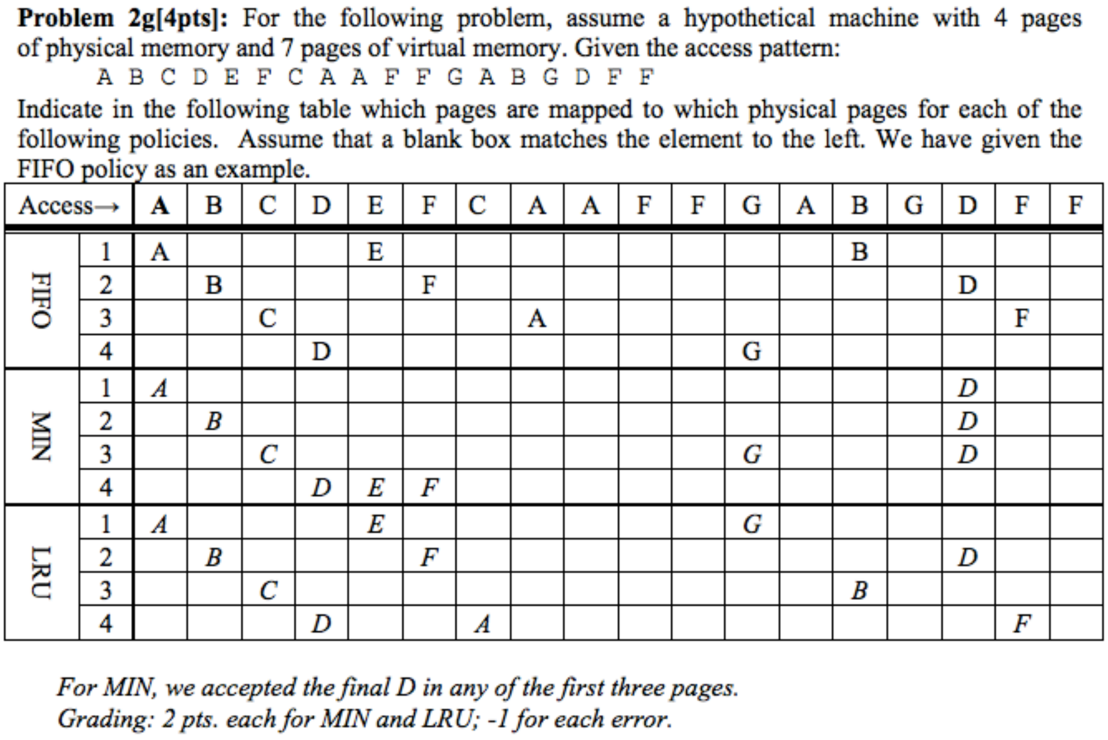
Longer Answer

7. Below is a pseudo-code for the clock page replacement algorithm (we are assuming the clock is entirely "full" with pages, and a new page must be found. Fill in the blank:

```
replaced = false;
while (!replace) {
        1. if (current page use_bit == 0) {replace page,
           replaced = true}

           else {use_bit = 0}

        2. Advance clock hand
```



Problem 2g[4pts]: For the following problem, assume a hypothetical machine with 4 pages of physical memory and 7 pages of virtual memory. Given the access pattern:

A B C D E F C A A F F G A B G D F F

Indicate in the following table which pages are mapped to which physical pages for each of the following policies. Assume that a blank box matches the element to the left. We have given the FIFO policy as an example.

Access→		A	B	C	D	E	F	C	A	A	F	F	G	A	B	G	D	F	F
FIFO	1	A				E									B				
	2		B				F										D		
	3			C					A									F	
	4				D								G						
MIN	1	*A*															*D*		
	2		*B*														*D*		
	3			*C*									*G*				*D*		
	4				*D*	*E*	*F*												
LRU	1	*A*				*E*							*G*						
	2		*B*				*F*										*D*		
	3			*C*											*B*				
	4				*D*			*A*										*F*	

For MIN, we accepted the final D in any of the first three pages.
Grading: 2 pts. each for MIN and LRU; -1 for each error.