Demand Paging

True or False: Adding more RAM reduces the number of page faults that occur in a system.

True or False: Compulsory misses in a cache can be reduced with prefetching.

True or False: The Clock Algorithm requires hardware support for a "use" bit in the PTE.

True or False: The Clock Algorithm swaps the oldest page to disk on a page fault.

True or False: LRU swaps the oldest to disk on a page fault (age is defined by amount of time in RAM).

True or False: One advantage of a software TLB is that the same hardware platform can support both forward and inverse page tables.

Why is it easier to deal with "precise exceptions" as opposed to "imprecise exceptions"?

Why is LRU not implemented in practice?

Briefly describe what happens during a page fault:

- 1)
- 2)
- 3)
- 4)
- 5)
- 6)

[Do this question last]: If the hardware is incapable of supporting dirty/used bits, but valid/writable bits can be set, then how do you implement the clock algorithm?

Fill in the following tables. Each column represents a time-step. If there is no page fault during that time-step, leave the column blank. For each policy:

Briefly describe how it works. List a disadvantage. Compute how many page faults there are.

FIFO Policy:

-		/													_
P hys	А	В	С	D	D	E	E	С	В	A	D	E	С	В	А
1	А														
2		В													
3			С												

MIN Policy:

	r int i one j.														
Р	Α	В	C	D	D	E	E	С	В	Α	D	Е	C	В	А
hys															
1	A														
2		В													
3			C												

LRU Policy:

P hvs	A	В	С	D	D	E	E	С	В	A	D	E	С	В	A
11,95															
1	A														
2		В													
3			С												

Clock Policy:

Р	А	C	В	D	В	А	E	F	В	F	А	G	E	F	А
nys															
1	Α														
2		В													
3			С												
4															