

TITLE CS61CL

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ALL Program

int main ( ) {

3 weeks

Assembly  
Lungou

MPS R7000

Machino Lanza

Ld R1, R3, R4

ADD R2, M R4

ST

.data

main: .int16. 01

3 weeks



Executable



I/O

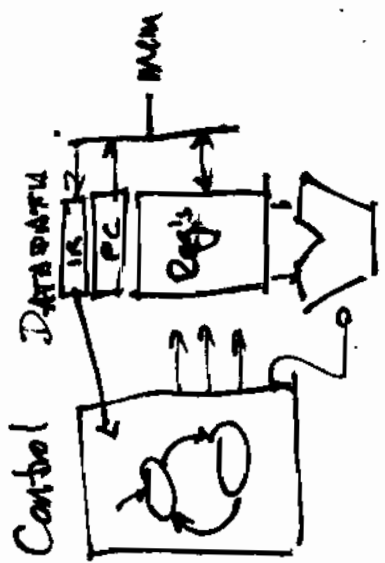
memories

Proc

3 weeks

Run time  
System

CALL6



Control

DATA PATH

IR

PC

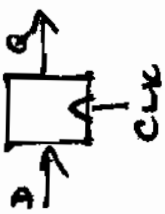
Reg's

CPU

MEM

Combinational  
Logic

Synchronizing  
Circuit  
(State)



3 weeks

3 weeks

Optimization  
- Performance  
- Power

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Witnessed & Understood by me, \_\_\_\_\_

Date \_\_\_\_\_

Invented by \_\_\_\_\_

Date \_\_\_\_\_

Recorded by \_\_\_\_\_