EE42/100 Spring 2006 Problem Set 12

Issued: Apr 20, 2006 Due: Apr 28, 2006

Please remember that homeworks are due at 12:00 noon Friday January 26.
Please put your homework in the appropriate box (EE42 or EE100) in 240 Cory Hall.
Print your name(s) in upper right corner of your paper and indicate whether you're enrolled in EE42 or EE100.

1. (Reading Assignment) Chapter 8 in Hambley 3rd edition.

2. (Schwarz and Oldham P12.18) For the system of Fig. 1:
   a. Construct a state table. Assume that initially $\mathbf{Q}_1 = \mathbf{1}$, $\mathbf{Q}_2 = \mathbf{Q}_3 = \mathbf{Q}_4 = \mathbf{0}$.
   b. Construct a state diagram for $\mathbf{Q}_1\mathbf{Q}_2\mathbf{Q}_3\mathbf{Q}_4$.

3. (Schwarz and Oldham P12.19) For the system of Fig. 1, construct a complete state diagram showing all 16 states of your system. Your diagram should have 16 circles, numbered 0000 through 1111, connected with arrows showing which state each state goes to after one tick of the clock. Interestingly, this system has a *limited cycle*: that is, no matter which state it starts in, it end up going repetitively through the same sequences of states. Find the limit cycle.

4. (Schwarz and Oldham P12.20) The system of Fig. 1 is known as a 4-bit *ring counter* because it can be used to give an output of **1** after every fourth clock pulse. Show how it can be used in this way. Can you design a system that gives an output of **1** after every *fifth* clock pulse?

5. (Schwarz and Oldham P12.21) We wish to design a system that gives an output of **1** after every 60 input pulses. (This system, which should be called a *divide-by-sixty counter*, could be used in a household clock. It would move a second hand one notch after every 60 cycles of the 60 Hz electric power line.) Design a suitable system using three ring counters. Do not use more than a total of 12 flip-flops.

6. (Schwarz and Oldham P12.22) Fig. 2 shows a 3-bit *Johnson counter*. Construct a complete state diagram showing all eight possible states. Show that the system has two different limit cycles. Show how (with the addition of one gate) it can be used as a divide-by-six counter.

7. (Schwarz and Oldham P12.23) A 5-bit Johnson counter is shown in Fig. 3. Show that, depending on the initial values of $\mathbf{Q}_1 ... \mathbf{Q}_5$, the device finds itself in one of four different limit cycles (repetitive sequences of states). Find the limit cycle that contains only two states.

8. (Schwarz and Oldham P12.24) In Fig. 4 the clock input is a train of regularly spaced pulses. Construct state diagrams for $\mathbf{Q_1Q_2}$ as follows:
    a. When input **A** = **1**.
    b. When input **A** = **0**.
    c. Sketch timing diagrams showing $\mathbf{Q_1}$ and $\mathbf{Q_2}$ as functions of time for the two cases **A** = **1** and **A** = **0**.
    d. Explain in words how the timing diagrams differ in the two cases.

9. (Schwarz and Oldham P12.25) Design am 8-bit digital-to-analog converter for which the full-scale voltage (output corresponding to an input FF_{16}) is 10V.

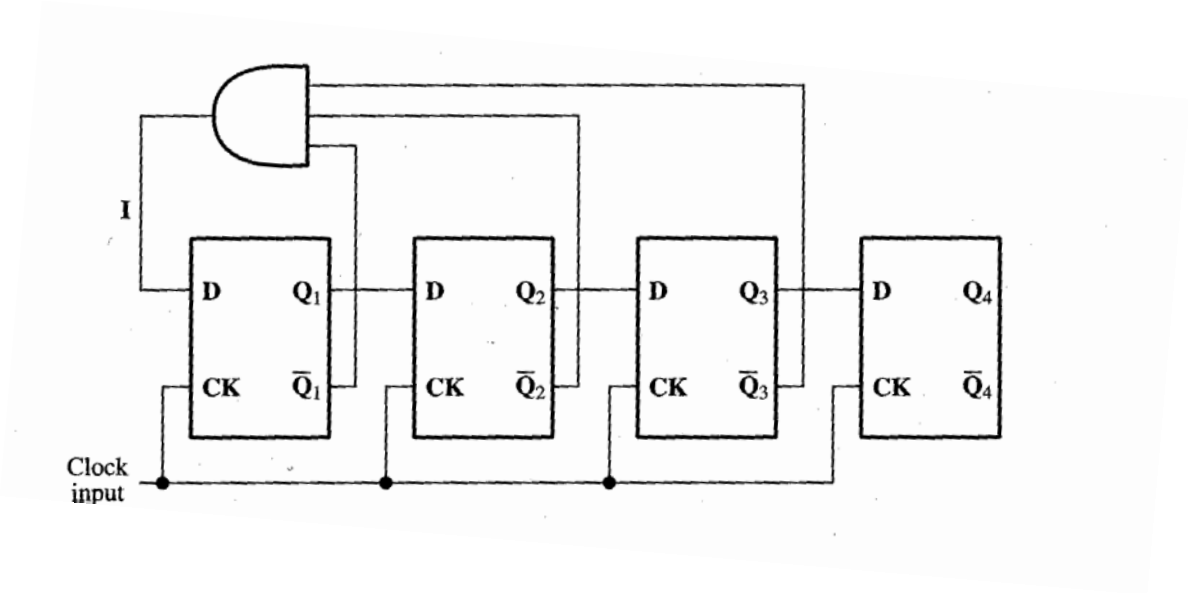

Figure 1

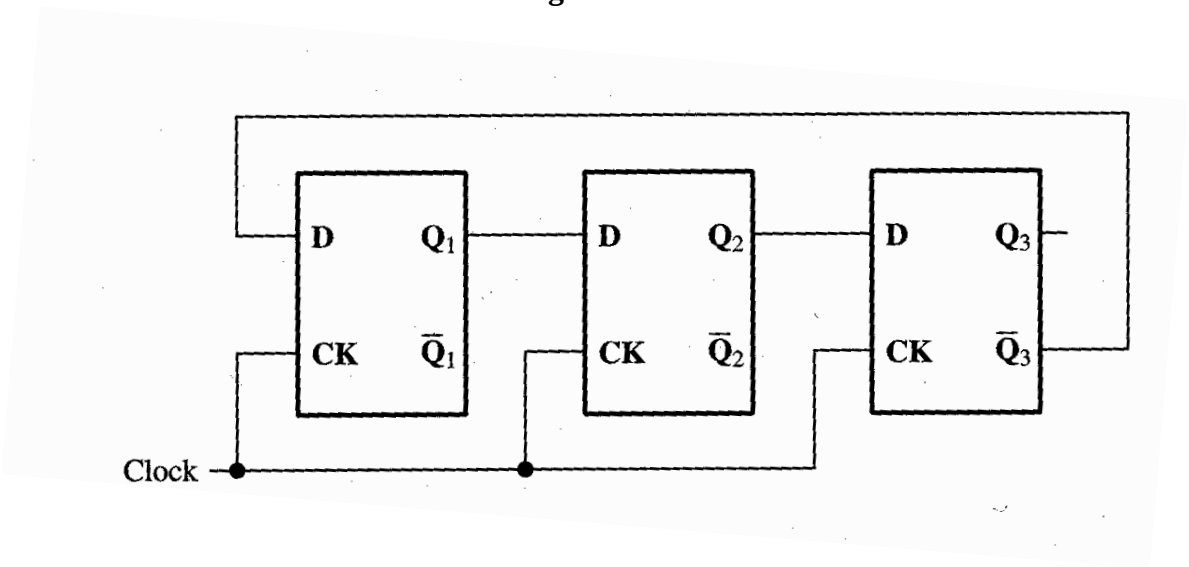

Figure 2

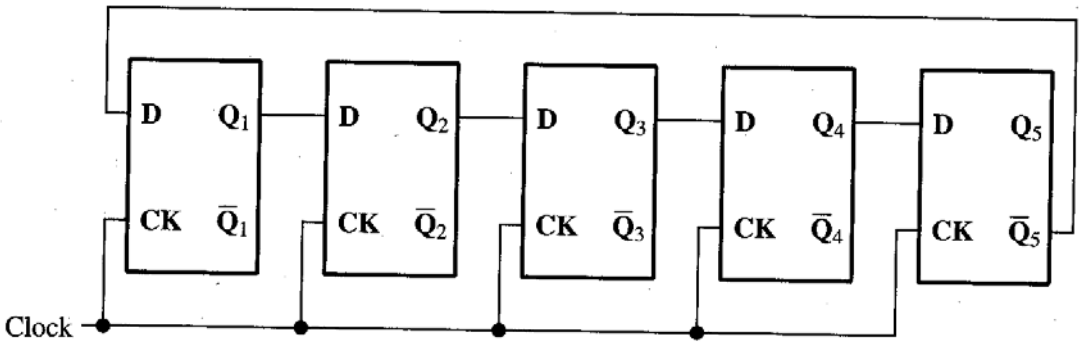

Figure 3

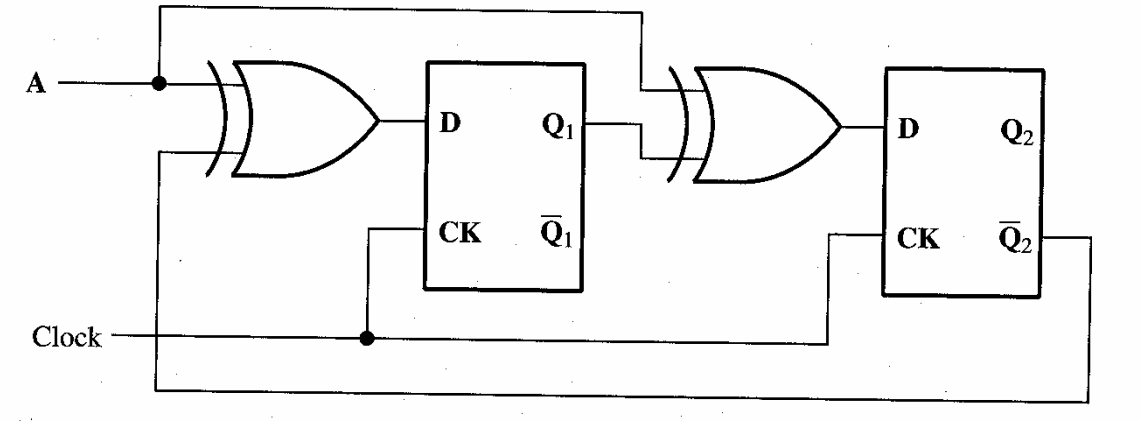

Figure 4