

Digital Logic Prelab

1. The Sum of Products canonical form

Consider the truth table for the XOR gate:

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

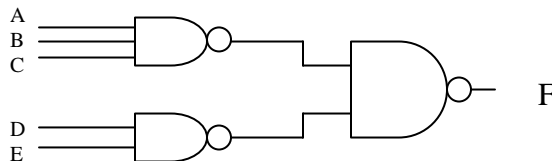
Determine the **SUM-OF-PRODUCTS** form for the XOR function F above.

2. NAND Implementation

(a) Using DeMorgan's theorem:

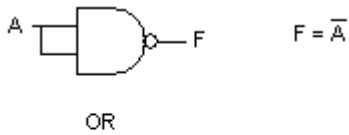
$$\begin{aligned} \overline{A + B} &= \overline{A} \cdot \overline{B} \\ \overline{AB} &= \overline{A} + \overline{B} \end{aligned}$$

rewrite your expression for F from question 1 above using **ONLY NAND** functions. (Hint: this is covered in most texts, e.g. in Schwarz and Oldham via problems 11.14-11.17.) You may shortcut this process and get your inspiration by simply writing out the sum of products logic expression for the following general circuit:

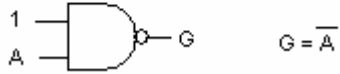


Stare at this expression and stare at the circuit. You should now be able to draw the circuit for any sum of products expression using NAND gates. (It takes one NAND gate for each product term and one to combine them. It may take some more to provide the NOT function if some of the inputs have bars over them.)

(b) Draw the complete schematic for the **NAND-ONLY** implementation of function F. Hint: To realize a NOT gate, see below. Note that one of these gates loads A with two inputs, but the other loads A by only one input.



OR



(c) What is the loading (fanout, number of gate inputs driven) for each individual NAND gate output in the XOR circuit? How might this affect the gate delay of each of the NAND gates? (qualitative answer)