ECE 461: Digital Communication

Lecture 8a: Capacity of the AWGN Channel

Introduction

In the last two lectures we have seen that it is possible to communicate rate efficiently and reliably. In this lecture we will see what the fundamental limit to the largest rate of such a reliable communication strategy is.

Power Constraint

In our discussion so far, we have considered the energy constraint on the transmit voltages:

$$|x[m]| \leq \sqrt{E}, \quad \forall m. \tag{1}$$

This constraint is also called a *peak power* constraint. An alternative and weaker constraint is on the average power:

$$\sum_{m=1}^{N} |x[m]|^2 \leq NE. \tag{2}$$

The peak power constraint in Equation (1) implies the average power constraint in Equation (2), but not vice versa. In this lecture we will consider the weaker average transmit power constraint. Our focus is the usual AWGN channel

$$y[m] = x[m] + w[m], \quad m = 1, \ldots \tag{3}$$

where $w[m]$ is i.i.d. (independent and identically distributed) with statistics at any time being Gaussian (zero mean and variance σ^2). In the last two lectures we had restricted the transmit voltage to be one of only two possible voltages ($\pm\sqrt{E}$), now we allow any real voltage as long as the average power constraint in Equation (2) is met. We will denote the ratio

$$\mathsf{SNR} \stackrel{\text{def}}{=} \frac{E}{\sigma^2} \tag{4}$$

as the signal to noise ratio of the channel.

Capacity

It turns out that the largest rate of arbitrarily reliable communication is

$$C_{\text{awgn}} \stackrel{\text{def}}{=} \frac{1}{2} \log_2 (1 + \mathsf{SNR}) \quad \text{bits/channel use.} \tag{5}$$

It is instructive to see how the capacity performs at low and high SNRs.

At high SNR, we can approximate $1 + \mathsf{SNR}$ by SNR and then

$$C_{\text{awgn}} \approx \frac{1}{2} \log_2 \mathsf{SNR} \quad \text{bits/channel use.} \tag{6}$$

We see that for every quadrupling of SNR the capacity increases by one bit. This is exactly the same behavior we have seen very early in this course, indeed way back in Lecture 1.

At low SNR, we have

$$C_{\text{awgn}} \approx \frac{1}{2} (\log_2 e)\, \mathsf{SNR} \quad \text{bits/channel use.} \tag{7}$$

In this situation a quadrupling of SNR also quadruples the capacity due to the linear relation between capacity and SNR.

Transmitter and Receiver Designs

How do the transmitter and receiver strategies that hope to work close to this fundamental limit look like?

- *Transmitter*: In our attempts to understand reliable communication at non-zero rates (in the last two lectures) we divided the transmitter strategy into two parts:
  - *coding*: mapping the information bits into coded bits; this is done at the block level. We focused specifically on *linear* coding.
  - *modulation*: mapping the coded bits into transmit voltages; this is done sequentially.

  It turns out that essentially the same steps continue to work even in attaining the fundamental reliable rate of communication in Equation (5). At low SNRs, binary modulation suffices. At high SNR, the modulation involves larger alphabets and is also done in a block manner, albeit the modulation block size is usually smaller than the coding block size.

- *Receiver*: In our study of the erasure channel in the previous lecture, we saw a fairly simple receiver structure. In this general setting, the receiver is more involved: the ML receiver is hopeless (computationally) to implement. Harnessing the understanding gleamed from the erasure channel codes, a class of suboptimal (compared to ML) receiver techniques that are simple to implement have been developed in the last decade. Specifically, these receivers *iterate* by alternating between demodulation and linear decoding, eventually converging to the true information bit transmitted. This study is somewhat out of the scope of this course. We will provide some reading material for those interested in this literature at a later point.

Looking Ahead

So far we have focused on the discrete time additive noise channel (cf. Equation (3)). We arrived at this model in Lecture 1 by using the engineering blocks of DAC (digital to analog conversion) and ADC (analog to digital conversion) at the transmitter and receiver, respectively. In the next lecture, we take a closer look at the DAC and ADC blocks in terms of how their design impacts the end-to-end communication process. Of specific interest will be what constrains the rate of discretization. Clearly, the larger this rate, the larger the capacity of

the end-to-end communication. We will see that the *bandwidth* of the transmit signal plays an important role in constraining the number of channel uses per second. Further we will be able to discuss the relation between the largest rate of reliable communication and the key physical resources available to the engineer: power and bandwidth.