UNIVERSITY OF CALIFORNIA
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EE 130 Prof. Liu
Fall 2013

NMOSFET Design Project

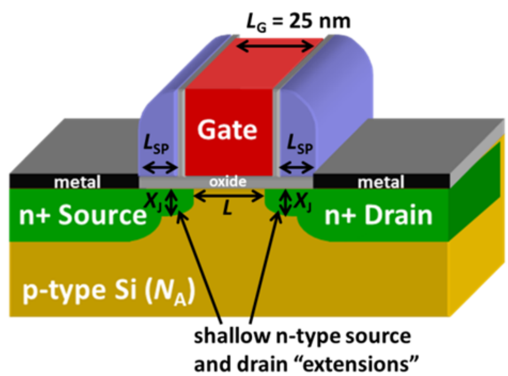
Due at 5PM PST on Thursday December 12, 2013

Introduction

In this project, you will use semiconductor device simulation software (Synopsys' Sentaurus package) to design an n-channel silicon MOSFET with gate length L_G = 25 nm (relevant for the "20 nm generation" of CMOS technology) to meet specified performance requirements within some practical design constraints. The simulator represents the transistor structure as a mesh of points, keeping track of the material properties and net dopant concentration (within a semiconductor material) at each point and self-consistently solving the Poisson equation and continuity equations to find the mobile charge carrier (electron and hole) concentrations, electric field, electric potential and current flow at each point. Analytical models are used to calculate the effective mass and carrier mobilities, and to account for phenomena such as band gap narrowing, generation-recombination, band-to-band (Zener) tunneling and velocity saturation. For a specified device structure and operating conditions (*i.e.* bias voltages and temperature), then, it can derive the terminal currents. If the device structure is described in only two dimensions (as is the case for this project), then the simulator assumes that the device width (*i.e.* the width of the MOSFET channel) is 1 micron.

MOSFET Structure

The channel region and "body" of the MOSFET are uniformly doped p-type, with dopant concentration $\boldsymbol{N_A}$. To mitigate the short-channel effect, the MOSFET structure comprises shallow n-type source/drain "extension" regions adjacent to the channel region; to mitigate parasitic series resistance, deeper and more heavily doped junctions are used in the regions where metallic contacts are made to the source and drain.



In practice, the n-type source/drain extension (SDE) regions are formed by implantation of dopants into the Si; the gate electrode blocks this implant from reaching the channel region, so that the SDE regions are naturally aligned to the gate electrode edges. The SDE junction depth $\boldsymbol{X_J}$ is determined by the implantation energy and post-implant thermal annealing conditions. (Annealing at a high temperature – typically greater than 900 degrees Celsius – is necessary to repair the implantation-induced damage to the crystalline lattice, such that dopant atoms reside on Si lattice sites.) Due to lateral "straggle" inherent to the implantation process, and dopant diffusion during the high-temperature annealing step, the channel length L is slightly smaller than the gate length L_G; **the deeper X_J is, the smaller L is**. The deep n+ source/drain regions are also formed by implantation of dopants (but at a higher energy and dosage than used to form the SDE regions), after the formation of dielectric (SiO_2 and/or Si_3N_4) "spacers" of length $\boldsymbol{L_{SP}}$ along the sidewalls of the gate electrode. The spacers serve to block this implant so that the deep source/drain regions are offset from the channel region. The longer L_{SP} is, the longer the length of the SDE regions (which have higher resistivity than the deep source/drain regions).

Fixed Design Parameters

Values for the following transistor parameters are fixed (*i.e.* you will not be allowed to adjust them), based on the *International Technology Roadmap for Semiconductors, 2011 Edition* (Process Integration, Devices, and Structures Chapter) which is available online at http://www.itrs.net/Links/2011ITRS/Home2011.htm

- Gate length L_G = 25 nm
- Effective oxide thickness T_{oxe} = 0.9 nm
- Gate work function = 4.28 eV (corresponding to aluminum)
- Deep source/drain regions:
  - Dopant concentration *vs*. depth profile is Gaussian
  - Peak dopant concentration = 2×10^{20} cm^{-3}
  - Junction depth (defined as the distance from the Si surface to the depth where the deep source/drain dopant concentration is equal to the body dopant concentration) = 25 nm
- Source/drain extension regions:
  - Dopant concentration *vs*. depth profile is Gaussian
  - Peak dopant concentration = 9×10^{19} cm^{-3}
- Power supply voltage V_{DD} = 0.9 V
- Body bias voltage V_B = 0 V.

Design Task

Your assignment is to co-optimize the channel/body dopant concentration N_A, SDE junction depth X_J, and spacer length L_{SP} to meet the following MOSFET performance specifications:

- $I_{OFF} \leq 100$ nA per micron channel width.
- $I_{ON} \geq 1.3$ mA per micron channel width.

with the following practical design constraints:

- 1×10^{15} cm$^{-3} \leq N_A \leq 3\times10^{18}$ cm^{-3}
- 15 nm $\leq L_{SP} \leq$ 30 nm
- 10 nm $\leq X_J \leq$ 15 nm

I_{ON} is defined to be I_{DS} for $V_{GS} = V_{DS} = V_{DD}$. I_{OFF} is defined to be I_{DS} for V_{GS} = 0 V & $V_{DS} = V_{DD}$.

Larger I_{ON} provides for faster (or higher frequency) circuit operation, while lower I_{OFF} provides for lower static power consumption; therefore, a high I_{ON}/I_{OFF} ratio is generally desirable. You should explore the trade-offs between I_{ON} and I_{OFF} by simulating the transfer characteristic (I_{DS} *vs*. V_{GS} curve) for different combinations of values for the three design parameters:

- Increasing N_A increases V_T and hence reduces I_{OFF} (unless N_A is so large that band-to-band tunneling at the drain junction becomes significant) but degrades the effective mobility and hence I_{ON}.
- Smaller X_J depth helps to reduce the short-channel effect and hence I_{OFF} but results in larger parasitic series resistance and hence degrades I_{ON}.
- Longer spacers help to reduce the influence of the deep source/drain regions on the channel region but result in larger parasitic series resistance.

Design Report [80 points]

For your finalized MOSFET design:

1. [10 pts] Illustrate your MOSFET design, labeling and indicating your values for the design parameters. Describe the process (in a paragraph) by which you arrived at your final design.

2. [20 pts] Run the I_{DS}-V_{GS} simulation for V_{DS} = 20 mV (corresponding to the linear region of operation) and for $V_{DS} = V_{DD}$ (corresponding to the saturation region of operation) and **plot the I_{DS}-V_{GS} curves for $0 \leq V_{GS} \leq V_{DD}$.** Manually extract the following performance parameters from the simulation outputs:
- Minimum subthreshold swing, S.
- Linear threshold voltage (V_{Tlin}), defined as the value of V_{GS} corresponding to I_{DS} = 100nA·W/L_G = 4 μA for $V_{DS} = V_{Dlin}$ = 20 mV.

  (Note that the saturation threshold voltage (V_{Tsat}), defined as the value of V_{GS} corresponding to I_{DS} = 100nA·W/L_G = 4 μA for $V_{DS} = V_{DD}$, is automatically extracted for you by the simulation package.)
- Drain-induced barrier lowering, in units of mV per Volt, defined as

$$DIBL = (|V_{Tlin}| - |V_{Tsat}|)/(V_{DD} - V_{Dlin})$$

Summarize your MOSFET design and performance parameters in tabular format:

N_A [cm^{-3}]	X_J [cm^{-3}]	L_{SP} [cm^{-3}]	I_{ON} [μA/μm]	I_{OFF} [μA/μm]	S [mV/dec]	DIBL [mV/V]
<designed value>	<designed value>	<designed value>	<simulated value>	<simulated value>	<simulated value>	<simulated value>

3. [20 pts] Run I_{DS}-V_{GS} simulations with $V_{DS} = V_{DD}$ (corresponding to the saturation region of operation), for gate length values ranging from 20 nm to 100 nm. Manually extract the saturation threshold voltage (V_{Tsat}) for each simulated curve and **plot V_{Tsat} *vs.* L_G for 20 nm ≤ L_G ≤ 100 nm** to see the short-channel effect.

4. [20 pts] Run I_{DS}-V_{DS} simulations for V_{GS} = 0.5 V, V_{GS} = 0.6 V, V_{GS} = 0.7 V, and V_{GS} = 0.8 V and **plot the I_{DS}-V_{DS} curves for $0 \leq V_{DS} \leq V_{DD}$**. Does your designed MOSFET exhibit a square-law dependence of saturation current on V_{GS}? **Explain briefly.**

5. [10 pts] Answer the following short-answer questions:

a. In an integrated circuit manufacturing process, there is always some statistical variation (*e.g.* ±10%) in the actual transistor parameters. Of the three design parameters explored in this project (X_J, L_{SP}, and N_A), which one causes the greatest process-induced variation in transistor performance? Why?

b. How would you expect I_{ON}, I_{OFF}, S, and V_T roll-off to change with increasing temperature (*e.g.* to 85^{o}C)?