EE130: Integrated Circuit Devices

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Web page: http://www-inst.eecs.berkeley.edu/~ee130/
Newsgroup: ucb.class.ee130

Schedule

- **Lectures** (289 Cory)**:** MWF 1-2 PM
- **Discussion Sections (beginning Friday 1/19):**
  - Section 101 (521 Cory): W 9-10 AM
  - Section 102 (531 Cory): F 2-3 PM
- **Office Hours:**
  - Prof. Liu (567 Cory): W 2-4PM
  - Frank Liao (382 Cory): M 9-10AM, Th 4-5PM
  - Alvaro Padilla (382 Cory): F 4-5PM

Relation to Other Courses

- **Prerequisite:**
  - EECS40: Simple *pn*-junction & MOSFET theory; MOSFET circuit applications
  - Familiarity with the Bohr atomic model
- **Relation to other courses:**
  - EE130 is a prerequisite for EE231 (Solid State Devices)
  - EE130 is also helpful (but not required) for IC analysis and design courses such as EE140 and EE141, as well as for the microfabrication technology course EE143

Reading Material

- **Textbook:**

  Semiconductor Device Fundamentals by R. F. Pierret (Addison Wesley, 1996)
- **References:**
  - *Solid State Electronic Devices* by B. G. Streetman & S. Banerjee (Prentice Hall, 2000)
  - *Fundamentals of Modern VLSI Devices* by Y. Taur & T. H. Ning (Cambridge University Press, 1998)

Grading

- **Homework** (posted online) — 10%
  - *due Mo (beginning of class)*
  - *late homeworks not accepted*
- **Design project** — 20%
  - *due on April 27th*
  - *You may work in pairs*
- **6 Quizzes** — 30%
  - *25 minutes each*
  - *closed book (1 page of notes allowed)*
  - *no make-up quizzes*
- **Final exam** — 40%
  - *Sa 5/12 from 12:30-3:30PM*
  - *closed book (6 pages of notes allowed)*
  - *bring calculator*

Letter grades will be assigned based approximately on the following scale:

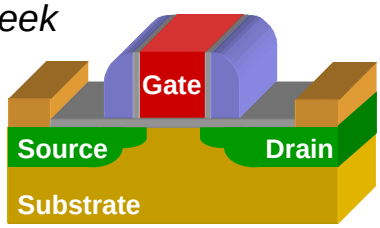
A+: 98-100
A: 88-98
A-: 85-88
B+: 83-85
B: 73-83
B-: 70-73
C+: 68-70
C: 58-68
C-: 55-58
D: 45-55
F: <45

Miscellany

- **Special accommodations:**
  - Students may request accommodation of religious creed, disabilities, and other special circumstances. Please make an appointment to discuss your request, in advance.
- **Academic (dis)honesty**
  - Departmental policy will be strictly followed
  - Collaboration (not cheating!) is encouraged
- **Classroom etiquette:**
  - Arrive in class on time!
  - Bring your own copy of the lecture notes.
  - Turn off cell phones, pagers, MP3 players, *etc*.
  - No distracting conversations
- **Weekly coffee hour** (beginning Wednesday 1/24):
  - 4PM Wednesdays at Brewed Awakenings (1807 Euclid Ave.)

Course Outline

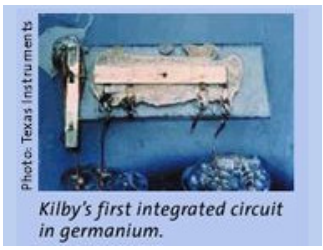
1. Semiconductor Fundamentals – *3 weeks*
2. Metal-Semiconductor Contacts – *1 week*
3. P-N Junction Diode – *3 weeks*
4. Bipolar Junction Transistor – *3 weeks*
5. MOS Capacitor – *1 week*
6. MOSFET – *4 weeks*

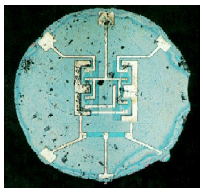


Introduction

The Integrated Circuit (IC)

- **An IC consists of interconnected electronic components in a single piece ("chip") of semiconductor material.**
  - **In 1958, Jack S. Kilby (*Texas Instruments*) showed that it was possible to fabricate a simple IC in germanium.**
  - **In 1959, Robert Noyce (*Fairchild Semiconductor*) demonstrated an IC made in silicon using SiO_2 as the insulator and Al for the metallic interconnects.**



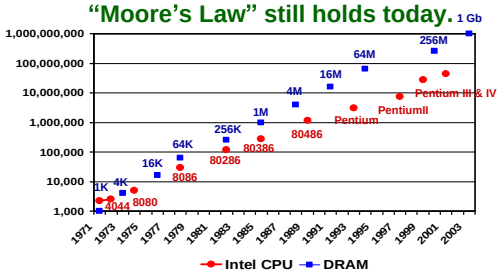


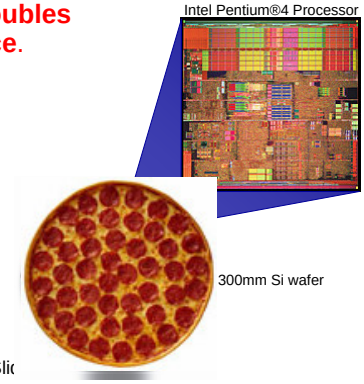
The first planar IC (actual size: 0.06 in. diameter)

From a Few, to Billions

- **By connecting a large number of components, each performing simple operations, an IC that performs very complex tasks can be built.**
- **The degree of integration has increased at an exponential pace over the past ~40 years.**
  - » **The number of devices on a chip doubles every ~18 months, for the same price.**

"Moore's Law" still holds today.





IC Technology Advancement

Improvements in IC performance and cost have been enabled by the steady miniaturization of the transistor

SMIC's Fab 4 (Beijing, China)
Photo by L.R. Huang, DigiTimes

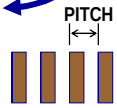
Transistor Scaling

Better Performance/Cost

Market Growth

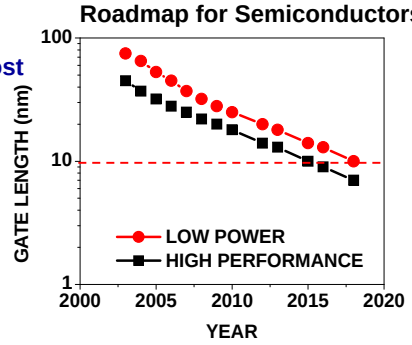
Investment

PITCH



YEAR:	2004	2007	2010	2013	2016
HALF-PITCH:	90nm	65nm	45nm	32nm	22nm

International Technology Roadmap for Semiconductors



The Nanometer Size Scale