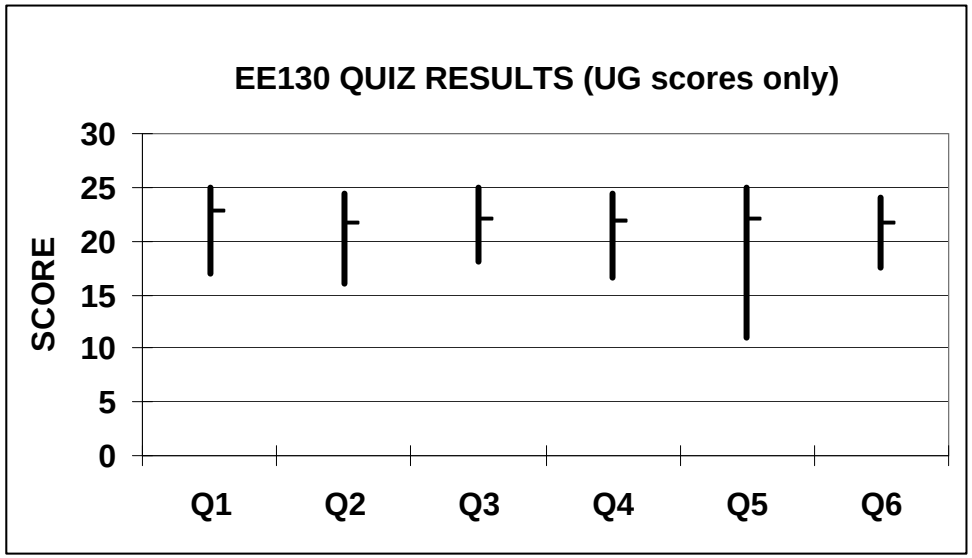
Announcements

- **A final review session will be offered on Thursday, May 10 from 10AM to 12noon in 521 Cory (the Hogan Room).**
- **The Final Exam will take place from 12:30PM to 3:30PM on Saturday May 12 in 60 Evans.**
  - **All of the material of the course will be covered (including HW#14)**
  - **Closed book, no calculators; 7 pages of notes allowed.**



Quiz 6 results:

- **Mean = 21.69**
- **Median = 22**
- **Std. Dev. = 1.779**
- **High = 24**
- **Low = 17.5**

MOSFET Scaling to the Limit … and Beyond

Prof. Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

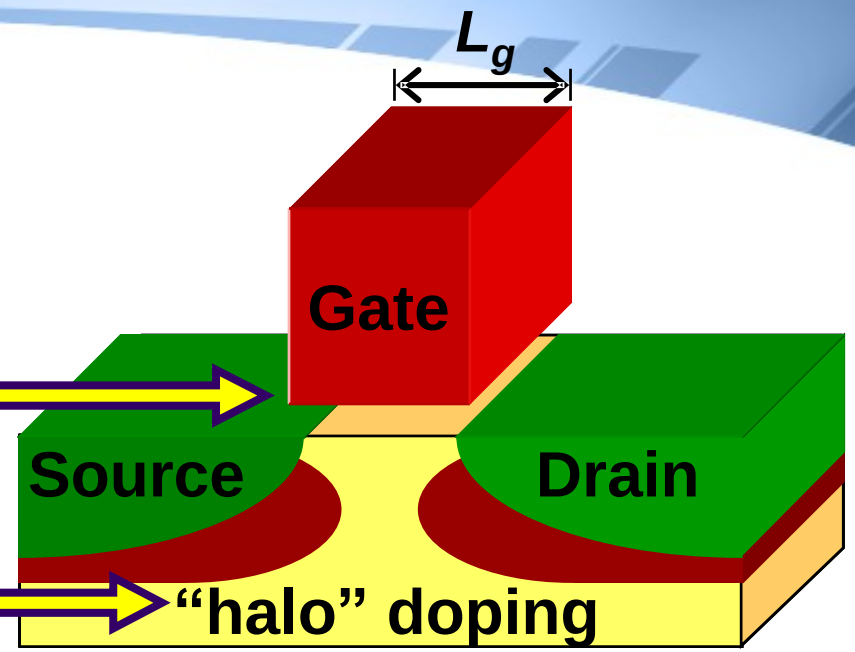
May 7, 2007

Transistor Scaling to the Limit

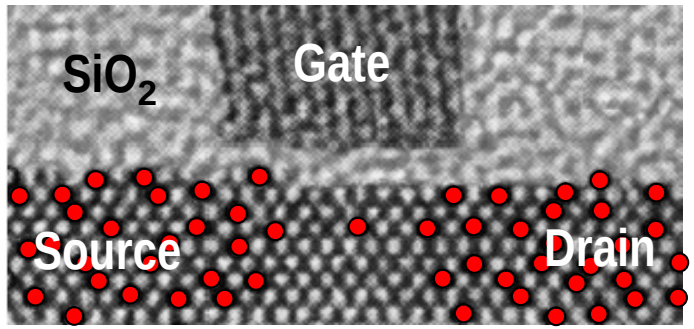
("More of Moore")

MOSFET Scaling Challenges

- **The traditional approach to transistor scaling is reaching fundamental limits**
  - » **Gate oxide scaling**
  - » **Shallow junctions**
  - » **Channel engineering**



- **Issues for scaling L_g to below 20 nm:**
  - » **Leakage**
  - » **Incommensurate gains in I_{Dsat}**
  - » **V_T variation**



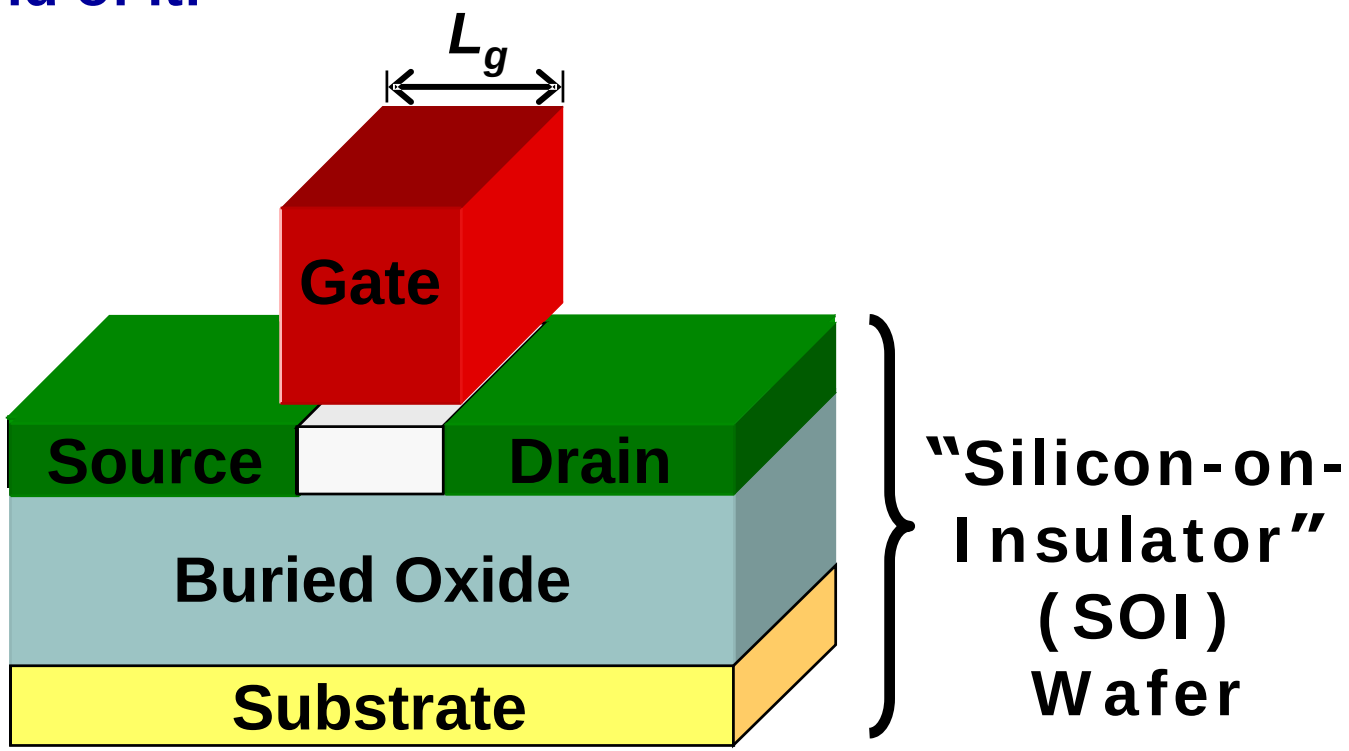
A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002

Why New Transistor Structures?

- Leakage must be suppressed to scale down L_g
- Leakage occurs in region far from channel surface

→ Let's get rid of it!

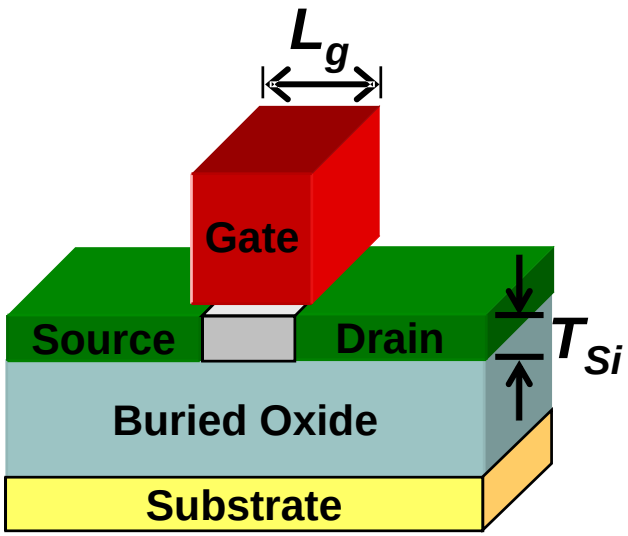
Thin-Body MOSFET



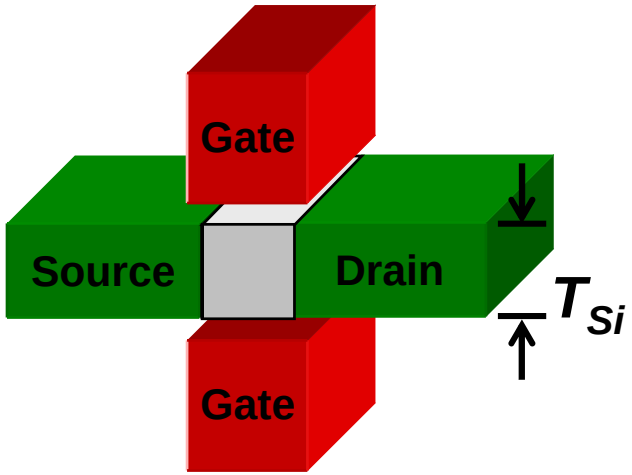
Thin-Body MOSFETs

- **Leakage is suppressed by using a thin body** ($T_{Si} < L_g$)
  - » **Channel doping is not needed → higher carrier mobility**
  - » **Aggressive gate-oxide scaling is not needed**
- **Double-gate structure is most scalable** (to L_g<10nm)

Ultra-Thin Body (UTB)

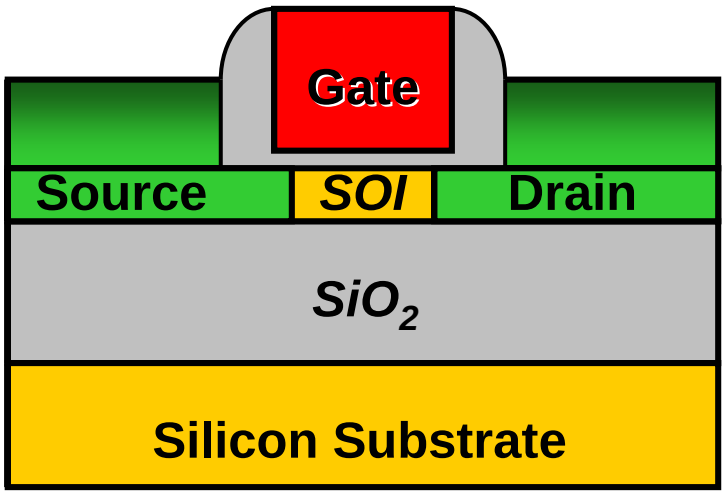


Double-Gate (DG)



Ultra-Thin-Body MOSFET

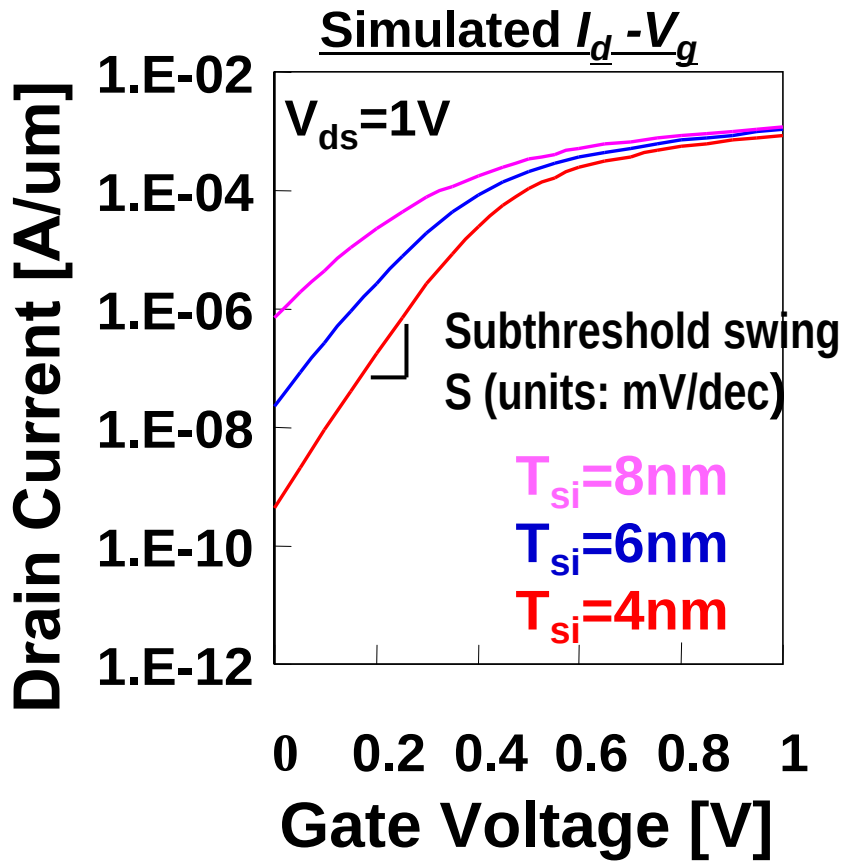
- UTB suppresses leakage
- Thick S/D => low R_{series}



M. Takamiya *et al.*, *Proc. 1997 ISDRS*, p. 215

B. Yu *et al.* (UC Berkeley), *Proc. 1997 ISDRS*, p. 623

- L_g = 12 nm
- T_{ox} = 2 nm



UTB MOSFET Scaling

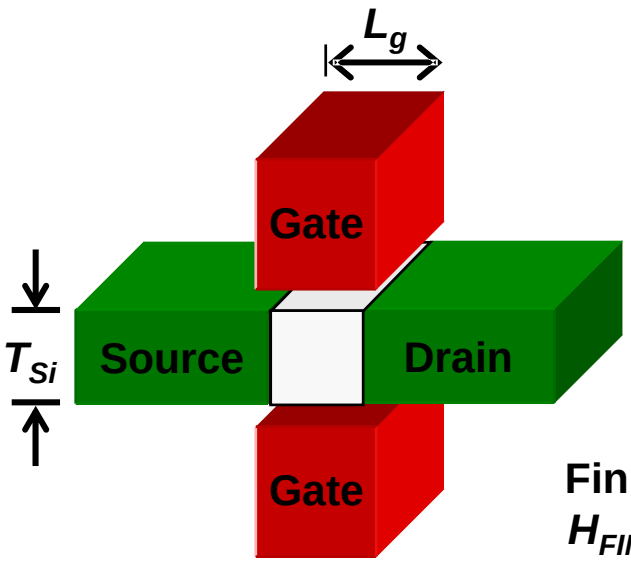
- **Issues for bulk-Si MOSFET scaling obviated**
  - » **Body does not need to be heavily doped**
  - » **T_{ox} does not need to be scaled as aggressively**
  - » **Ultra-shallow S/D junction formation is not an issue**

- **Body thickness must be less than ~1/3 x L_g**
  - » **Formation of uniformly thin body is primary challenge**
  - » **For T_{Si} < 4 nm, quantum confinement & interface roughness → V_T variation and degraded g_m**

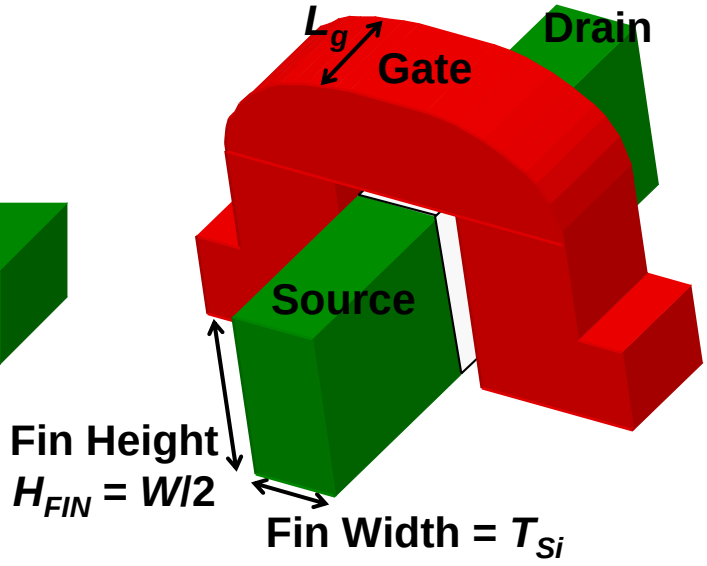
K. Uchida *et al.*, *IEDM Technical Digest*, pp. 47-50, 2002

Double-Gate "FinFET"

Planar DG-FET



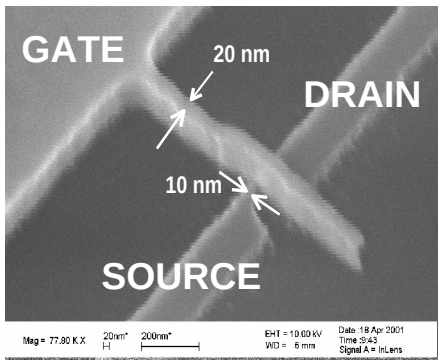
FinFET



D. Hisamoto *et al.* (UC Berkeley), *IEDM Technical Digest*, pp. 1032-1034, 1998

N. Lindert *et al*. (UC Berkeley), *IEEE Electron Device Letters*, pp. 487-489, 2001

15nm L_g FinFET:



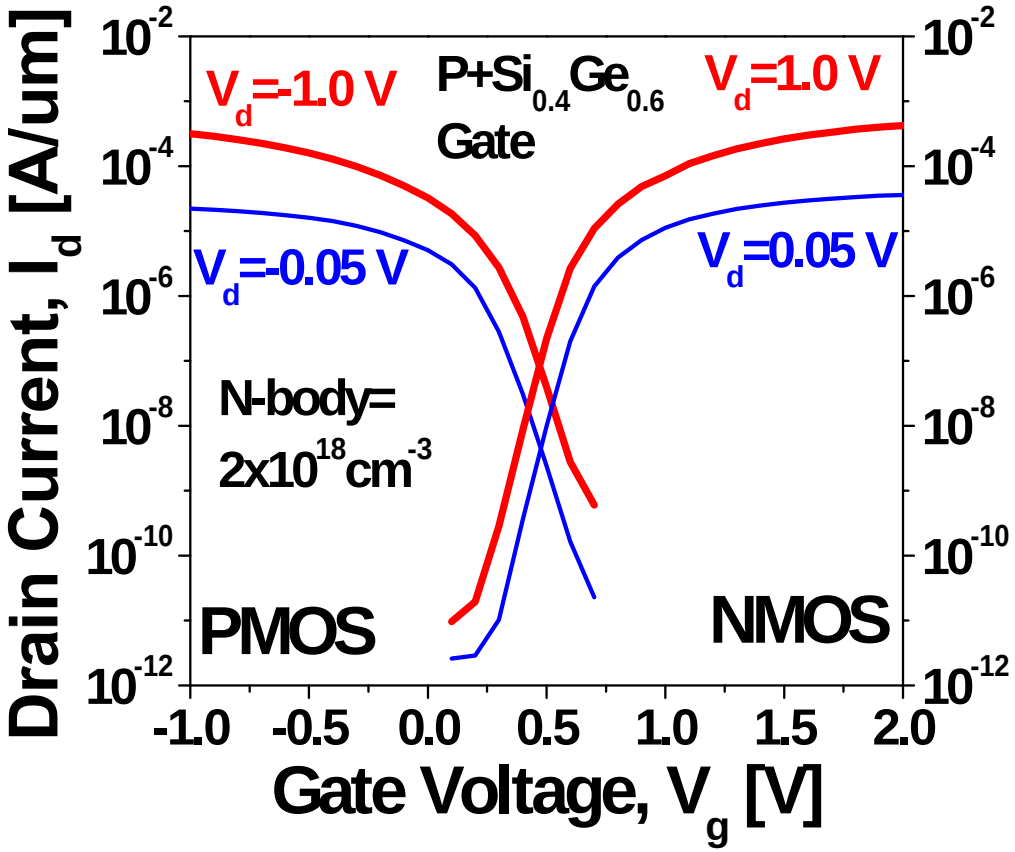
Y.-K. Choi *et al*. (UC Berkeley), *IEDM Technical Digest, pp. 421-424*, 2001

15 nm L_g FinFETs

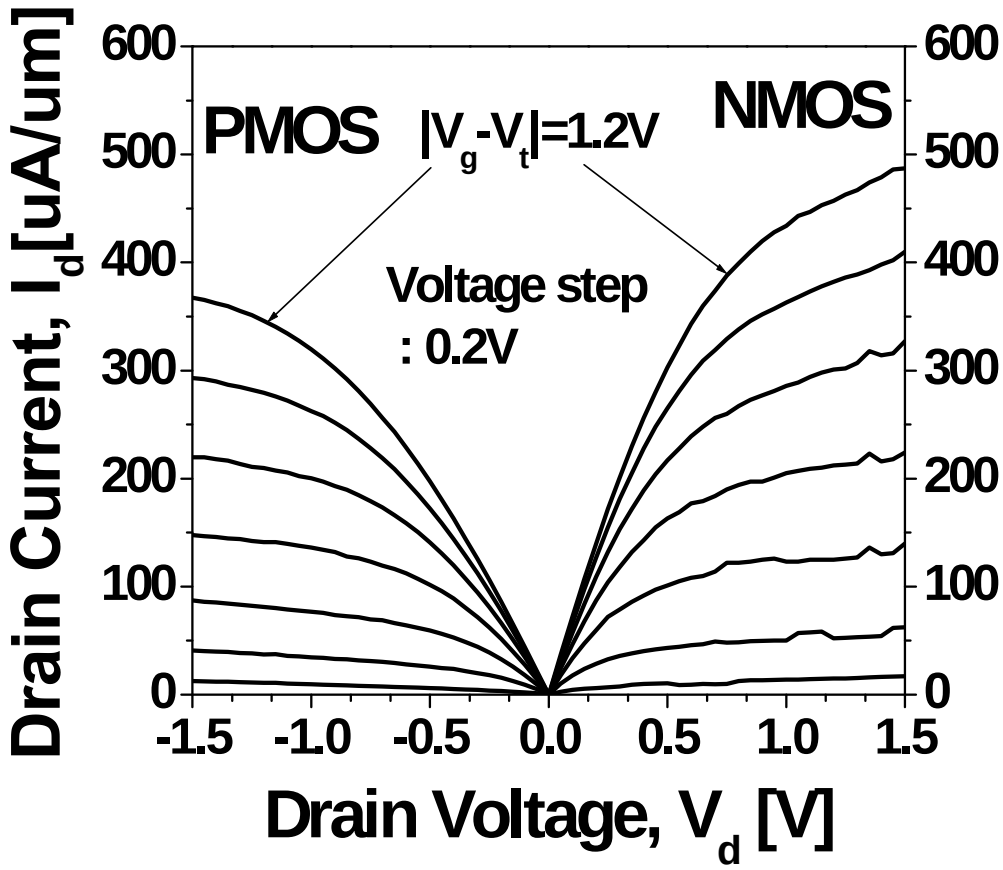
Y.-K. Choi *et al*. (UC Berkeley), *IEDM Technical Digest*, pp. 421-424, 2001

T_{Si} = 10 nm; T_{ox} = 2.1 nm

Transfer Characteristics

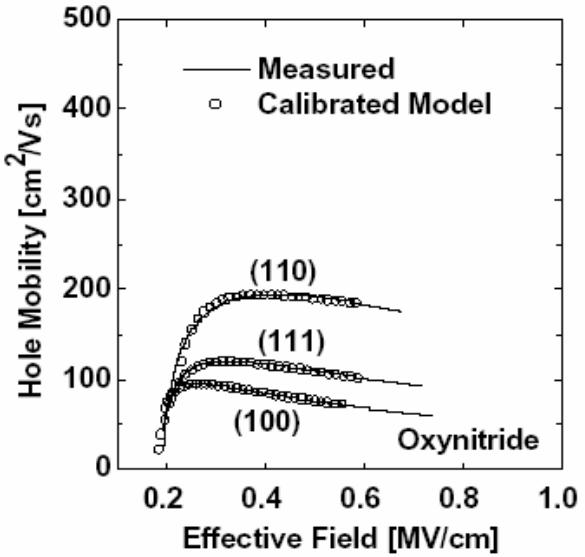


Output Characteristics

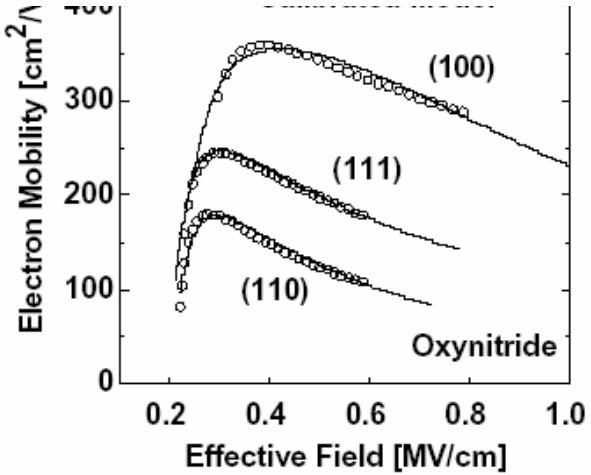


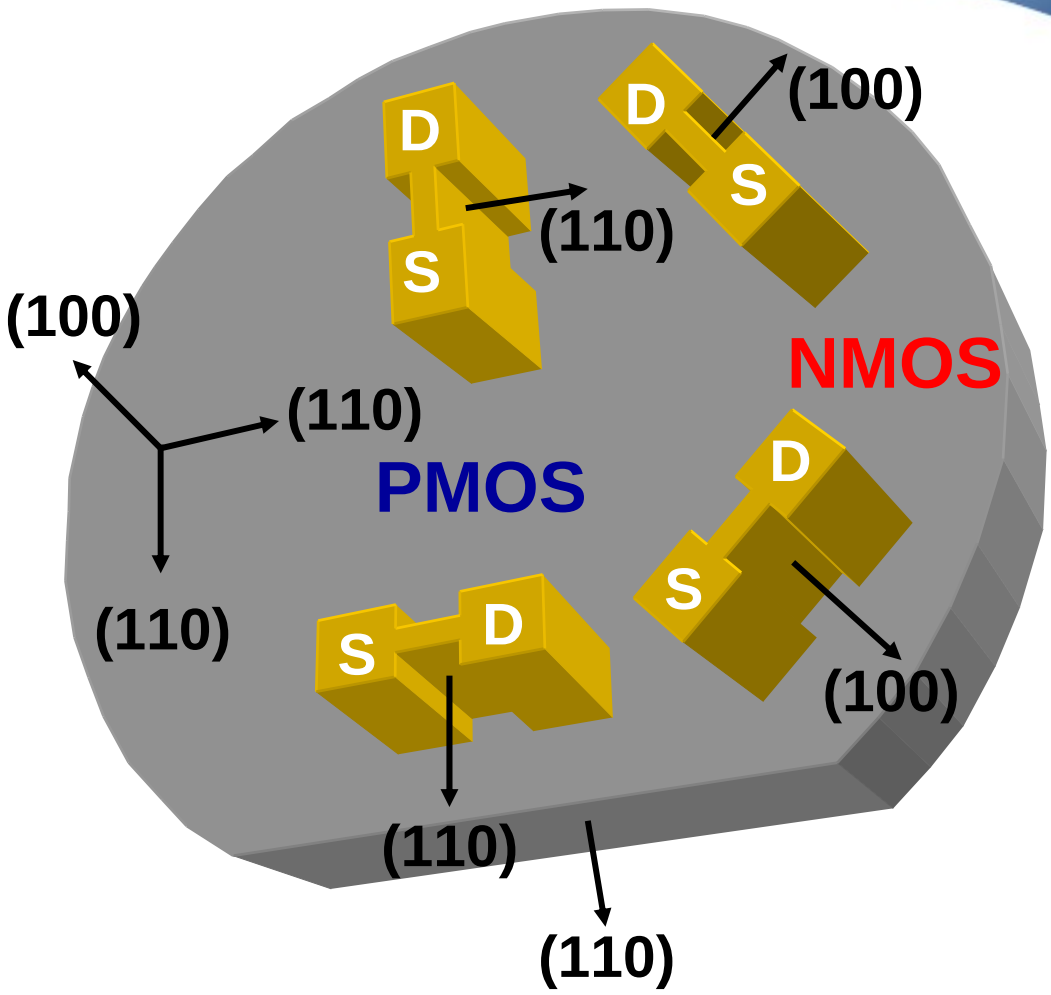
Impact of FinFET Orientation

Hole Mobility



Electron Mobility

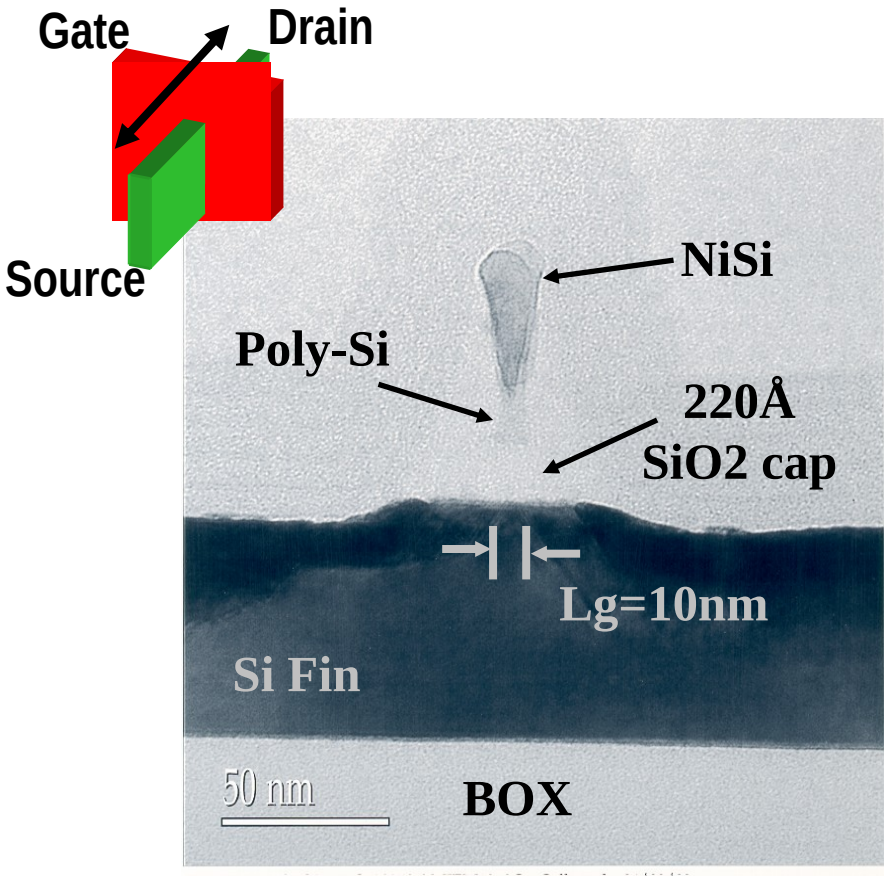




L. Chang *et al.*, *IEEE Trans. Electron Devices*, Vol. 51, p. 1621, 2004

10 nm L_g FinFETs

B. Yu *et al*. (AMD & UC Berkeley), *IEDM Technical Digest*, pp. 251-254, 2002



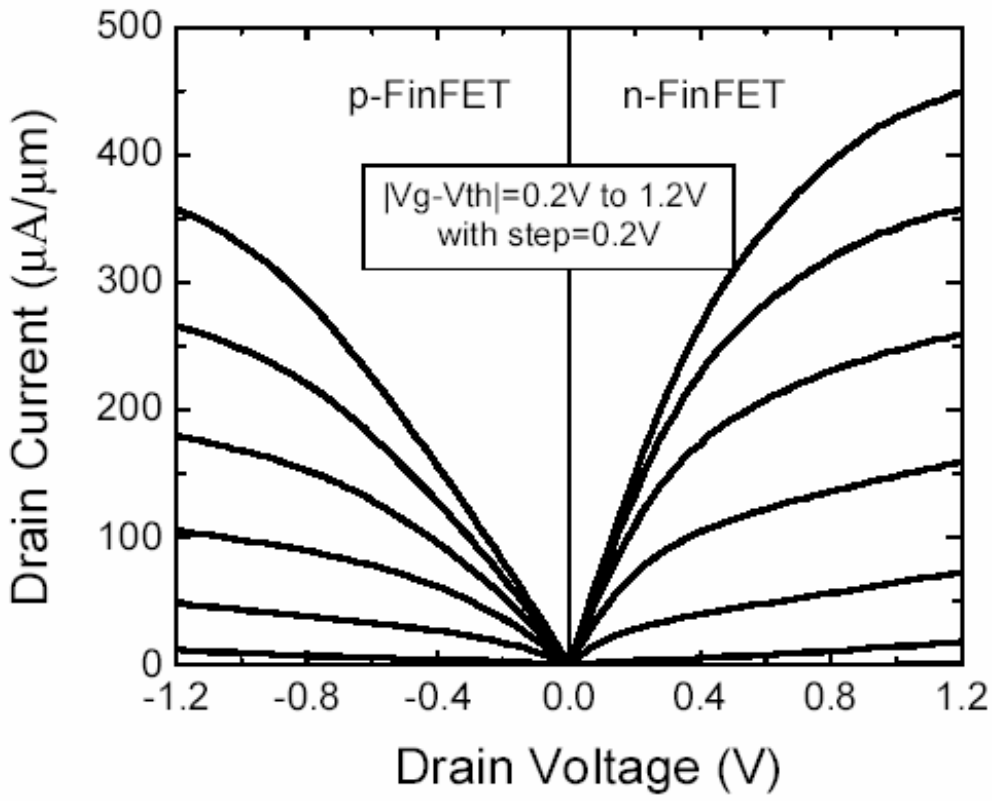


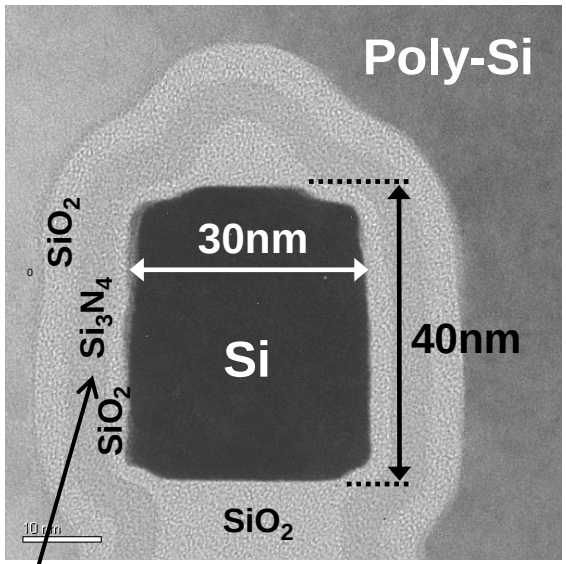
Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

FinFET Flash Memory Cell

P. Xuan *et al.* (UC Berkeley), *IEDM Technical Digest*, pp. 609-612, 2003

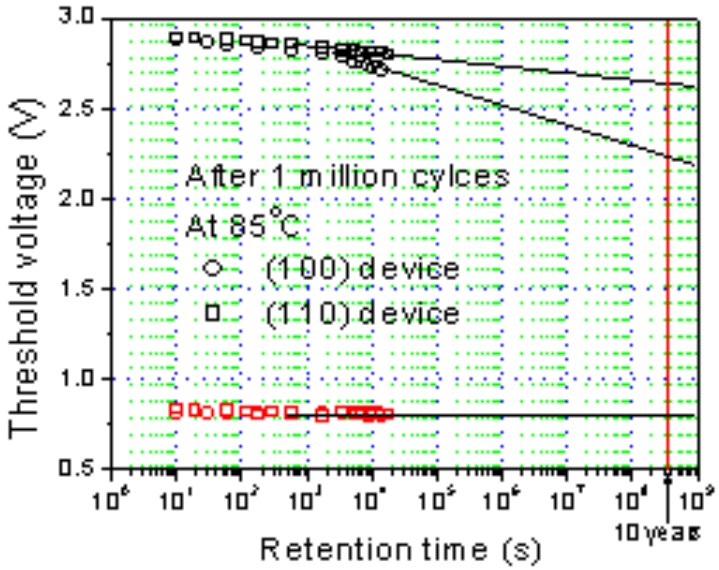
- **The FinFET is attractive for high-density flash memory**

FinFET SONOS Device Cross-Section

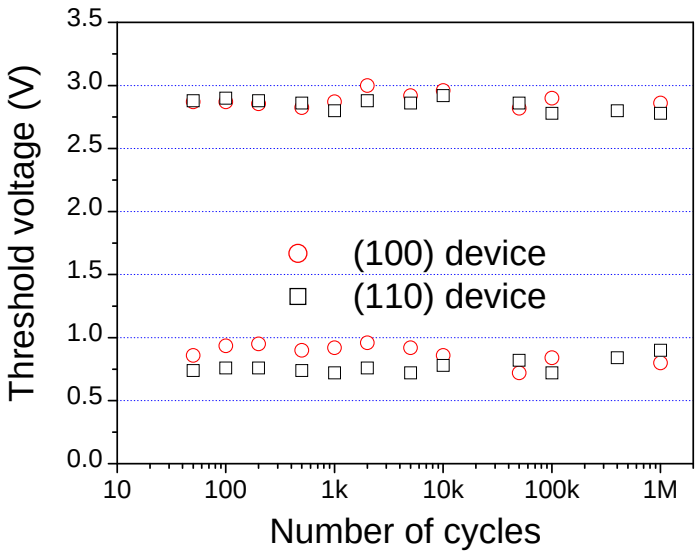


charge-storage layer

Measured Retention Characteristics



Measured Endurance Behavior



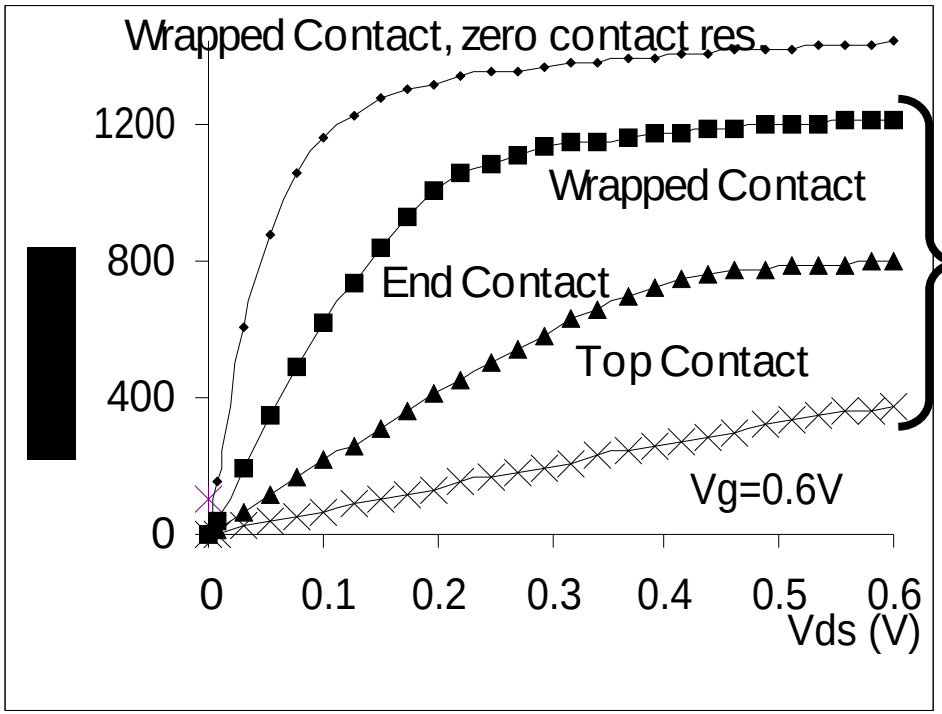
Subsequent publications:

- M. Specht *et al*. (Infineon Technologies), *IEDM* 2004
- C. W. Oh *et al*. (Samsung Electronics), *IEDM* 2004
- E. S. Cho *et al*. (Samsung Electronics), *Symp. VLSI Technology* 2005

Impact of S/D Contact Structure

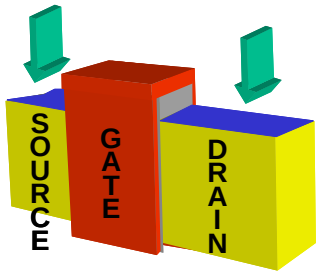
H. Kam and T.-J. King, *Proc. 2004 Silicon Nanoelectronics Workshop*, pp. 9-10

L_g=18nm, L_{eff} = 20nm, W_{fin}=10nm, T_{ox}=5A

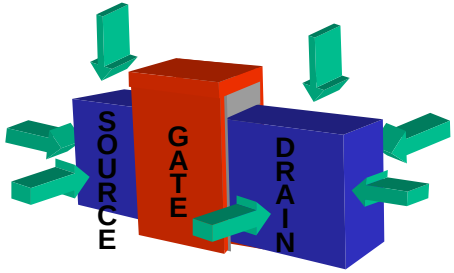


$\rho_c = 10^{-8}\ \Omega\text{-cm}^2$

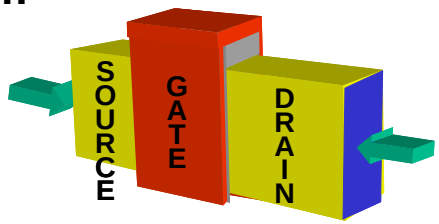
Top Contact



Wrapped Contact

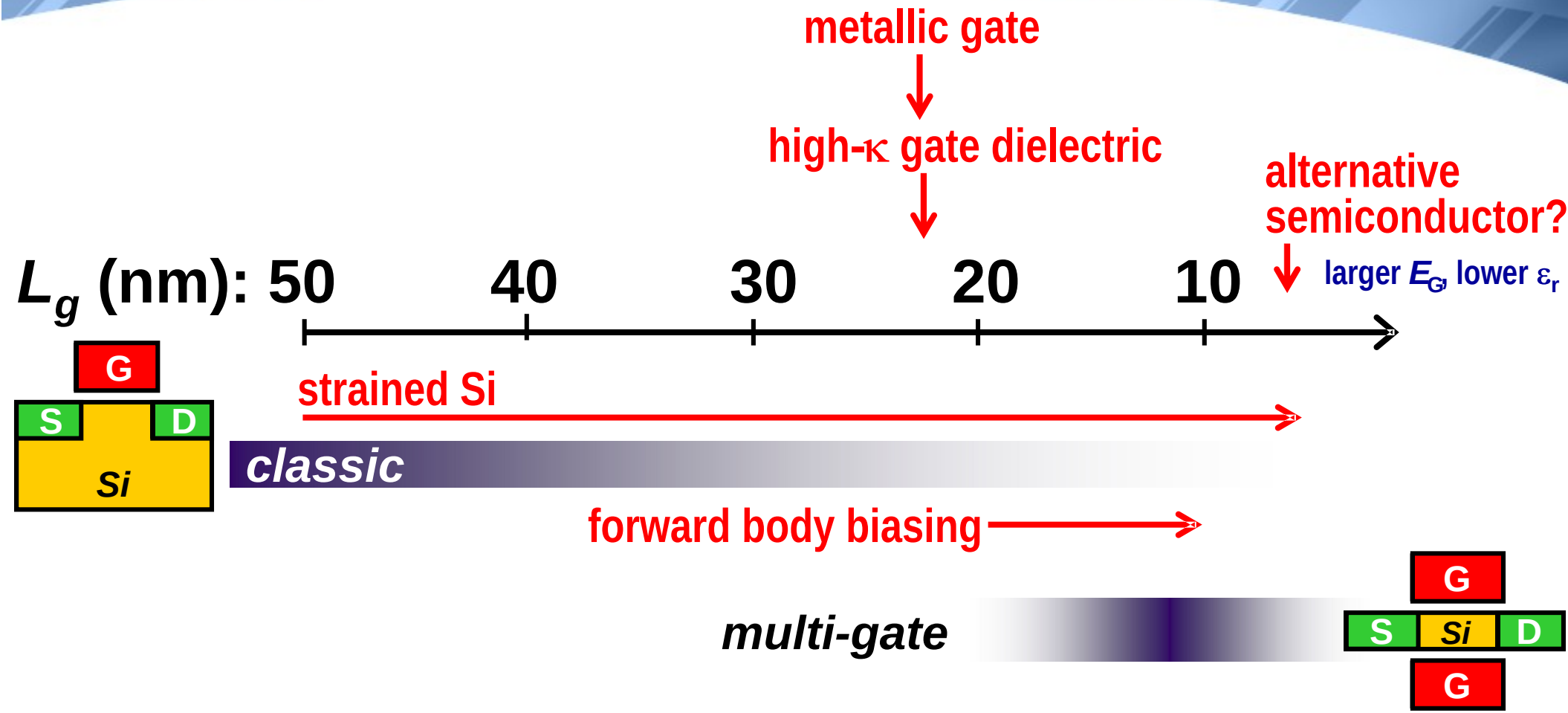


End Contact



Parasitic resistance (& capacitance) will limit the performance of nanoscale CMOS → Better FET designs are needed!

MOSFET Scaling Scenario



- Advanced structures will enable Si FET scaling to L_g <10 nm
  - » Minimization of parasitics will become the primary challenge

Channel-Length Scaling Limit

J. Wang *et al.*, *IEDM Technical Digest*, pp. 707-710, 2002

- **Quantum mechanical tunneling sets a fundamental scaling limit for the channel length *L*, to ~5 nm.**

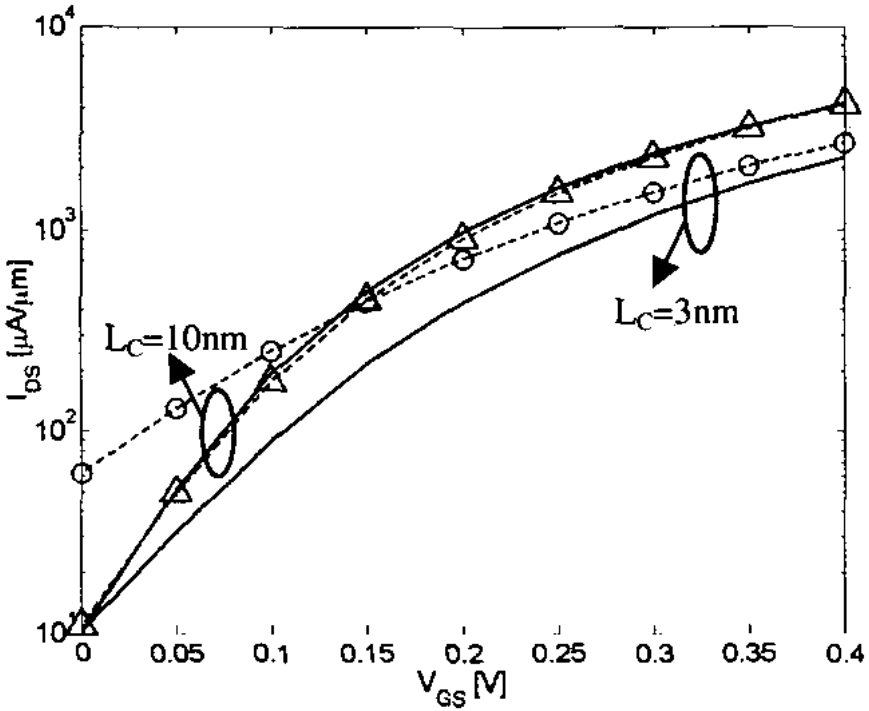
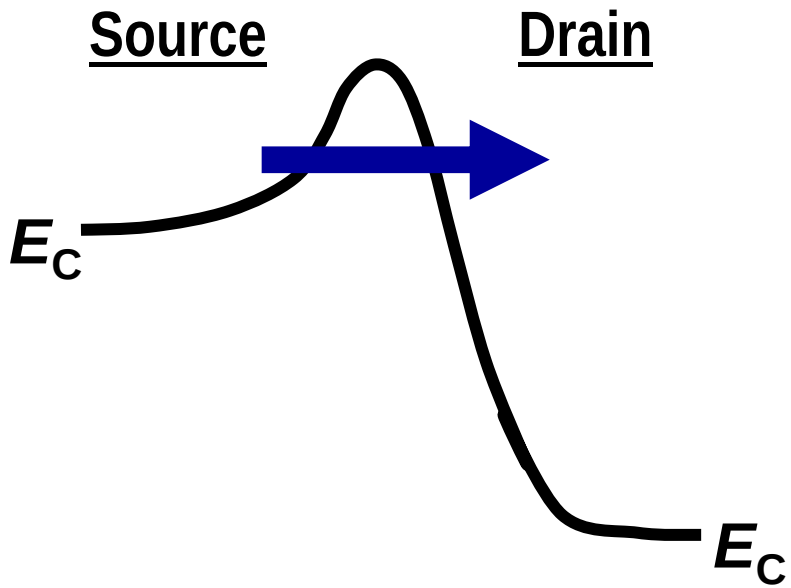


Fig. 2 I_{DS} *vs.* V_{GS} for the DG MOSFETs with 1nm body thickness and two different channel lengths (L_C=3nm and 10nm). (V_{DS}=V_{DD}=0.4V) The simulation is based on the classical (solid lines) and quantum (dashed lines: circle for L_C=3nm, and triangle for L_C=10nm) ballistic transport models. Different gate work functions are used to achieve the same off-current value (10 μA/μm) for each channel length (classical simulation). It can be clearly seen that the S/D tunneling effect does not significantly affect the current characteristics at 10nm channel length but it really does at 3nm channel length.

If electrons can easily tunnel through the source-to-channel potential barrier, the gate cannot shut off the transistor.

NMOSFET Band Diagram

(OFF state)



Beyond Transistor Scaling

("More than Moore")

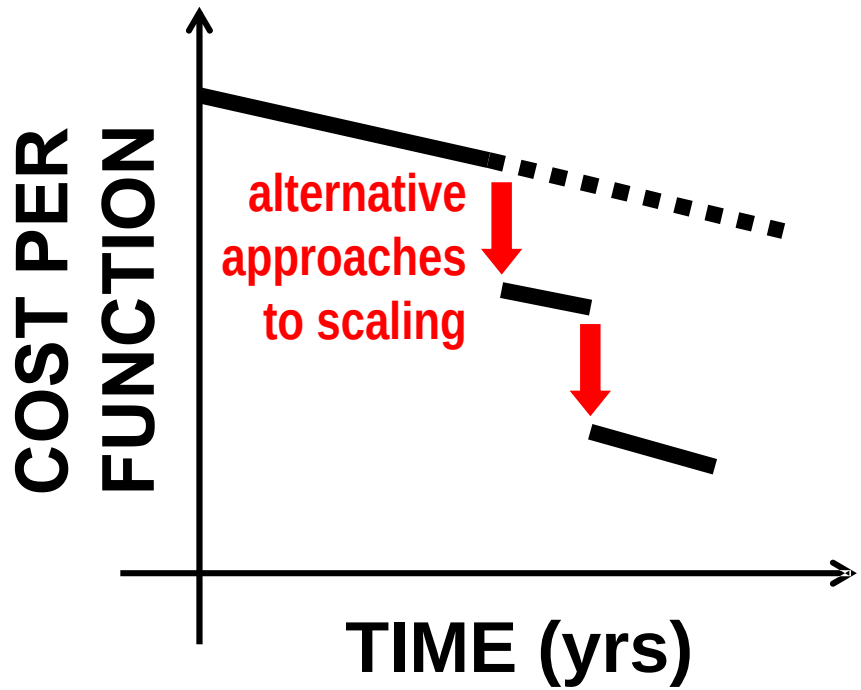
Off the Roadmap…

- **Alternative approaches to**
  - » **enhance performance and/or functionality**
  - » **lower power consumption per function**

can help to reduce cost per function

- ➢ **innovative circuit & system design**
- ➢ **novel semiconductor devices**
- ➢ **3-D & heterogeneous integration**

e.g. with micro-electro-mechanical devices (MEMS), microfluidics…

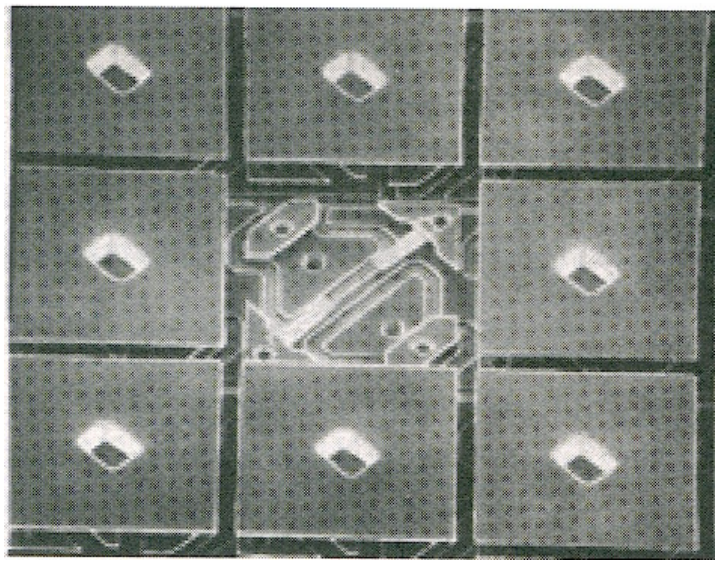


DMD™ Projection Display Chip

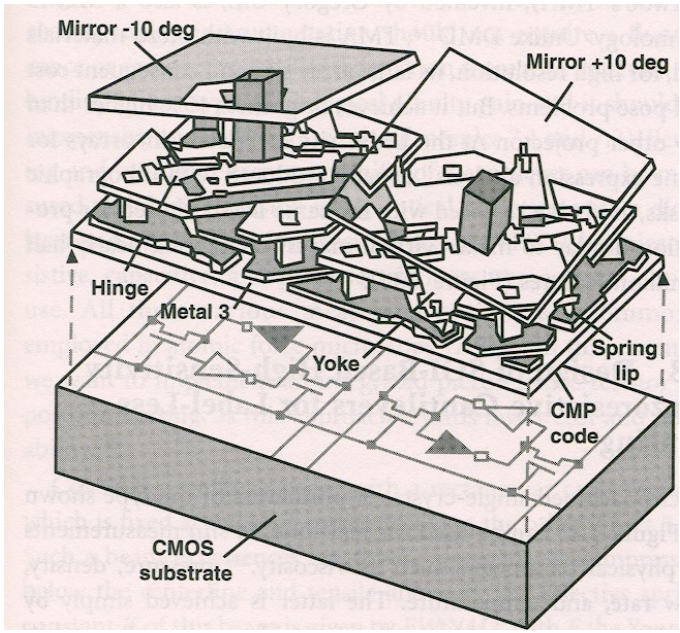
Texas Instruments Inc.

- **Mirrors are made using layers of metals (Al alloys) deposited on top of CMOS circuitry**

SEM image of pixel array

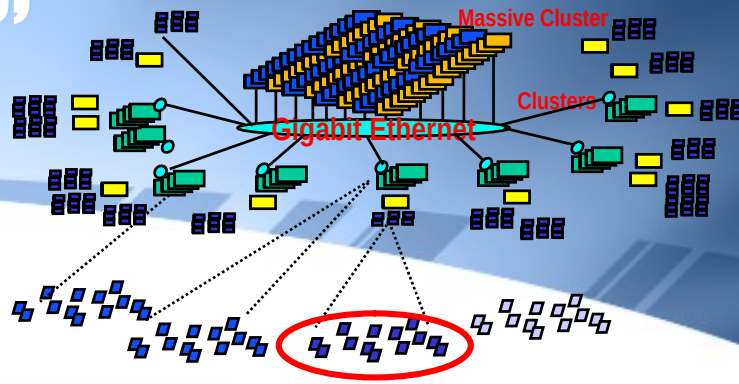


Schematic of 2 pixels



Each mirror corresponds to a single pixel, programmed by an underlying memory cell to deflect light either into a projection lens or a light absorber.

Enabling "Radio on a Chip"



wireless sensor network

Integration trend for mobile phones

- dual band
- >200 L-R-Cs
- 10 ICs
- 4 RF-filters
- 1 IF-filter

- triple band
- 100 L-R-Cs
- 3 ICs
- 3 RF-filters
- no IF-filter

- quad band
- 30 L-R-Cs
- 2 ICs
- 4 RF-filters

- quad band + UMTS
- 20 L-R-Cs
- 1 IC
- 6 RF-filters

MEMS - enabled single-chip radio

1999 2003 2006 2008 2010

courtesy of Robert Aigner (Infineon Technologies)

- **Advantages of MEMS RF filters:**
  - small size
  - low power
  - low phase noise
  - high Q
- **Timing reference can also be implemented on-chip with MEMS**

Droplet Transport by Electrowetting

http://www.ee.duke.edu/research/microfluidics/

- An electric field modifies the wetting behavior of a liquid droplet on a surface, by reducing interfacial energy

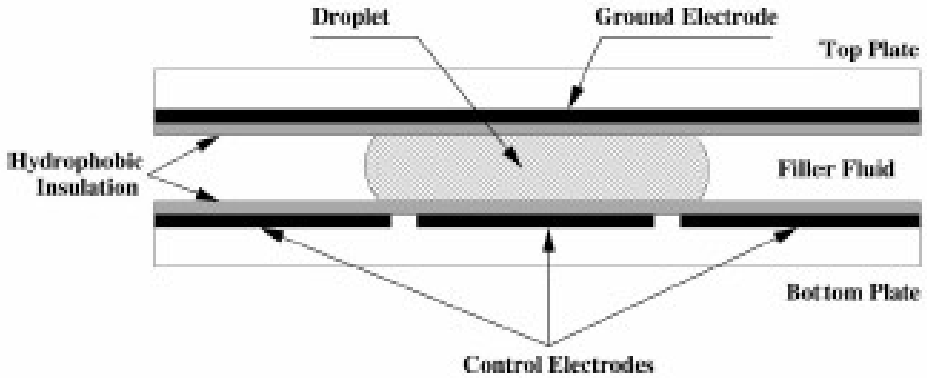


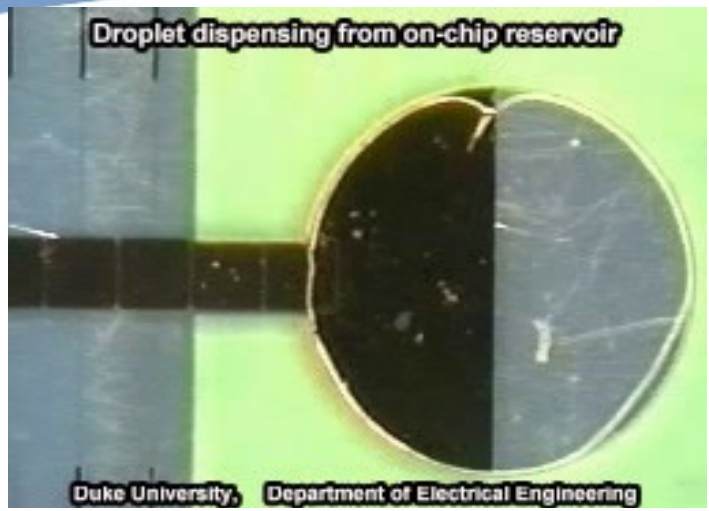
FIG. 1. Schematic cross-section of the electrowetting microactuator.

- The electric field can be induced by applying a voltage across 2 electrodes sandwiching the droplet

- If an electric field is applied non-uniformly, then a surface-energy gradient is created, which causes the droplet to move

Digital Microfluidic Processing

R. B. Fair *et al.*, *IEDM Technical Digest*, pp. 779-782, 2003



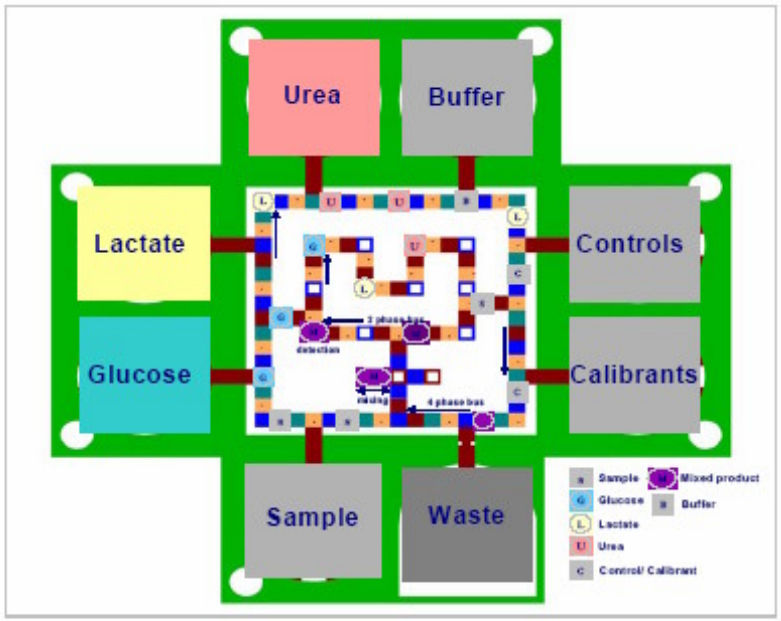


Fig. 9. Multiplexed assay μTAS with on-chip sample processing and 4-phase bus clocking.

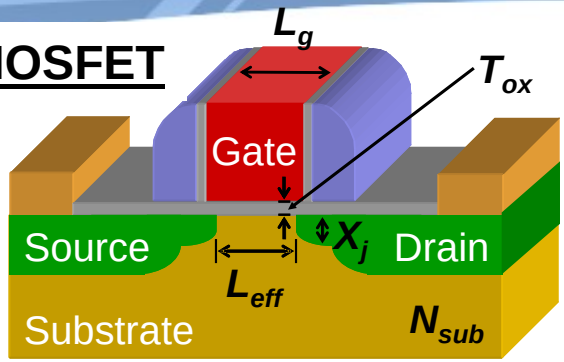
- **Multiple control electrodes can be used to manipulate droplets across a surface under direct electrical control**
  - » **No pumps, valves, channels needed**
  - » **Units of fluid can be transported, stored, mixed, reacted, or analyzed using a sequence of electrode voltage combinations.**

→ **Electrowetting arrays are promising for highly integrated and automated "lab-on-a-chip" systems!**

Summary

Silicon as the Electronics Platform

Bulk-Si MOSFET

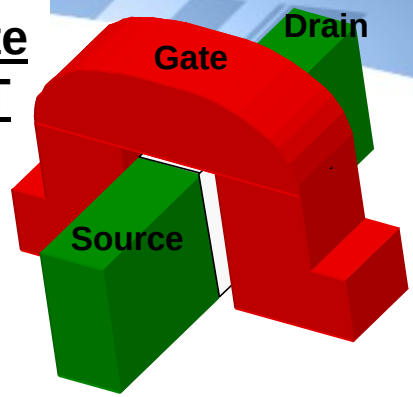


(~1970 to present)

scaling to L_g < 20 nm

(beyond 2010)

Multi-Gate MOSFET



- **CMOS scaling will continue with advances in**
  - » **transistor design**
  - » **fabrication techniques**
  - » **materials**

- **Opportunities remain for innovations to**
  - » **reduce power per function** (*e.g.* novel devices)
  - » **lower system cost** (*e.g.* integrated system on chip)
  - » **increase system functionality**

(*e.g.* heterogeneous integration of III-V devices, M/NEMS, CNTs, molecular devices, *etc.*)