On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years.

A new 3-dimensional transistor design will enable the production of integrated-circuit chips that operate faster with less power…

THE WALL STREET JOURNAL. * * * * Thursday, May 5, 2011

CORPORATE NEWS

Intel Rethinks Chip's Building Blocks

By Don Clark

Intel Corp. showed off what it called the most radical shift in semiconductor technology in more than fifty years, a design that could produce more powerful chips for gadgets without taxing their batteries.

The company plans to change a key part of each chip into a vertical, fin-like structure, a similar principle to the way high-rise buildings pack more office space in a city. The parts being changed—transistors—are the building block of nearly all electronic products; today's microchips can contain billions of the tiny switching elements.

Intel said its latest technology could bring more computing power to smartphones and tablet computers as well as speed up corporate data centers—all while sharply reducing power consumption.

Though rivals also have been exploring similar technologies, Intel is the first to commit to using the so-called 3-D approach in high-volume production, a gamble that analysts said could help Intel match the performance advantages of rivals that have largely kept Intel's chips out of the smartphone market.

"We've been talking about these 3-D circuits for more than 10 years, but no one has had the confidence to move them into manufacturing," said Dan Hutcheson, a chip-manufacturing specialist with the firm VLSI Research.

Intel executives demonstrated working chips based on the new approach at a gathering Wednesday in San Francisco. They indicated the first microprocessors would likely be targeted for high-end desktop computers and server systems and arrive in early 2012.

For decades, chip manufacturers have raced to shrink the size of components, which increases the performance of chips while decreasing the cost of each computing function. Competition has spurred companies to introduce ever-smaller processes every couple of years.

Intel executives say the shift to 3-D transistors brings more benefits than simply moving to a new generation of manufacturing technology. For example, if designers keep performance consumption constant, the new technology consumes half the power as Intel's existing production method.

"That is an unprecedented gain," said Mark Bohr, who holds the title of Intel fellow and leads its development of new manufacturing processes. "We've never achieved that kind of performance gain at low voltage."

Chip designers have long worked in more than two dimensions, with transistors topped by layers of interconnecting wiring. Intel's shift relates to a part of each transistor that determines how fast electricity flows and how much current may leak out, affecting power consumption.

Intel engineers replaced a flat channel for conducting electrons with a fin-shaped structure surrounded on three sides by a device called a gate that turns the flow on and off. The three-dimensional shape, Mr. Bohr said, lets more current flow during the "on" state and less current to leak when the transistor is switched "off."

Intel disclosed the underlying approach in research papers in 2002, and has spent the intervening years perfecting it. It has opted to shift completely to the new transistors for its next manufacturing process—slated to create chips with circuit dimensions measured at 22 nanometers, or billionths of a meter. Intel's current chips use 32-nanometer technology.

Departures from conventional manufacturing technologies tend to increase costs, and chip companies try to avoid them. Mr. Bohr said Intel concluded it could move to the new technology with a 2% to 3% increase in the cost of a finished silicon wafer, each of which contains hundreds of chips.

Others are expected to use the approach at some point, too, but not until they have shrunk their circuitry beyond 22 nanometers.

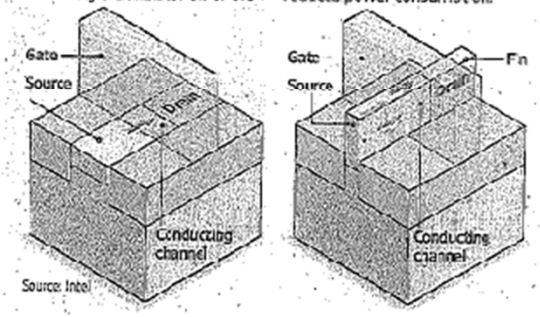
Globalfoundries, a production service spun off from Advanced Micro Devices Inc., said Wednesday it will use conventional transistors for its forthcoming 20-nanometer process. "We don't see the need" for technologies like 3-D transistors until subsequent production processes, a spokesman said.

Intel's Move Into 3-D

The chip maker breaks from conventional approaches to make transistors.

Conventional transistor: Electrons flow between components called a source and a drain, forming a two-dimensional conducting channel. A component called a gate starts and stops the flow, switching a transistor on or off.

Intel's new transistor: A fin-like structure rises above the surface of the transistor with the gate wrapped around it, forming conducting channels on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.



The 3-D Tri-Gate transistor is a variant of the FinFET developed at UC-Berkeley, and is being used in Intel's 22nm-generation microprocessors.

Lecture 28

OUTLINE

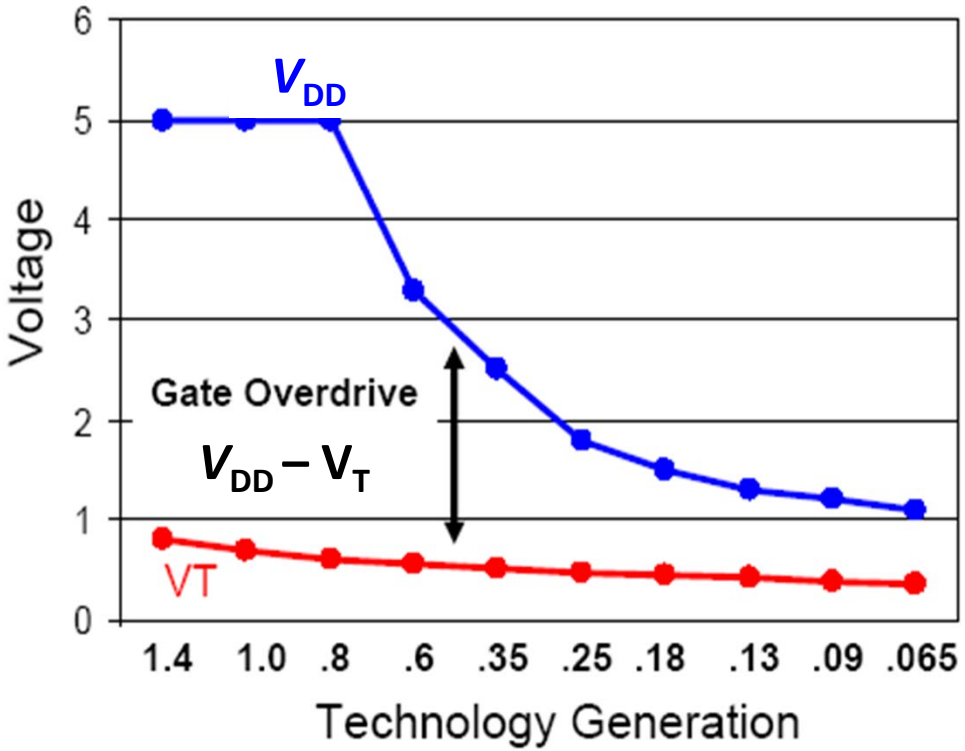
CMOS Technology Advancement

- The CMOS power crisis
- Advanced MOSFET structures
  - Thin-body MOSFET structures
  - History and future of multi-gate MOSFETs

Reading: Hu 7.8

Historical Voltage Scaling

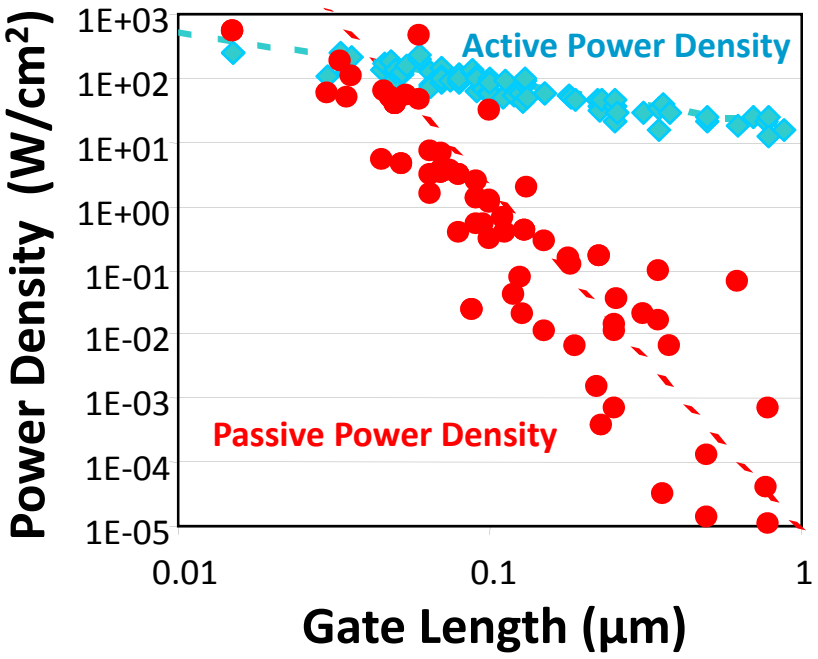
- **Since V_T cannot be scaled down aggressively, the supply voltage (V_{DD}) has not been scaled down in proportion to the MOSFET gate length:**



Source: P. Packan (Intel), 2007 IEDM Short Course

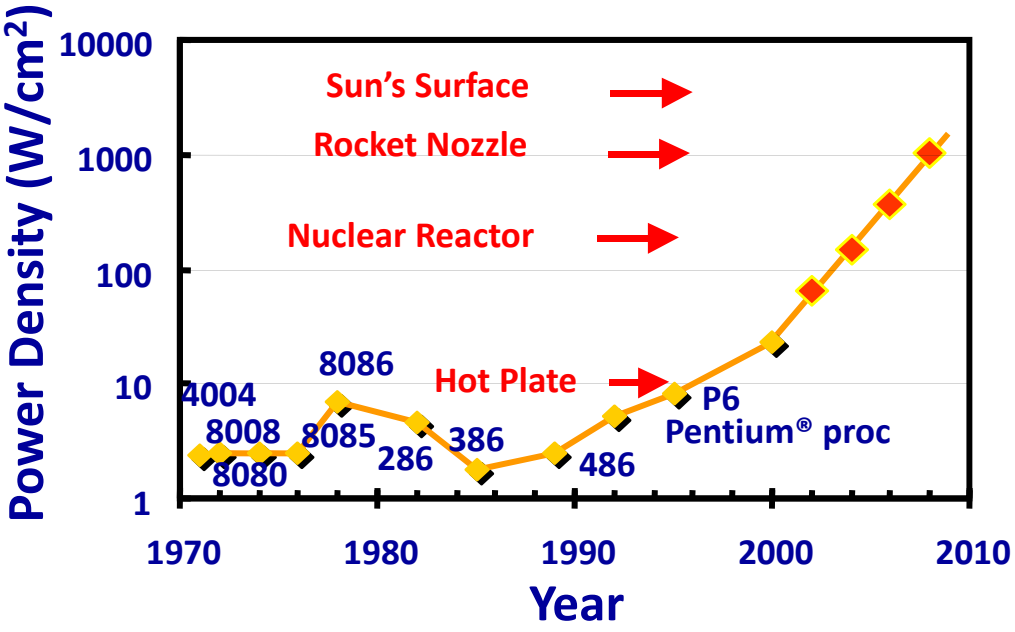
Power Density Scaling – NOT!

Power Density Trend



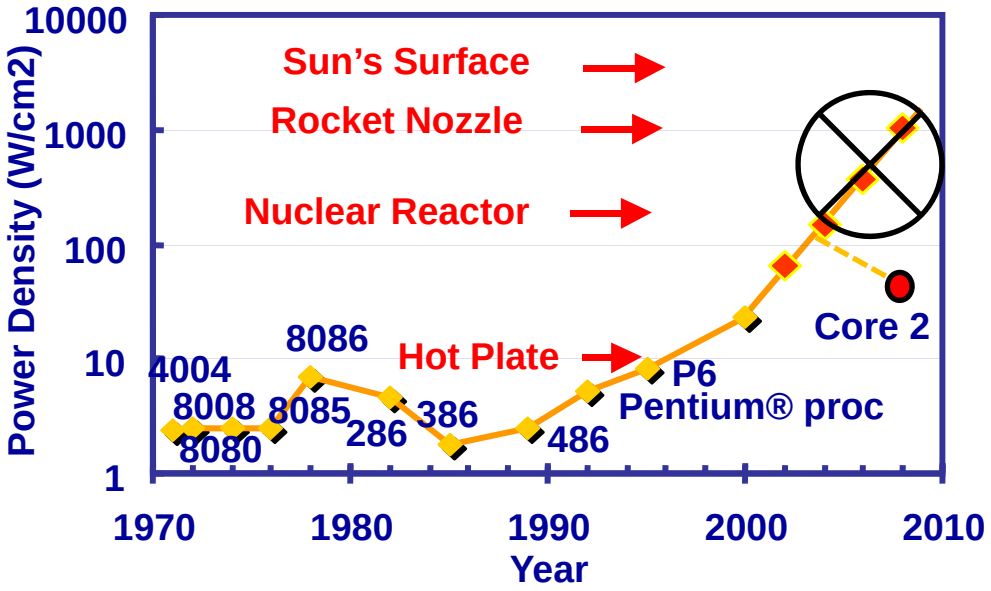
Source: B. Meyerson (IBM) Semico Conf., January 2004

Power Density Prediction circa 2000

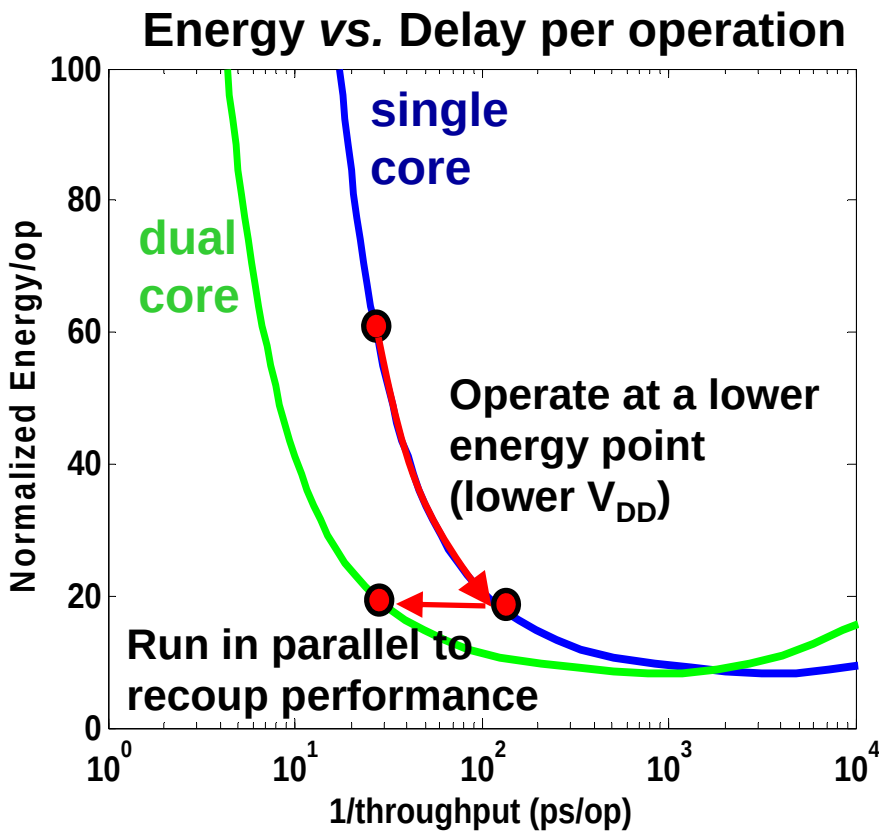


Source: S. Borkar (Intel)

Parallelism



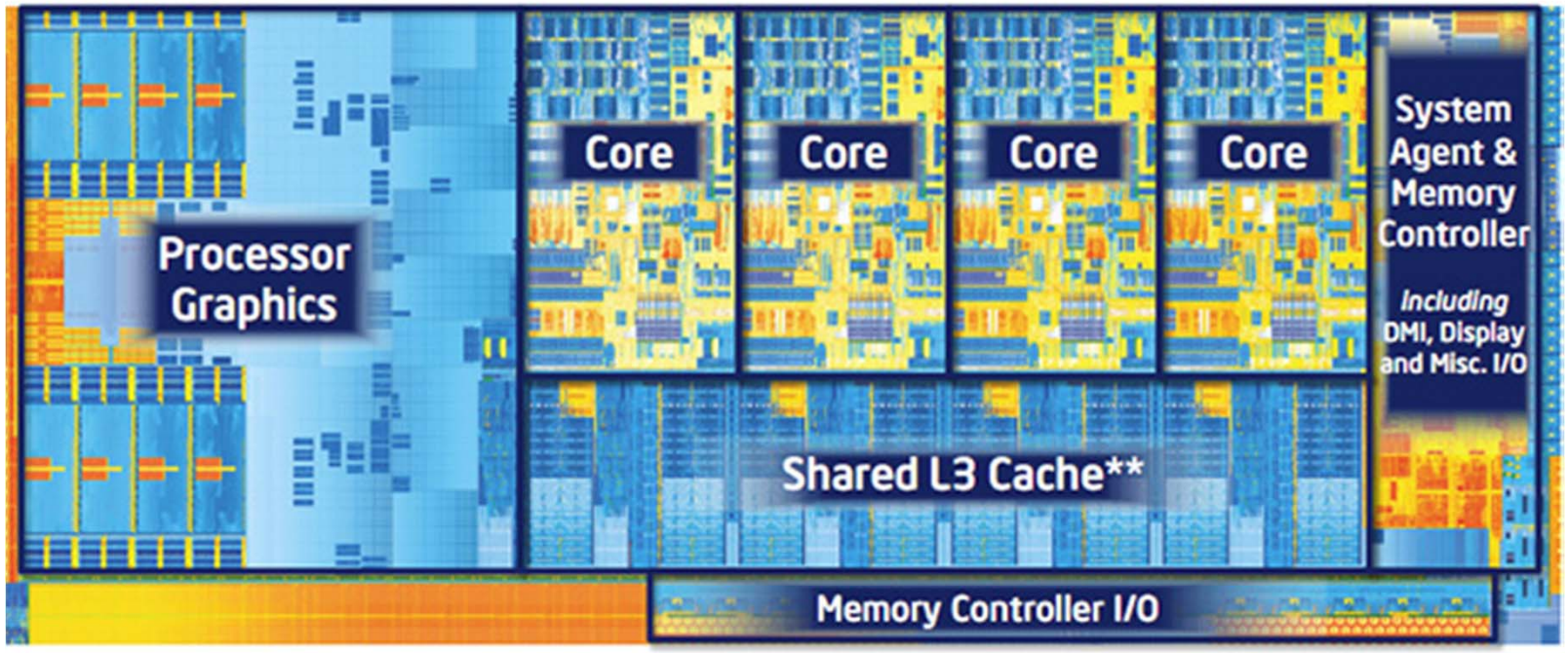
Source: S. Borkar (Intel)



- **Computing performance is now limited by power dissipation. This has forced the move to parallelism as the principal means of increasing system performance.**

Intel Ivy Bridge Processor

3rd Generation Intel® Core™ Processor: 22nm Process



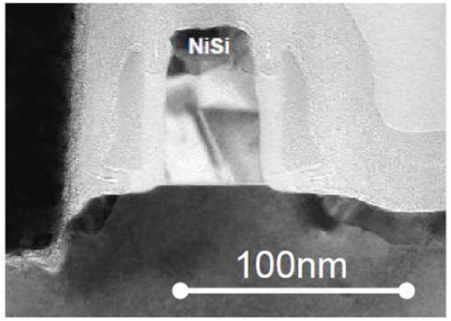
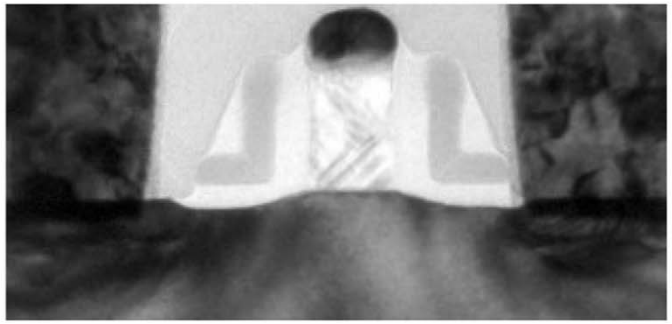
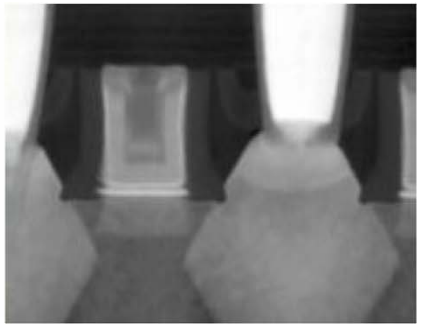
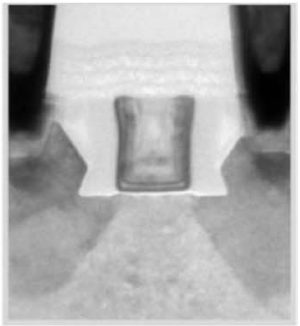
New architecture with shared cache delivering more performance and energy efficiency

Quad Core die with Intel® HD Graphics 4000 shown above
Transistor count: 1.4Billion Die size: 160mm²
** Cache is shared across all 4 cores and processor graphics

CMOS Technology Scaling

XTEM images with the same scale

courtesy V. Moroz (Synopsys, Inc.)

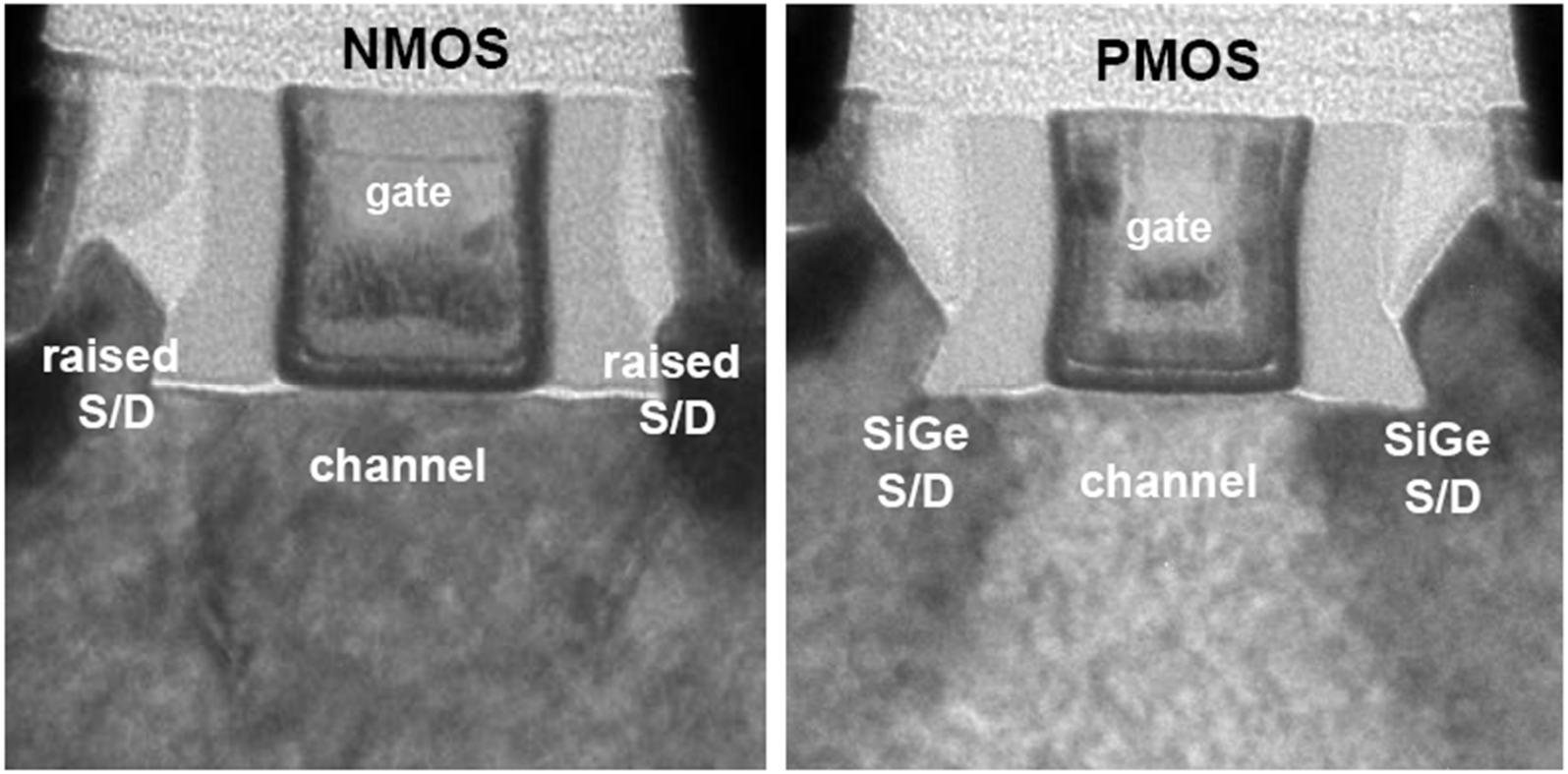
90 nm node	65 nm node	45 nm node	32 nm node
			
T. Ghani *et al.*, *IEDM* 2003	(after S. Tyagi *et al.*, *IEDM* 2005)	K. Mistry *et al.*, *IEDM* 2007	P. Packan *et al.*, *IEDM* 2009

- **Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.**
  - **Transistor performance has been boosted by other means.**

MOSFET Performance Boosters

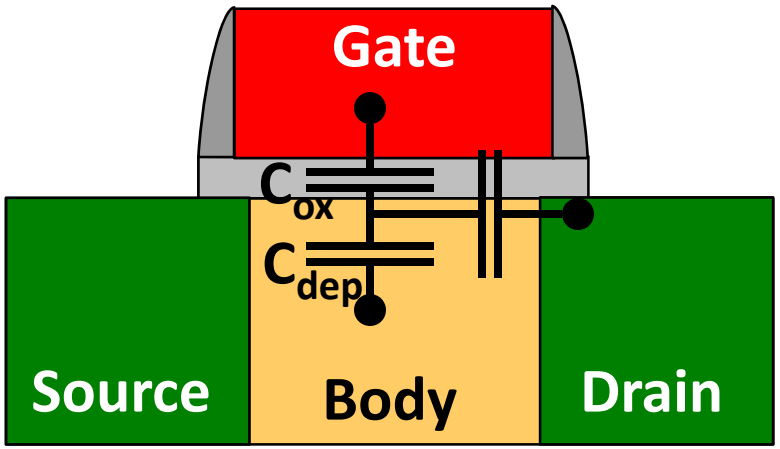
- Strained channel regions → $\mu_{eff}\uparrow$
- High-k gate dielectric and metal gate electrodes → $C_{ox}\uparrow$

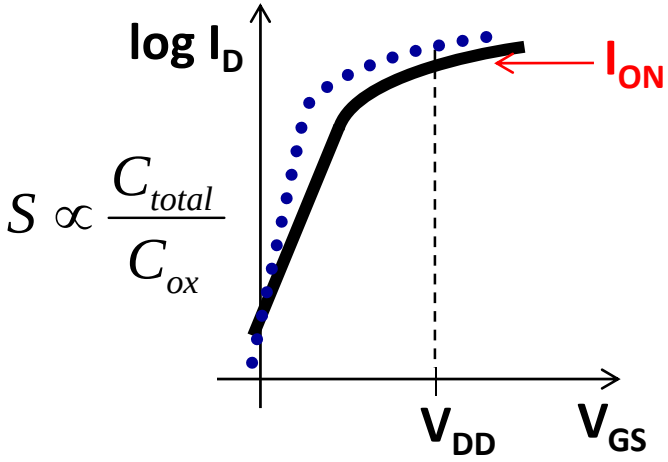
Cross-sectional TEM views of Intel's 32nm CMOS devices



P. Packan *et al.*, *IEDM Technical Digest*, pp. 659-662, 2009

Key to V_{DD} Reduction: Gate Control

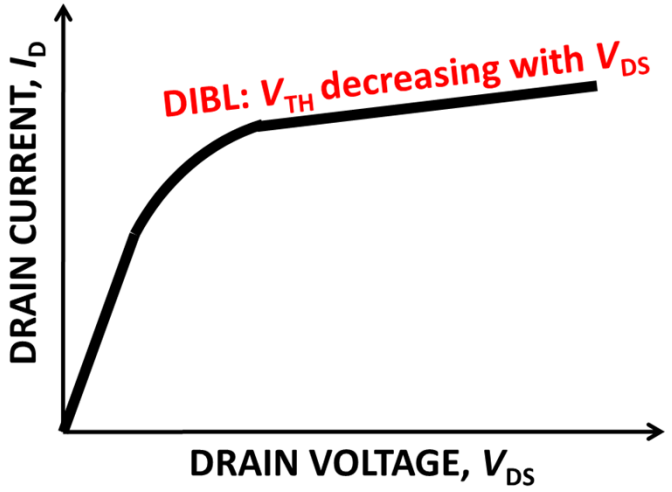




- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

→ **lower V_{DD} to achieve target I_{ON}/I_{OFF}**

→ **reduced short-channel effect (SCE) and drain-induced barrier lowering (DIBL)**

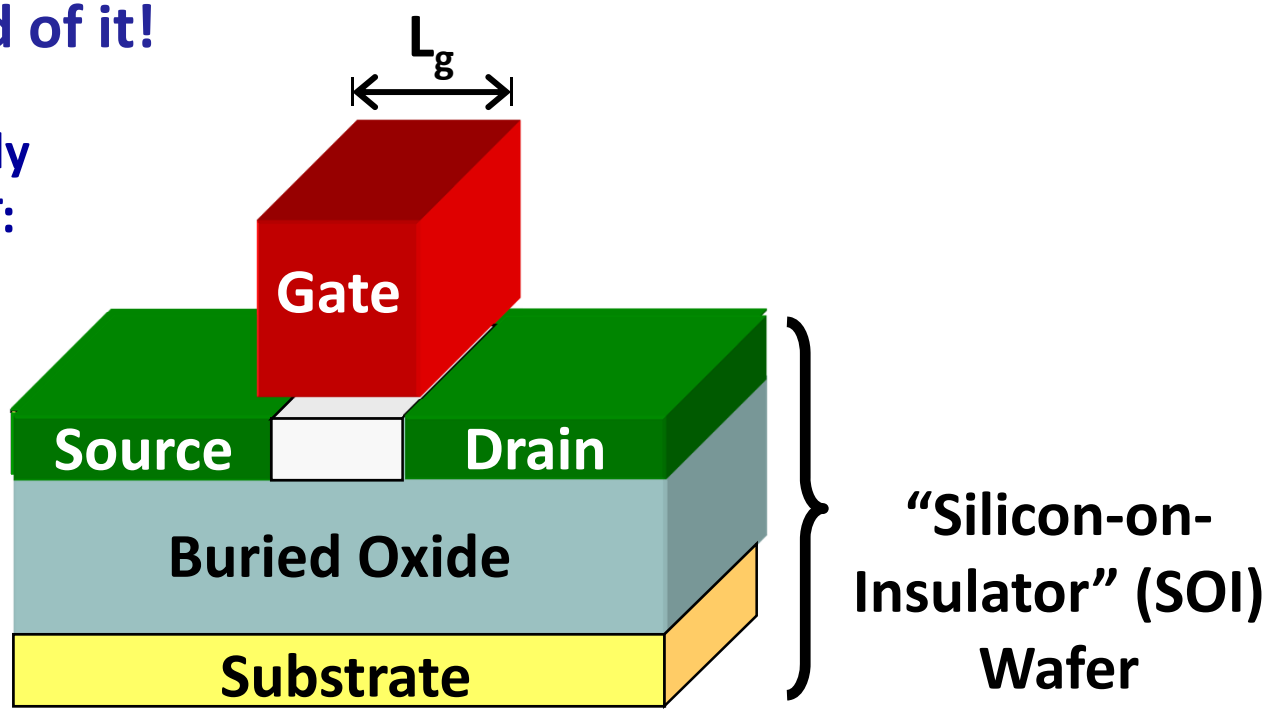


Why New Transistor Structures?

- Off-state leakage (I_{OFF}) must be suppressed as L_g is scaled down
  - allows for reductions in V_T and hence V_{DD}
- Leakage occurs in the region away from the channel surface

→ Let's get rid of it!

Thin-Body MOSFET:

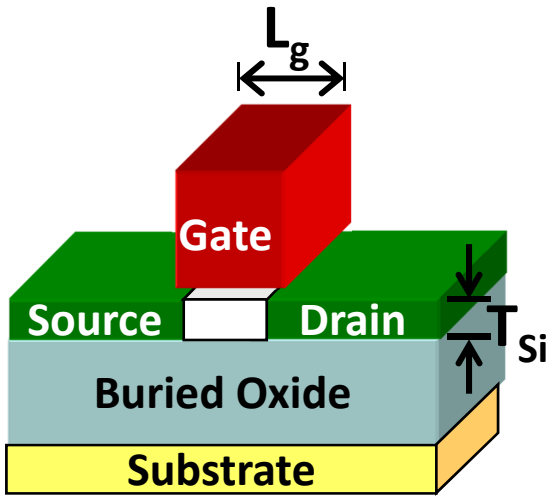


Thin-Body MOSFETs

- I_{OFF} is suppressed by using an adequately thin body region.
  - Body doping can be eliminated

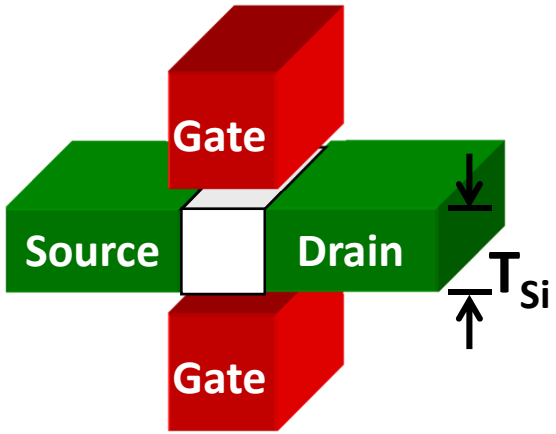
    → higher drive current due to higher carrier mobility

Ultra-Thin Body (UTB)



$T_{Si} < (1/4) \times L_g$

Double-Gate (DG)

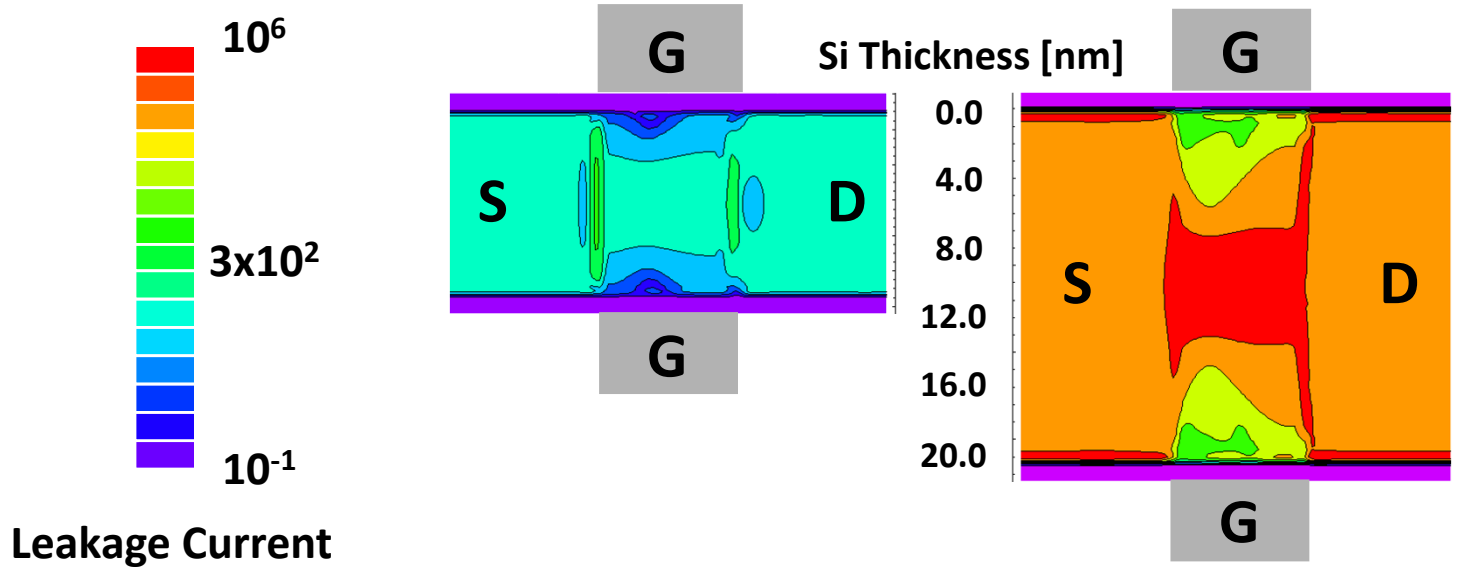


$T_{Si} < (2/3) \times L_g$

Effect of T_{Si} on OFF-state Leakage

L_g = 25 nm; $t_{ox,eq}$ = 12Å

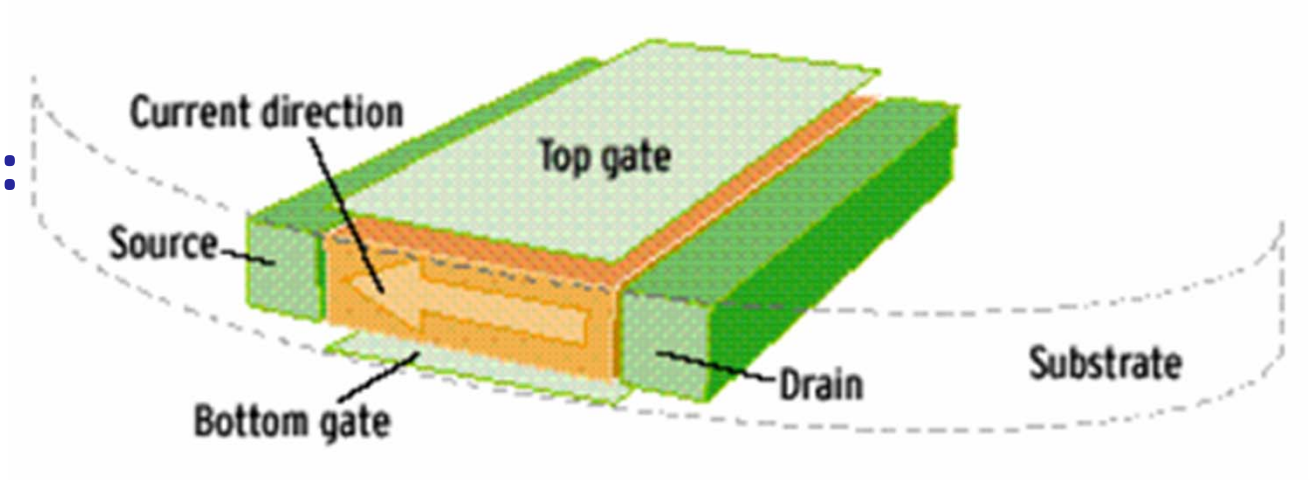
T_{Si} = 10 nm T_{Si} = 20 nm



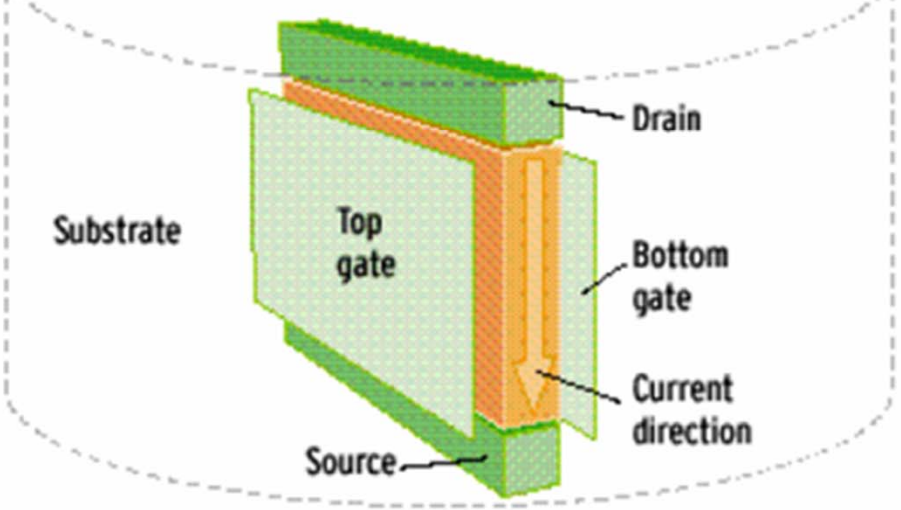
I_{OFF} = 2.1 nA/μm I_{OFF} = 19 μA/μm

Double-Gate MOSFET Structures

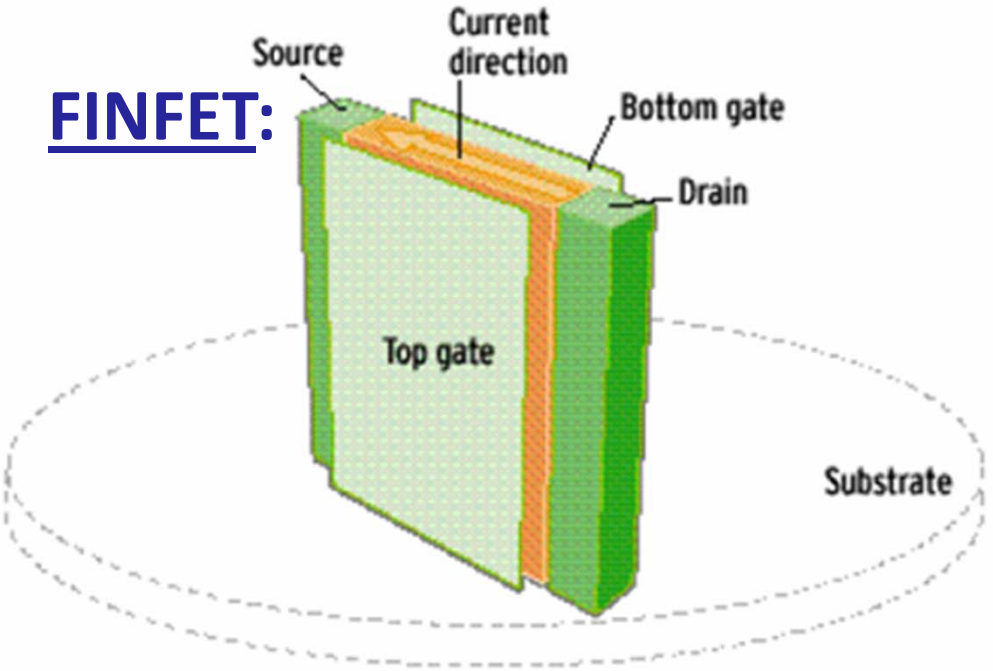
PLANAR:



VERTICAL

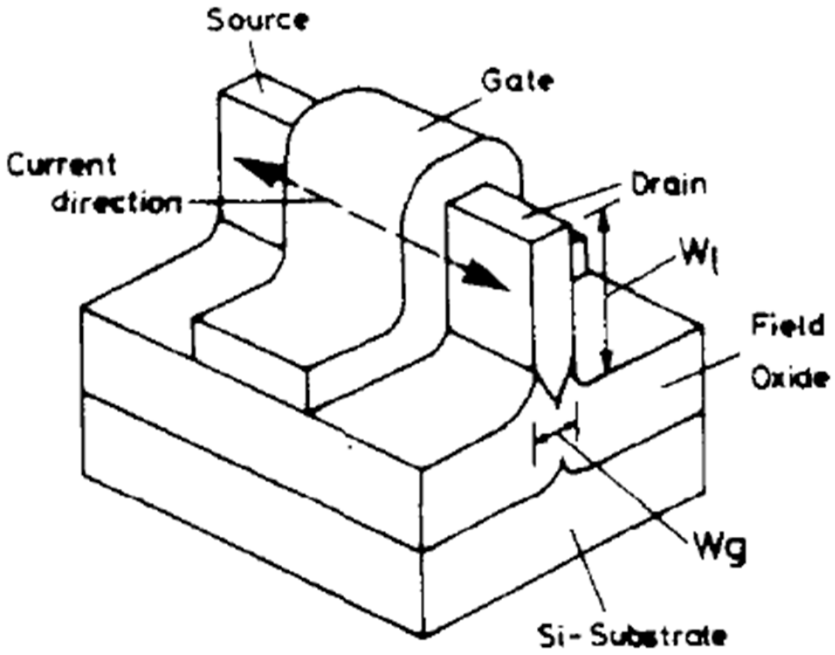


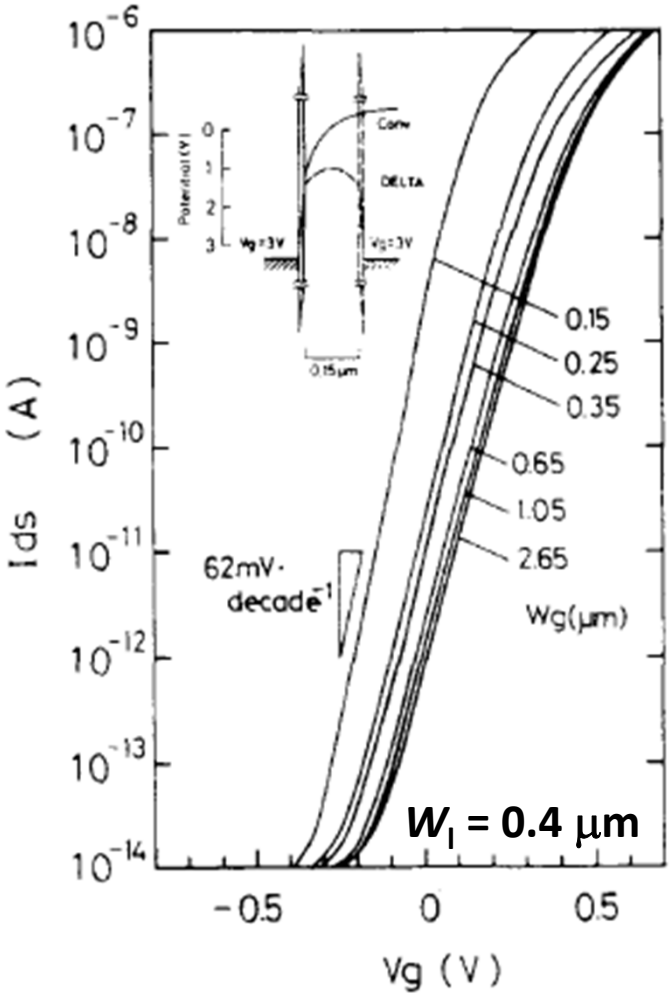
FINFET:



DELTA MOSFET

D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda (Hitachi Central Research Laboratory),
"A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET,"
IEEE Electron Device Letters Vol. 11, pp. 36-39, 1990

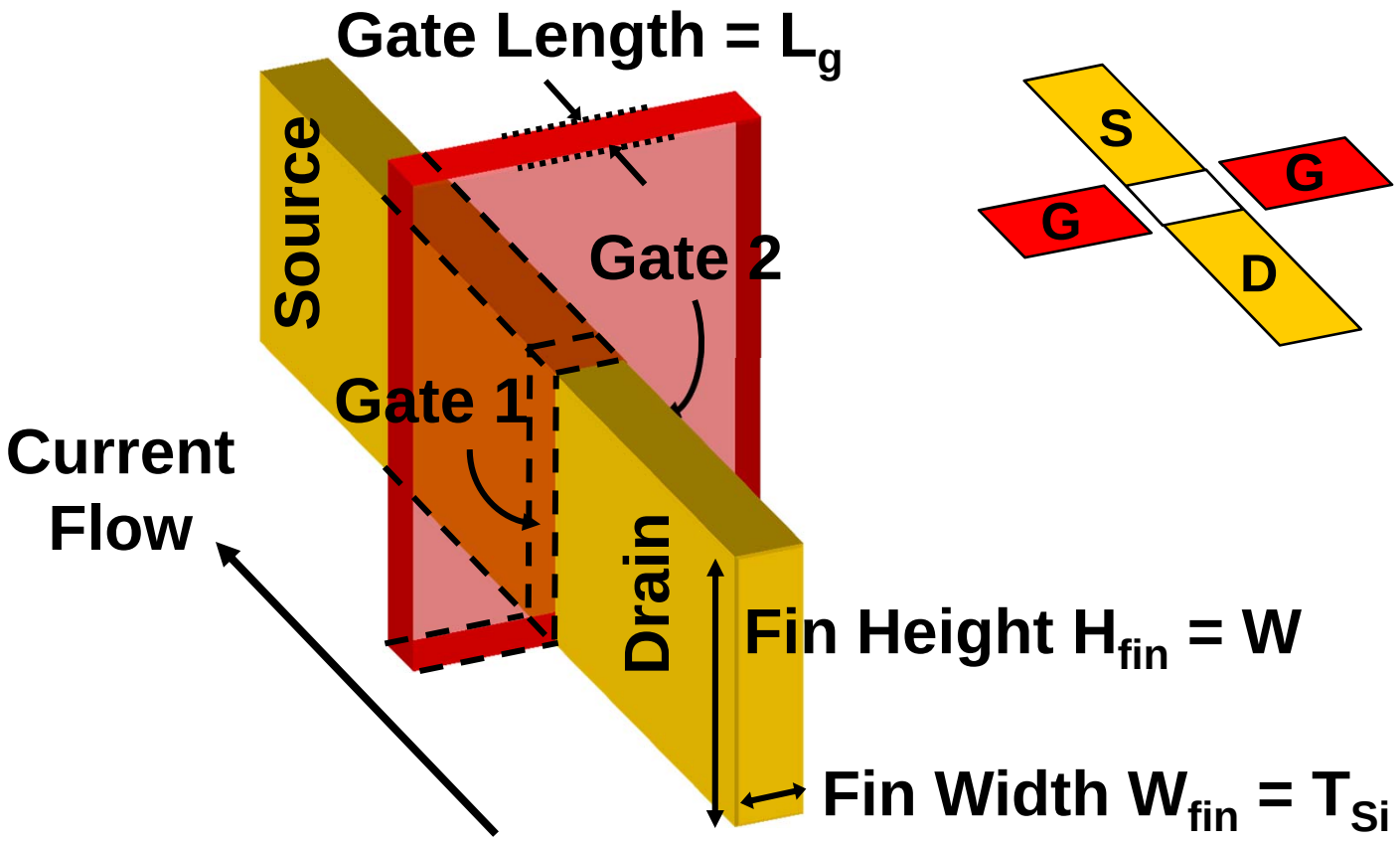




- **Improved gate control observed for W_g < 0.3 μm**
  - L_{EFF}= 0.57 μm

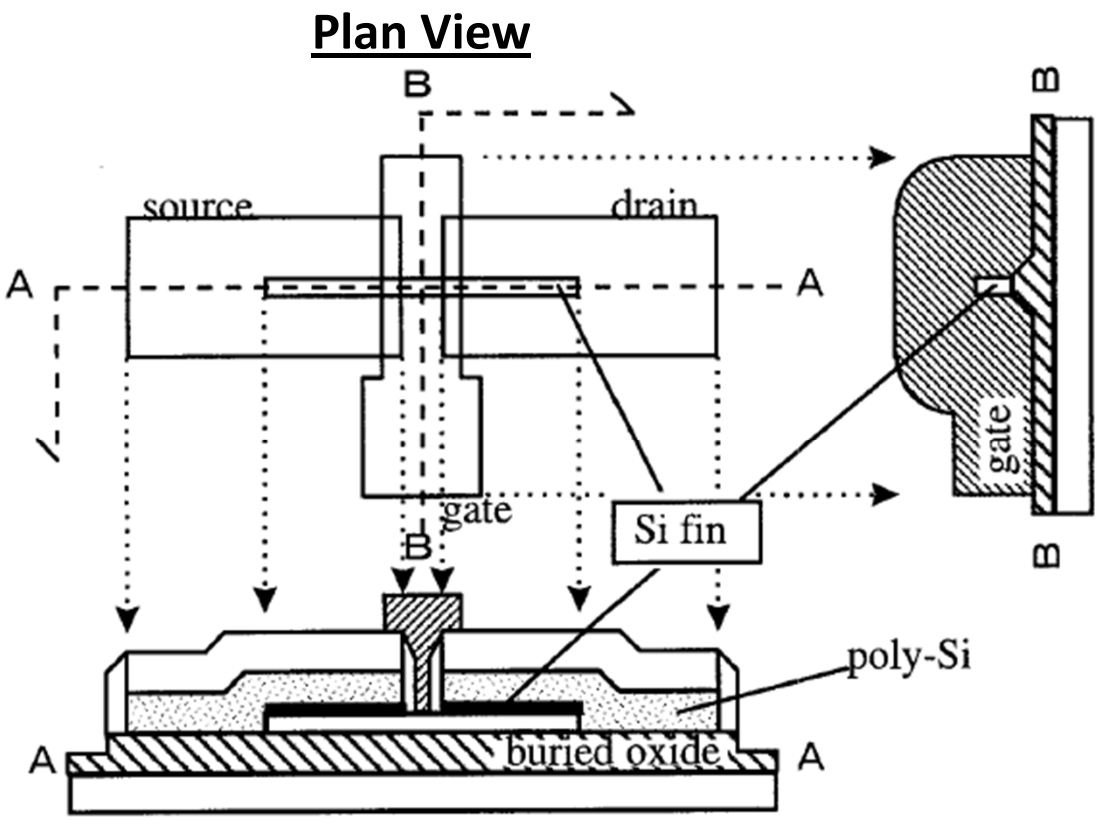
Double-Gate FinFET

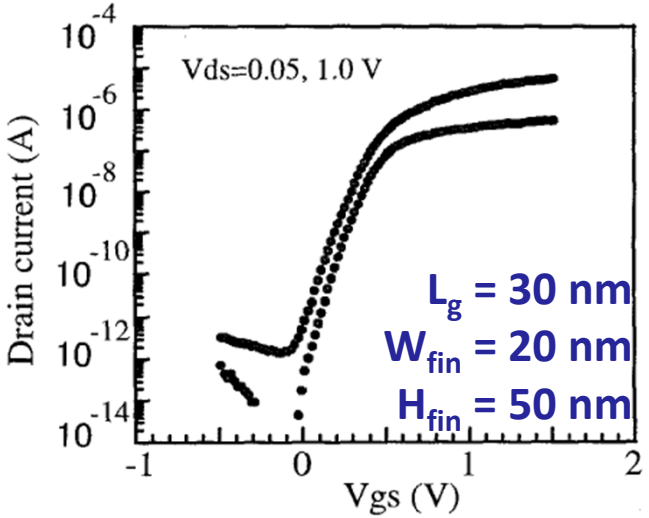
- Self-aligned gates straddle narrow silicon fin
- Current flows parallel to wafer surface

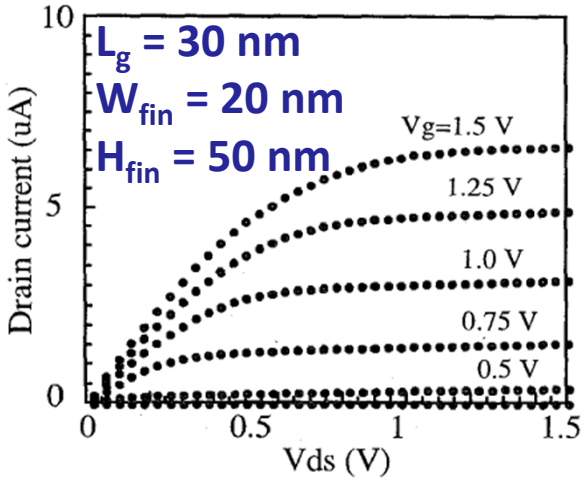


1998: First n-channel FinFETs

D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu,
"A folded-channel MOSFET for deep-sub-tenth micron era,"
IEEE International Electron Devices Meeting Technical Digest, pp. 1032-1034, 1998







- Devices with L_g down to 17 nm were successfully fabricated

1999: First p-channel FinFETs

X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEEE International Electron Devices Meeting Technical Digest*, pp. 67-70, 1999

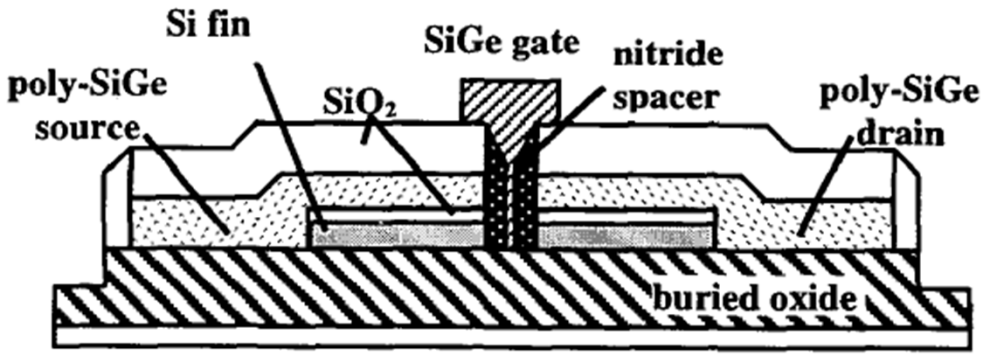
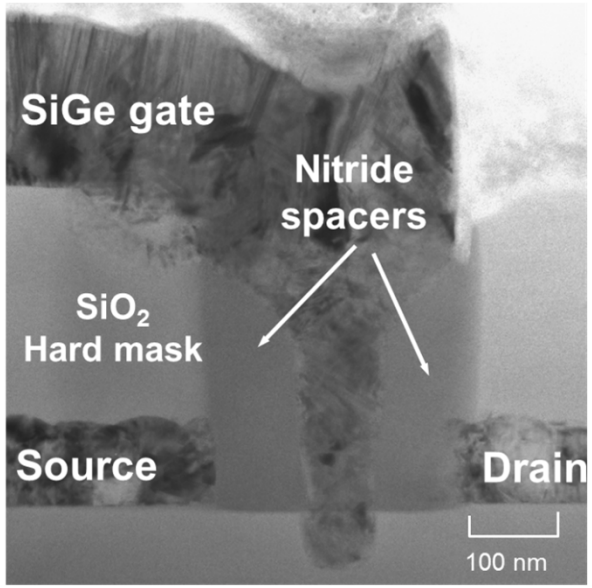
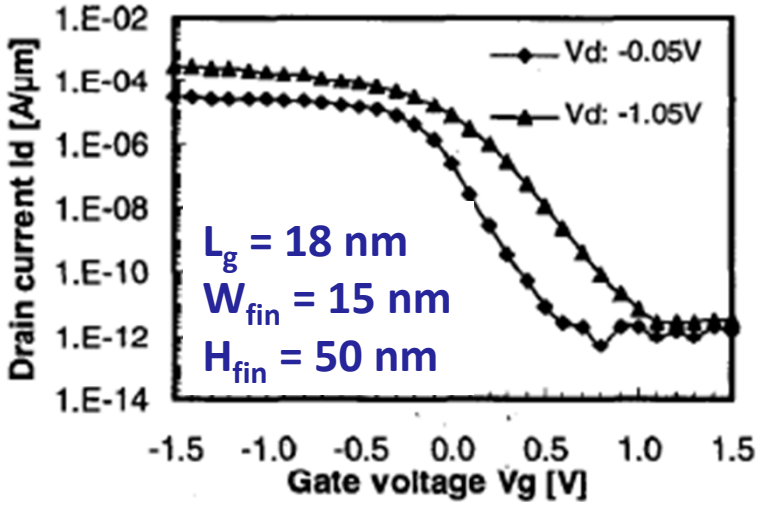
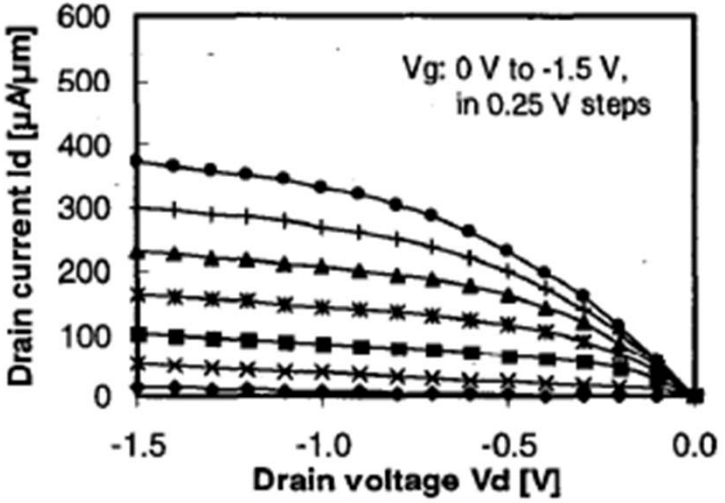


Figure 1: Schematic drawing of FinFET



Transmission Electron Micrograph





Recognition

The New York Times

MONDAY, DECEMBER 6, 1999

Computer Chip Researchers Set to Showcase Advances

A Shift to Further Miniaturization Is Seen

By JOHN MARKOFF

Computer chip researchers are gathering for an industry conclave in Washington this week, where a range of technical presentations are expected to revive the recently flagging spirts of the semiconductor community.

The announcements planned by **I.B.M., Lucent's** Bell Laboratories, **Motorola**, the University of California at Berkeley and other research laboratories at the International Electron Device Meeting suggest that researchers are finding ways to accelerate the speed at which chip makers can further shrink the size of the microscopic transistors that are the basic component of microelectronic systems.

Word of the advances are significant now, since a number of prominent semiconductor researchers have been expressing concerns that the industry might be approaching fundamental physical limits that might curtail chip development.

"This is important because in the last five years there has been a doomsday feeling among semiconductor researchers," said Chenming Hu, a University of California at Berkeley electrical engineering professor. A research team led by Mr. Hu will present a paper detailing a new kind of transistor that the research team believes can be scaled down to just 18 nanometers — or about the width of 100 atoms. That would be about one-twentieth the size of today's smallest transistors.

The Berkeley researchers predict that the new transistor design could lead to devices that store 400 times as much data as today's densest memory chips.

While such a transistor might not be common for another decade, the Berkeley announcement indicates that it might be possible to extend the future of microscopic semiconductor circuitry well beyond the year 2014, when some researchers have been predicting that the technology would meet its theoretical limits.

Since the 1960's, the chip industry has operated under an assumption that had proved so reliable that it is known as Moore's Law — named for the Intel co-founder Gordon Moore, who had observed that the number of transistors that chip makers could fit on a given piece of silicon was doubling every 18 months. But recently, even Mr. Moore himself has warned that the growth rate was coming at such spiraling costs that Moore's Law might no longer be sustainable.

This week's meeting, however, may indicate that the circuiteers have made new breakthroughs in their quest for the infinitessimal.

I.B.M. will also report on a new complementary metal oxide semiconductor, or CMOS, chip-making technology that the company says should pave the way for a generation of microprocessors that will reach computing speeds above a billion operations a second. The new technology is based on a relatively new kind

Developments in transistors will be prominent.

of manufacturing process known as silicon-on-insulator, which offers higher speeds and lower power consumption than conventional silicon-based CMOS chips.

The company would not state specific product dates but said it generally makes such technology announcements a year to 18 months before products are introduced.

Researchers at Motorola Laboratories have developed a new class of materials known as perovskites (pronounced per-AHV-skights) that will permit a new class of transistors.

DARPA Significant Technical Achievement Award
presented at DARPATECH 2000 Symposium

UC-Berkeley FinFET Patent

(12) **United States Patent**
Hu et al.

(10) **Patent No.: US 6,413,802 B1**
(45) **Date of Patent: Jul. 2, 2002**

(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

(73) Assignee: **The Regents of the University of California**, Oakland, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/695,532**
(22) Filed: Oct. 23, 2000

(51) **Int. Cl.**[7] **H01L 21/00**; H01L 21/84

(52) **U.S. Cl.** **438/151**; 438/283

(58) **Field of Search** 438/151, 157, 438/201, 223, 241, 258, 279, 283, 437, 588, 594, 259, 270, 303, 305, 589, 592

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,356,824 A		10/1994	Chouan et al.	437/41
5,604,368 A	*	2/1997	Taur et al.	257/348
5,646,058 A	*	7/1997	Taur et al.	438/283
5,773,331 A		6/1998	Solomon et al.	438/164
5,804,848 A		9/1998	Mukai	257/270
5,899,710 A		5/1999	Mukai	438/156
6,214,670 B1	*	4/2001	Shih et al.	438/259

OTHER PUBLICATIONS

V. Subramanian et al., "A Bulk-Si-compatible Ultrathin-body SOI Technology for sub-100nm MOSFETS," Proceedings of the 57th Annual Device Research Conference, pp. 28–29 (1999).

Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era," 1998 IEEE International Electron Device Meeting Technical Digest, pp. 1032–1034 (1998).

Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE International Electron Device Meeting Technical Digest, pp. 67–70 (1999).

Auth et al., Vertical, Fully-Depleted, Surrounding Gate MOSFETS on sub-0.1μm Thick Silicon Pillars, 1996 54th Annual Device Research Conference Digest, pp. 108–109 (1996).

Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)—A Novel Vertial Ultrathin SOI MOSFET," IEEE Electron Device Letters, v. 11(1), pp. 36–38 (1990).

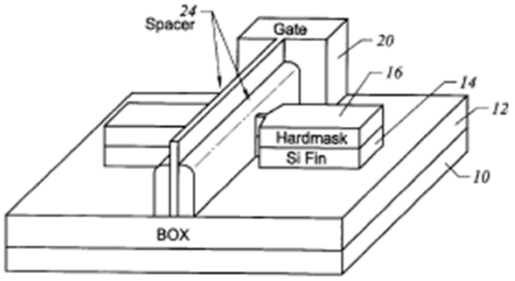
(List continued on next page.)

Primary Examiner—David Nelms
Assistant Examiner—Phuc T. Dang
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP; Henry K. Woodward

(57) **ABSTRACT**

A FinFET device is fabricated using conventional planar MOSFET technology. The device is fabricated in a silicon layer overlying an insulating layer (e.g., SIMOX) with the device extending from the insulating layer as a fin. Double gates are provided over the sides of the channel to provide enhanced drive current and effectively suppress short channel effects. A plurality of channels can be provided between a source and a drain for increased current capacity. In one embodiment two transistors can be stacked in a fin to provide a CMOS transistor pair having a shared gate.

28 Claims, 4 Drawing Sheets



What is claimed is:

1. A method of fabricating a double gate MOSFET device comprising the steps of:

a) providing a silicon on insulator (SOI) substrate with a first silicon layer overlying an insulating layer and having an exposed major surface,

b) providing an etchant mask on the major surface,

c) patterning the etchant mask to define source, drain, and channel regions and expose surrounding portions of the silicon layer,

d) etching the exposed silicon layer and forming source, drain, and channel regions extending from the insulator layer, the channel being a fin with a top surface and two opposing sidewalls,

e) forming a gate dielectric on sidewalls of the channel region,

f) depositing gate material over the etchant mask and the gate dielectric,

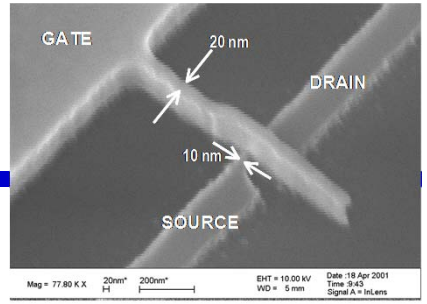
g) selectively masking and etching the gate material to form a gate on the top surface and sidewalls of the channel region and separated from the channel region by the gate dielectric and the etchant mask,

h) forming dielectric spacers between the gate and the source and drain regions, and

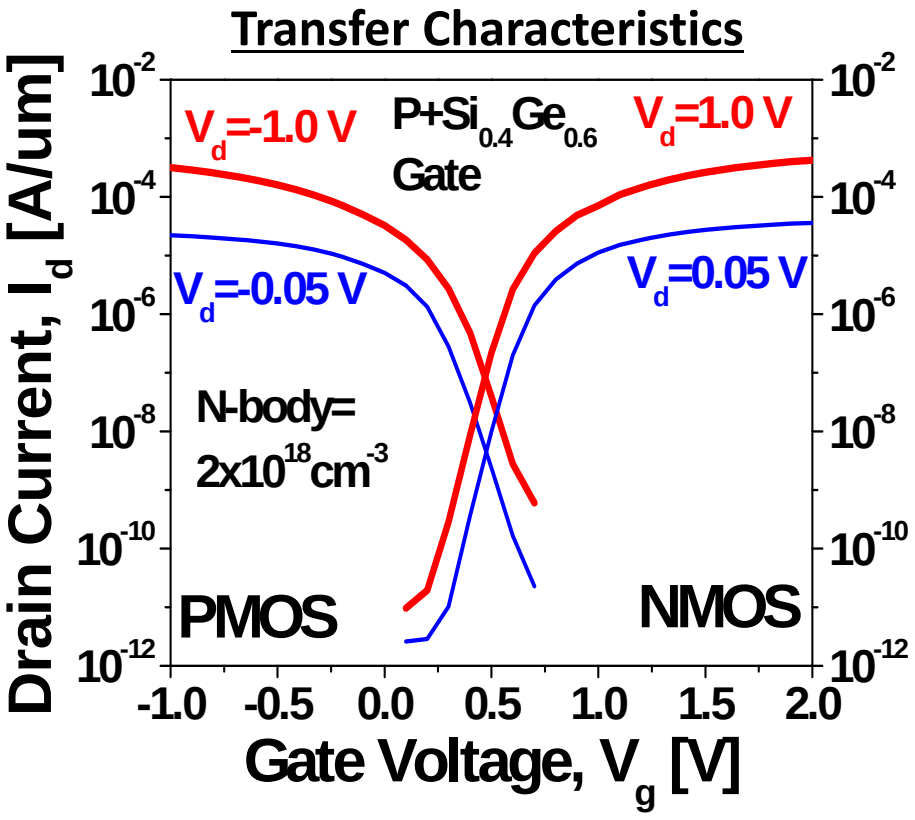
i) doping the source and drain regions.

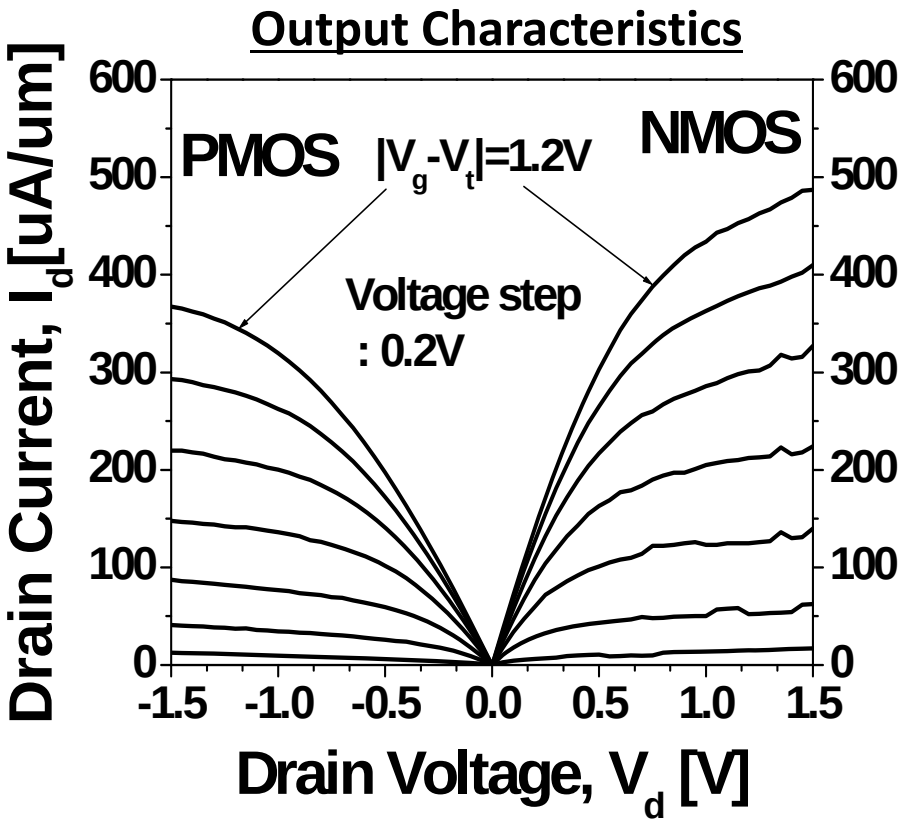
+ 27 additional claims…

2001: 15 nm FinFETs



Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, C. Hu, "Sub-20nm CMOS FinFET technologies," *IEEE International Electron Devices Meeting Technical Digest*, pp. 421-424, 2001

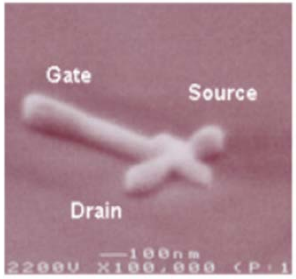




W_{fin} = 10 nm; T_{ox} = 2.1 nm

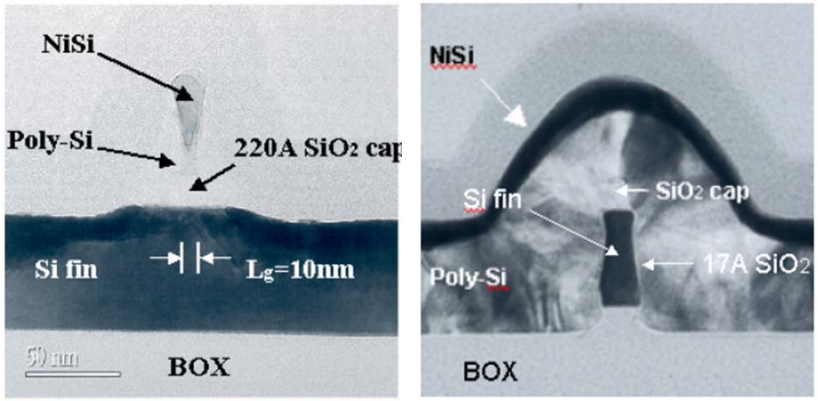
2002: 10 nm FinFETs

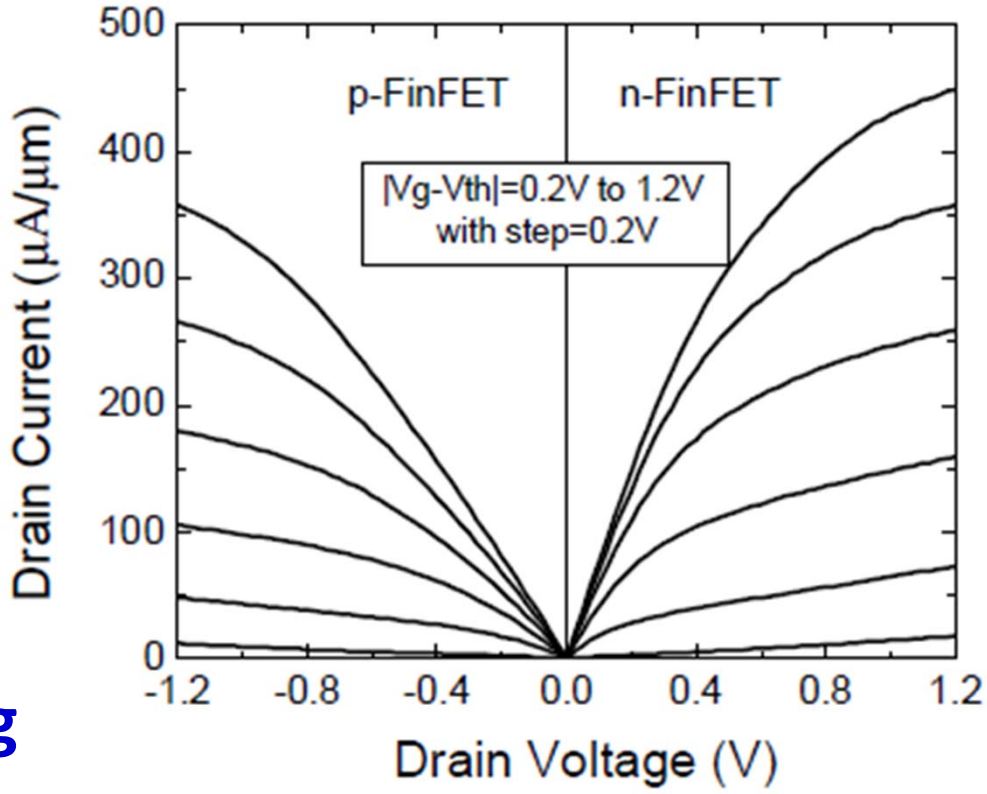
SEM image:



B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Hu, T.-J. King, J. Bokor, M.-R. Lin, and D. Kyser, "FinFET scaling to 10nm gate length," *International Electron Devices Meeting Technical Digest*, pp. 251-254, 2002

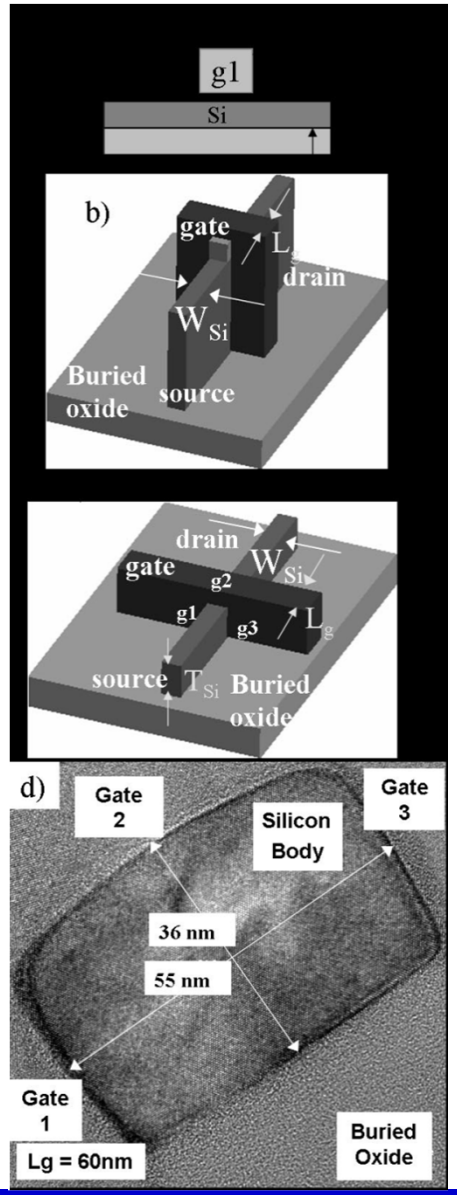
TEM images

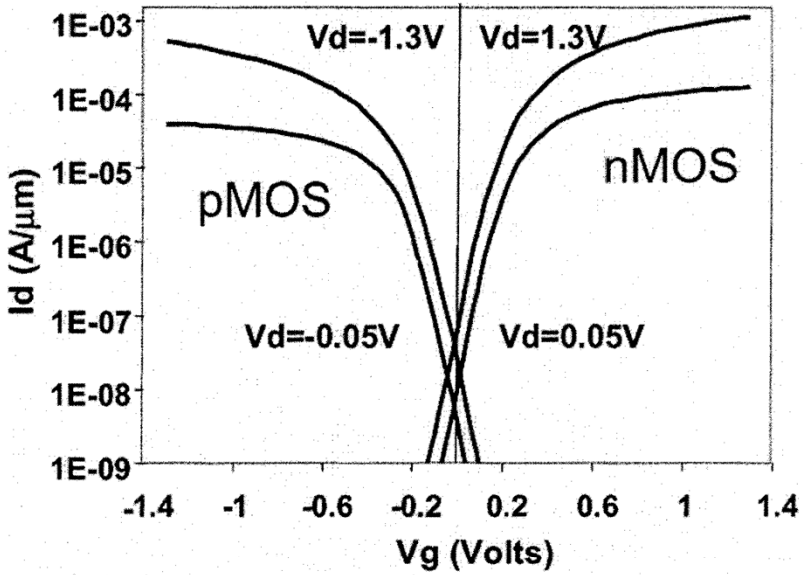


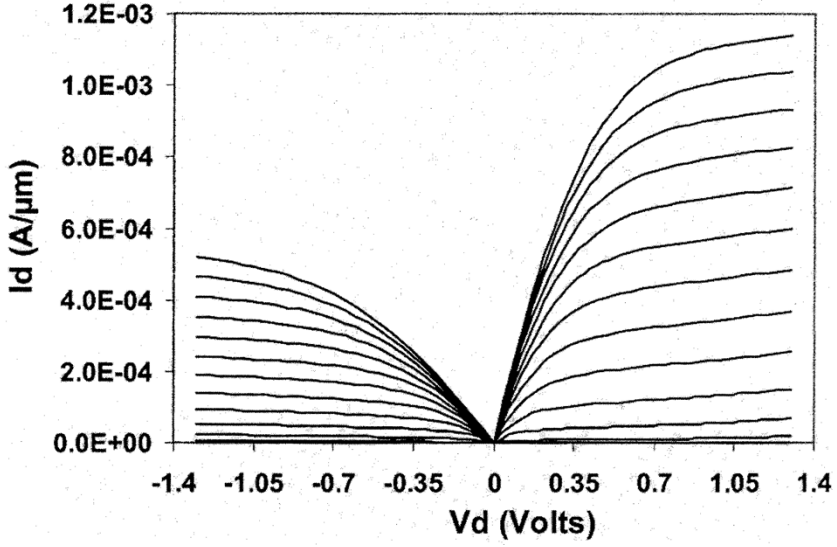


- **These devices were fabricated at AMD, using optical lithography.**

Tri-Gate FET (Intel Corp.)







L_g = 60 nm
W_{fin} = 55 nm
H_{fin} = 36 nm

Bulk FinFET (Samsung Electronics)

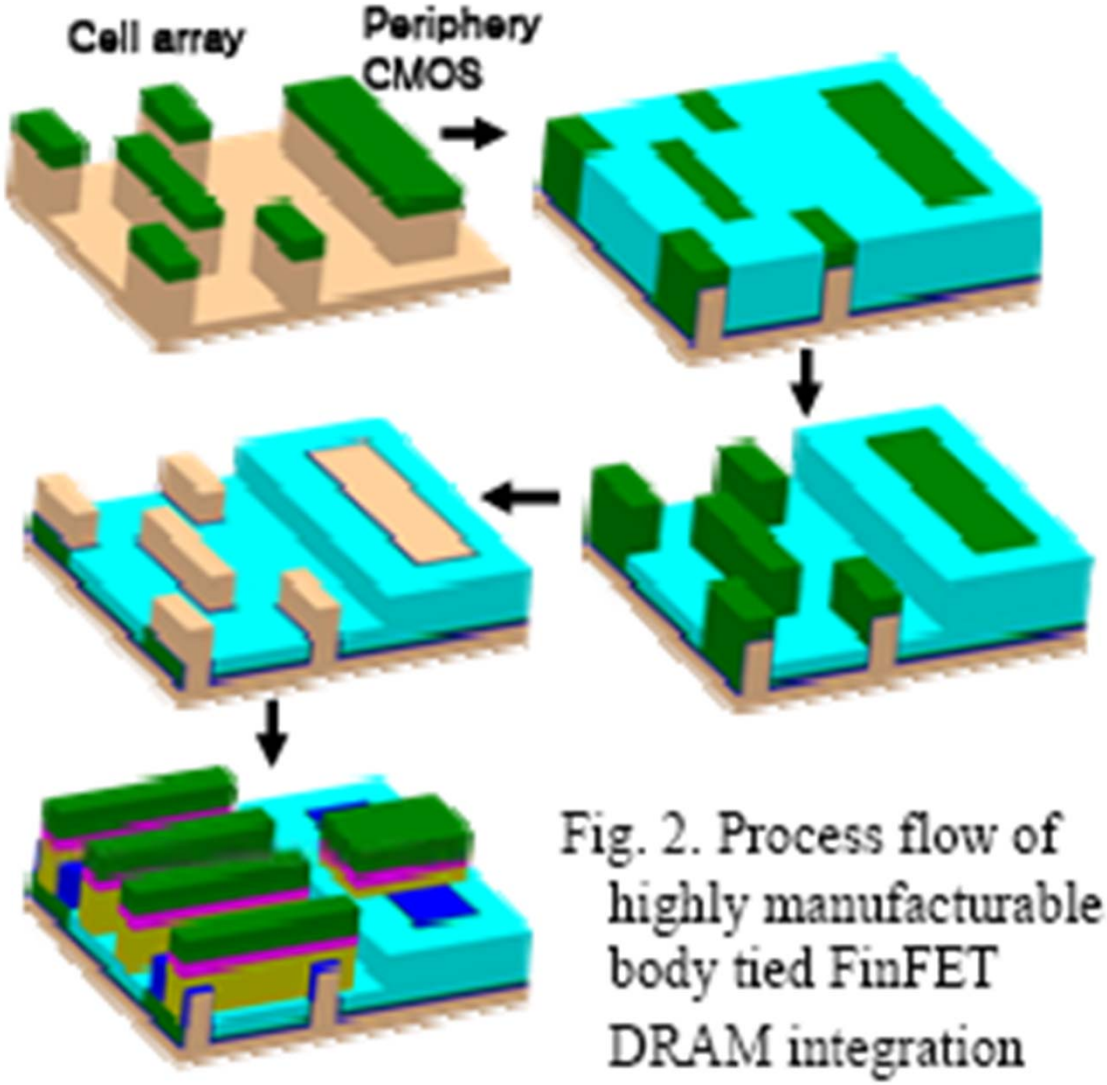


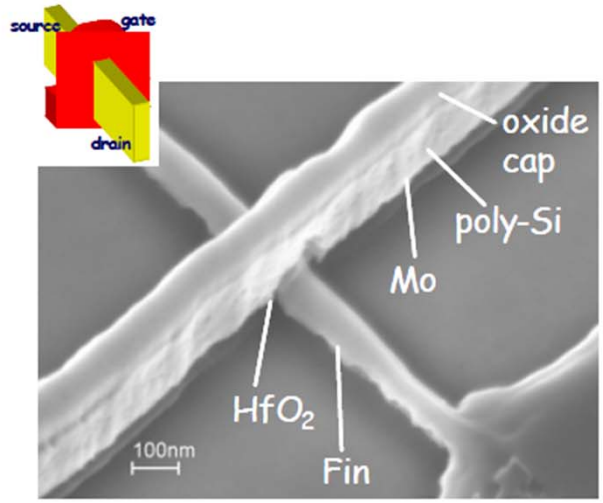
Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

- FinFETs can be made on bulk-Si wafers
  - ✓lower cost
  - ✓improved thermal conduction
- 90 nm L_g FinFETs demonstrated
  - W_{fin} = 80 nm
  - H_{fin} = 100 nm

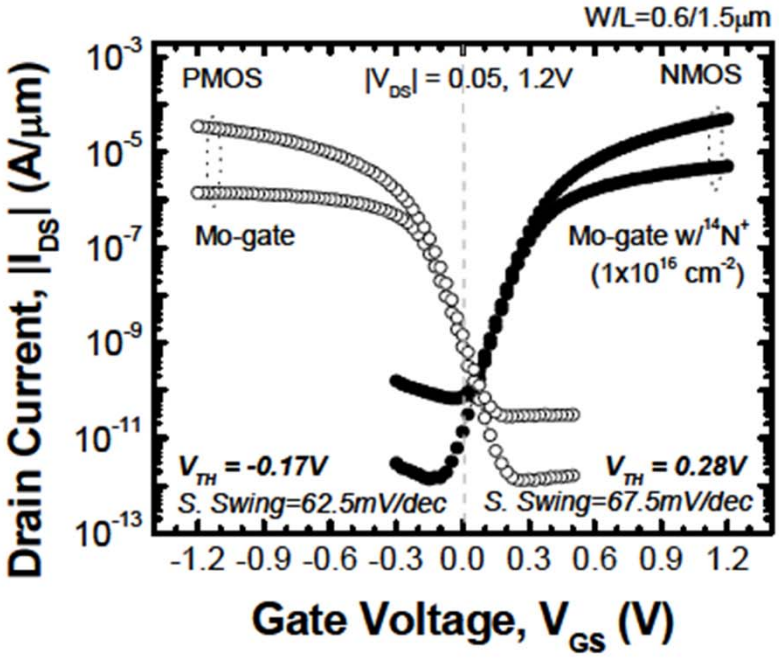
  DIBL = 25 mV

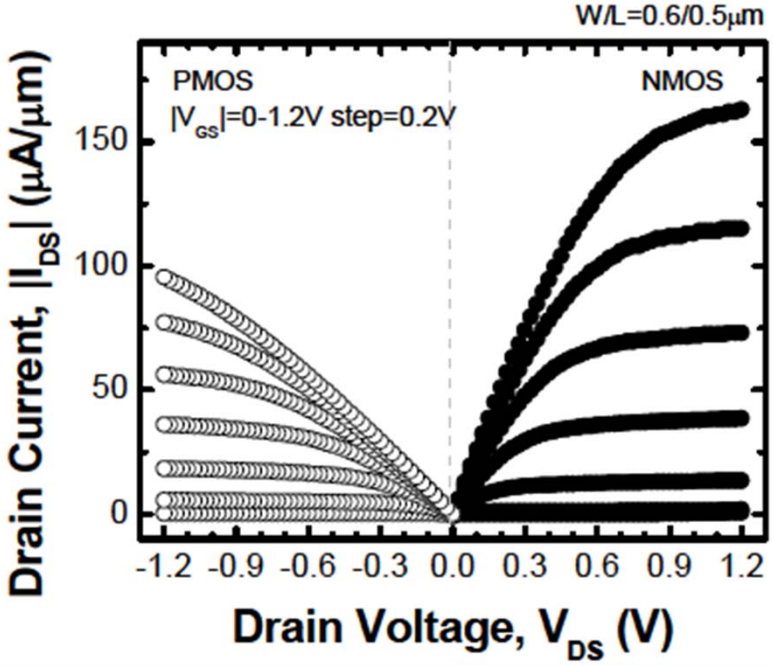
C.-H. Lee *et al.*, *Symposium on VLSI Technology Digest*, pp. 130-131, 2004

2004: High-k/Metal Gate FinFET



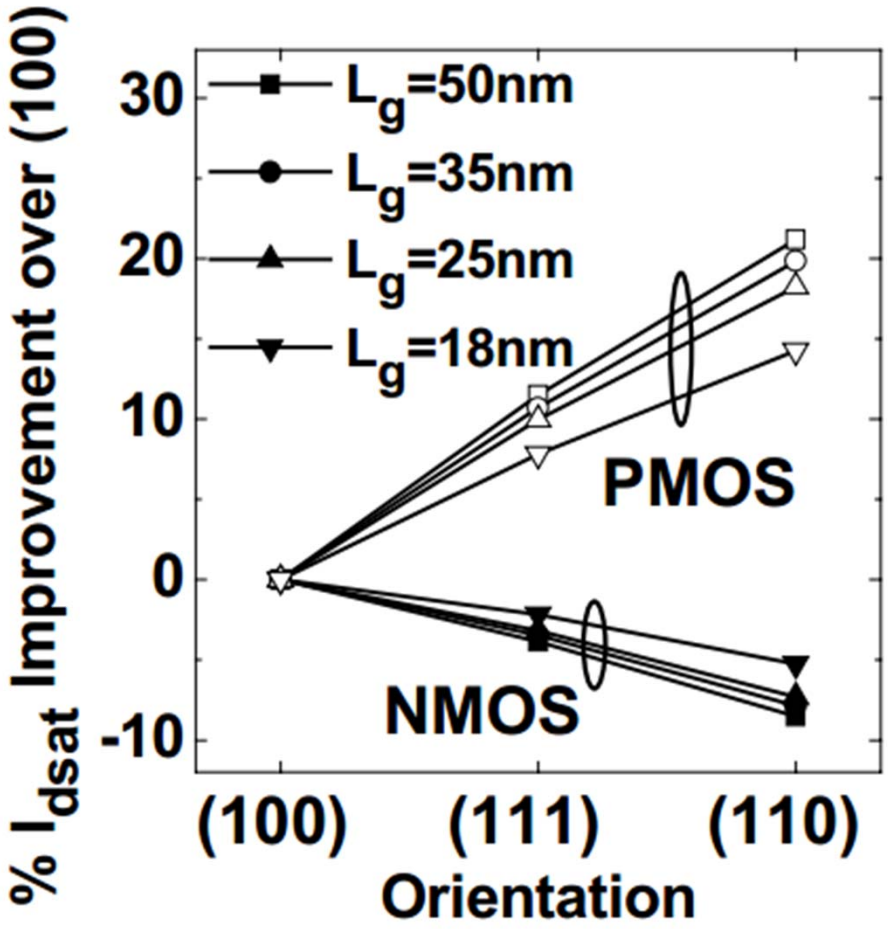
D. Ha, H. Takeuchi, Y.-K. Choi, T.-J. King, W. Bai, D.-L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum-gate HfO_2 CMOS FinFET technology," *IEEE International Electron Devices Meeting Technical Digest*, pp. 643-646, 2004



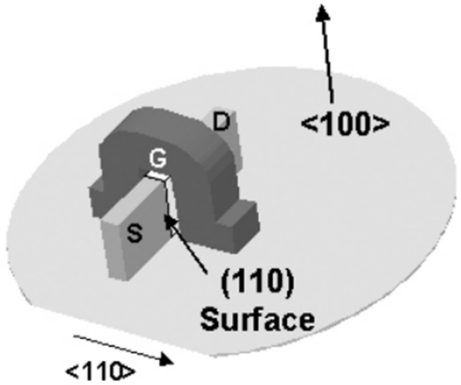


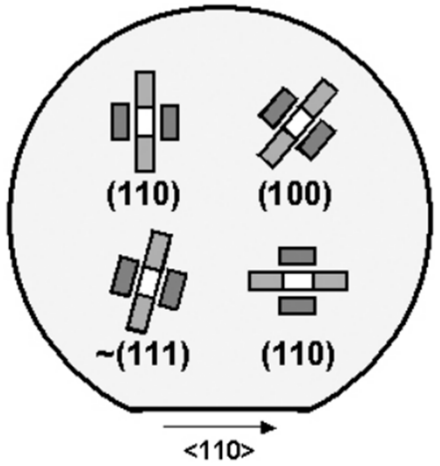
Impact of Fin Layout Orientation

L. Chang *et al.* (IBM), *SISPAD* 2004



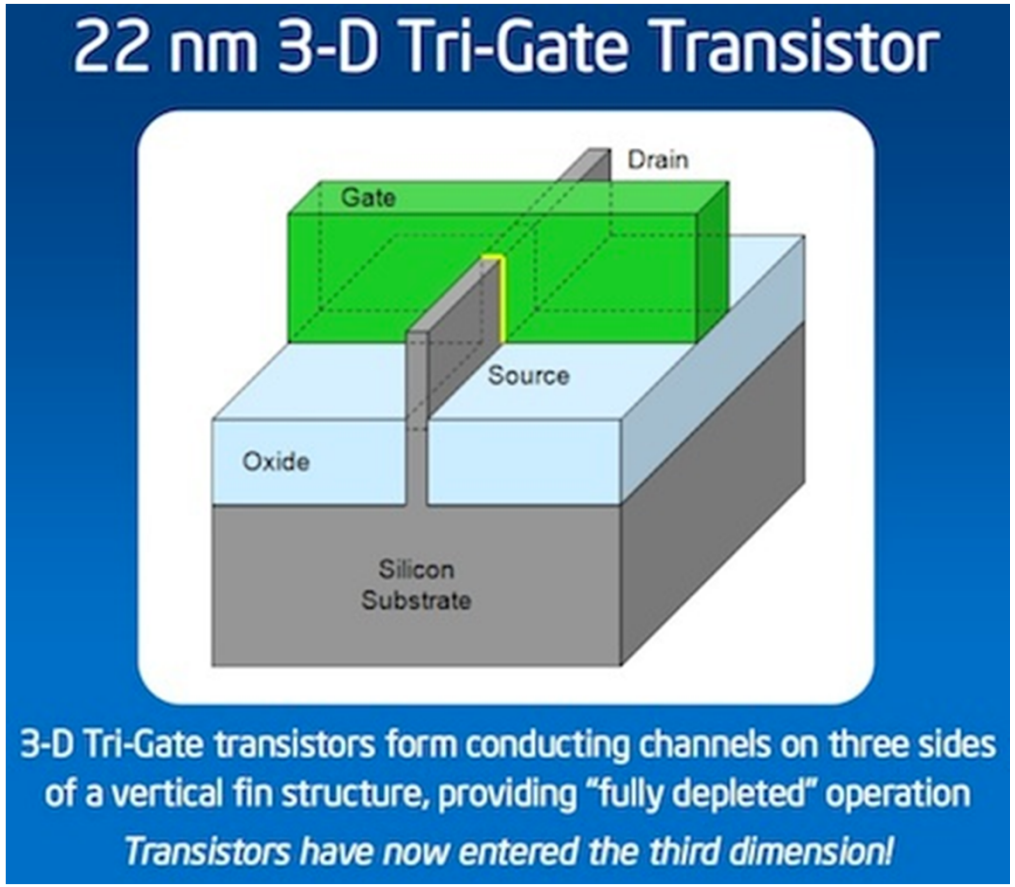
(Series resistance is more significant at shorter L_g.)





- **If the fin is oriented || or ⊥ to the wafer flat, the channel surfaces lie along (110) planes.**
  - **Lower electron mobility**
  - **Higher hole mobility**
- **If the fin is oriented 45° to the wafer flat, the channel surfaces lie along (100) planes.**

May 4, 2011: Intel Announcement



- **Ivy Bridge-based Intel® Core™ family processors will be the first high-volume chips to use 3-D Tri-Gate transistors.**
- **This silicon technology breakthrough will also aid in the delivery of more highly integrated Intel® Atom™ processor-based products…**

http://newsroom.intel.com/community/intel_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure

22 nm node Tri-Gate FETs

- L_g = 30-34 nm; W_{fin} = 8 nm; H_{fin} = 34 nm
- High-k/metal gate stack, EOT = 0.9 nm
- Channel strain techniques

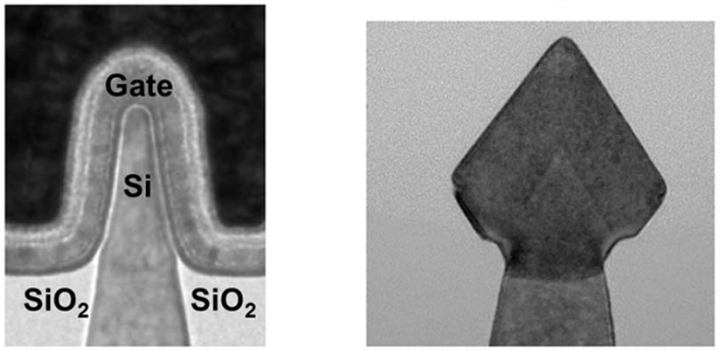
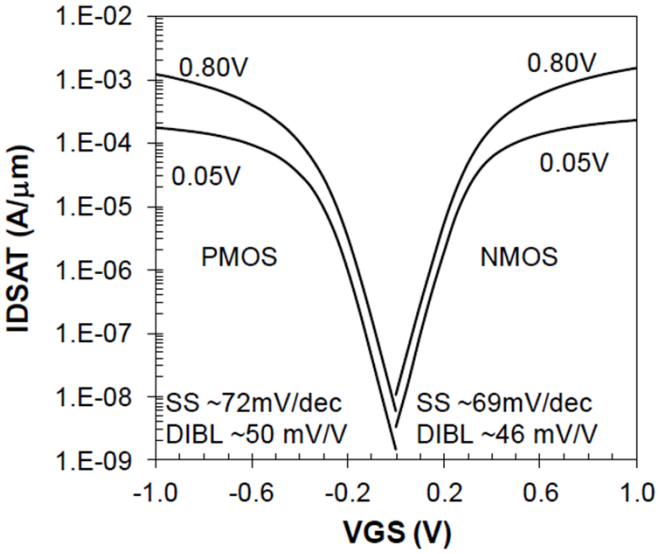
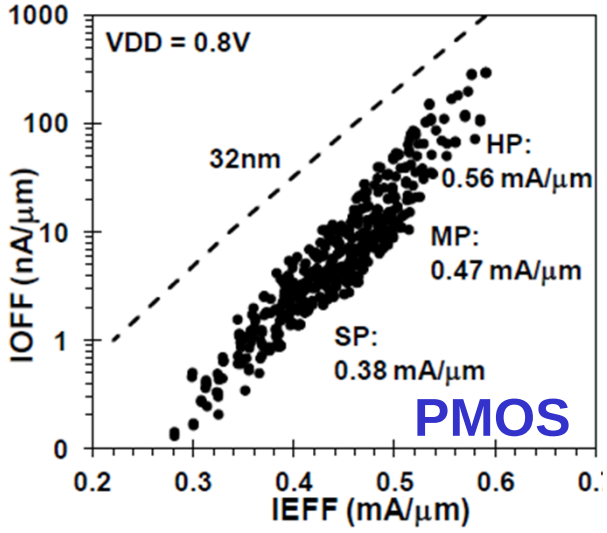


Fig.2 TEMs of the PMOS channel under the gate (left) and in the S/D region (right) showing the SiGe epitaxy in the S/D region.

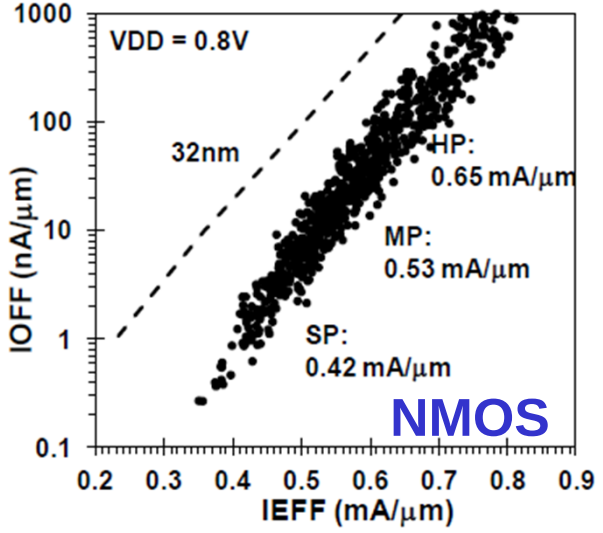
Transfer Characteristics



I_{OFF} *vs.* I_{EFF}



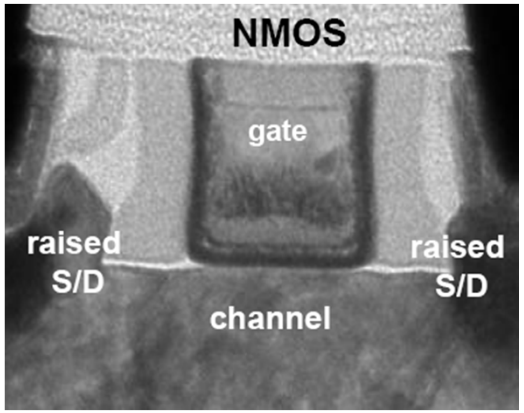
I_{OFF} *vs.* I_{EFF}

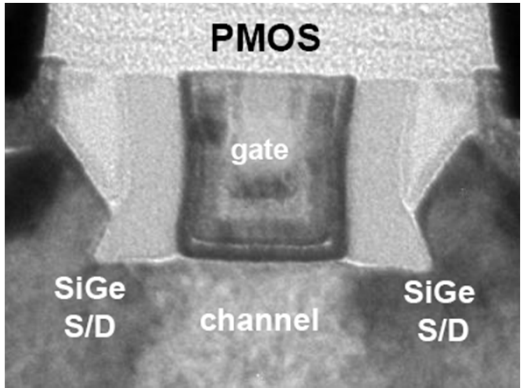


C. Auth *et al.*, *Symp. VLSI Technology* 2012

MOSFET Evolution

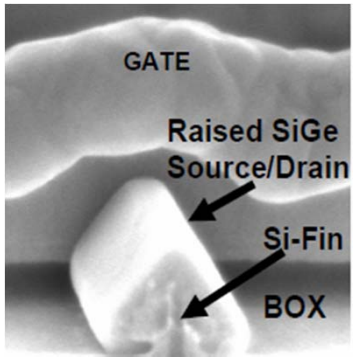
32 nm planar



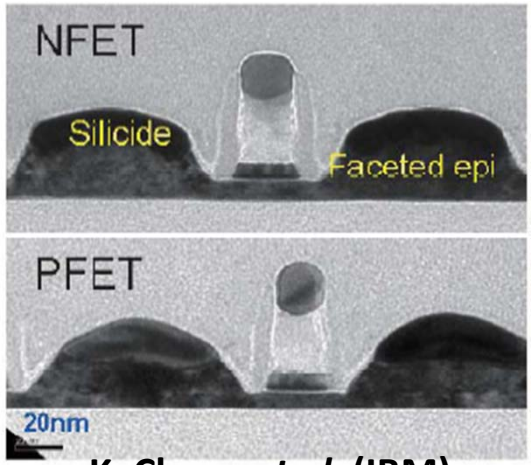


P. Packan *et al*. (Intel), *IEDM* 2009

22 nm thin-body

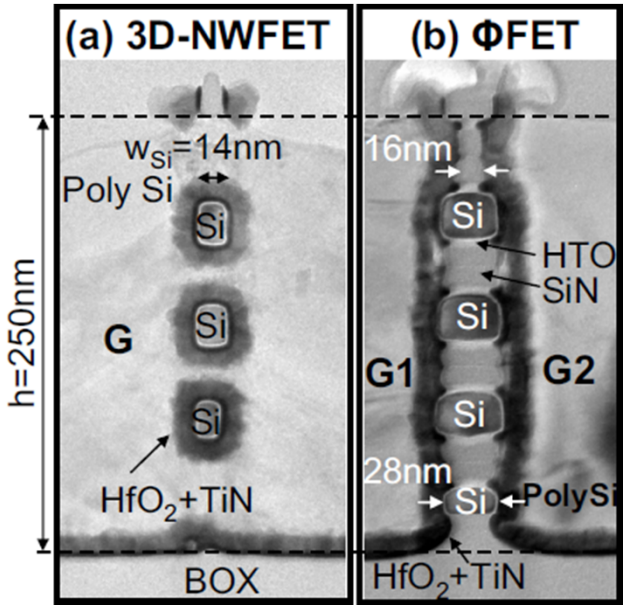


J. Kavalieros *et al*. (Intel) *Symp. VLSI Technology* 2006



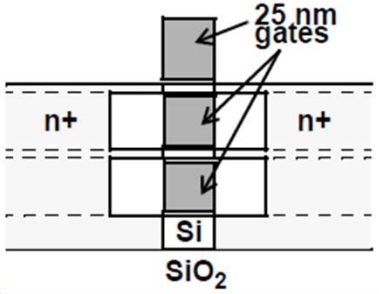
K. Cheng *et al*. (IBM) *Symp. VLSI Technology* 2009

beyond 10 nm nanowires?



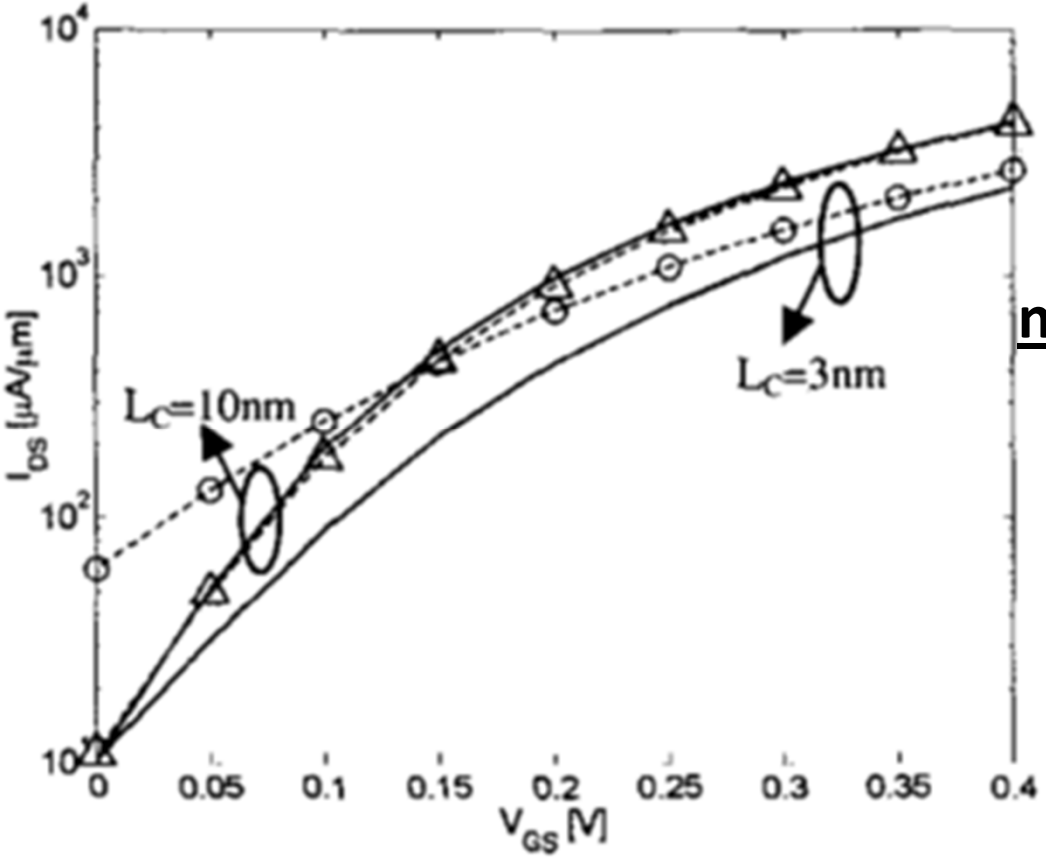
C. Dupré *et al*. (CEA-LETI) *IEDM* 2008

UC-Berkeley DARPA AME proposal: (Feb. 1997)



Channel-Length Scaling Limit

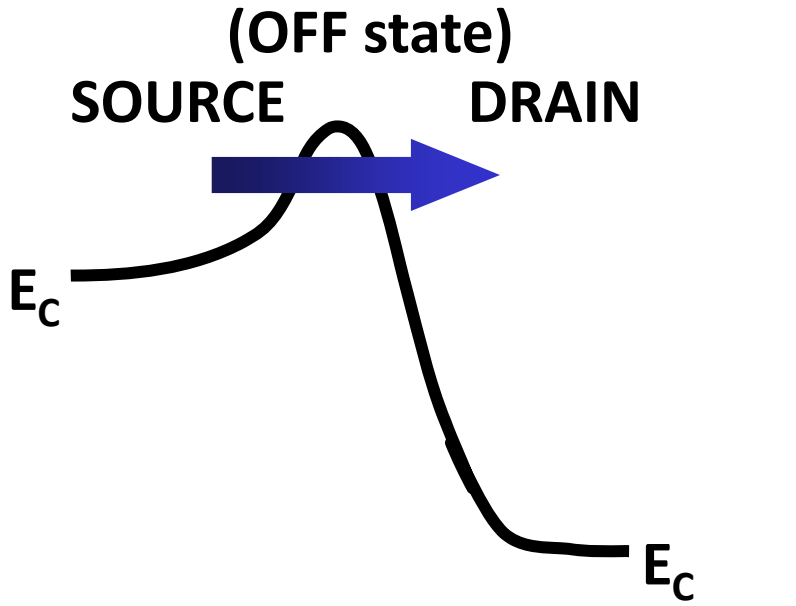
- **Quantum mechanical tunneling sets a fundamental scaling limit for the channel length.**



J. Wang *et al.*, *IEDM Technical Digest*, pp. 707-710, 2002

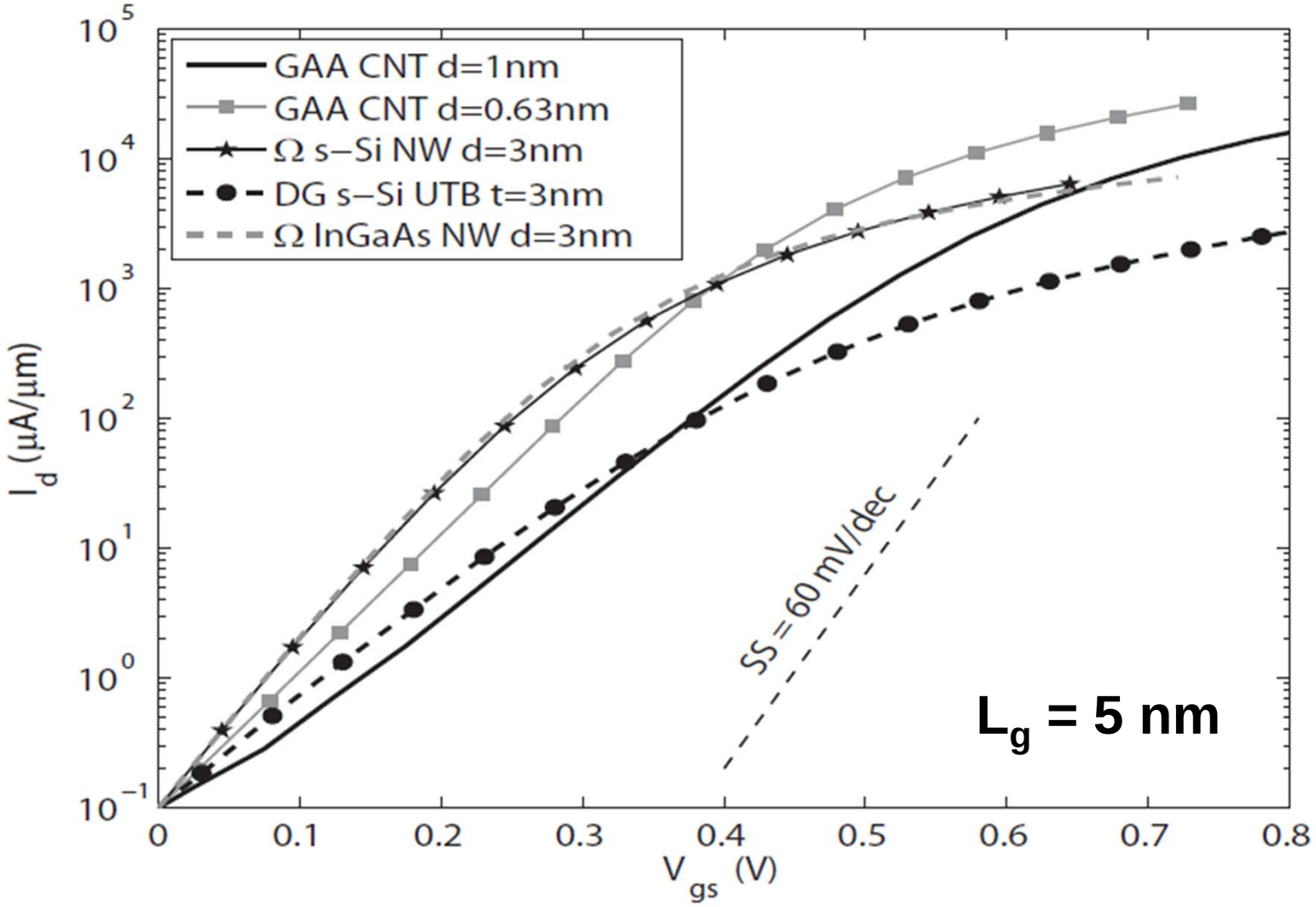
If electrons can easily tunnel through the source potential barrier, the gate cannot shut off the transistor.

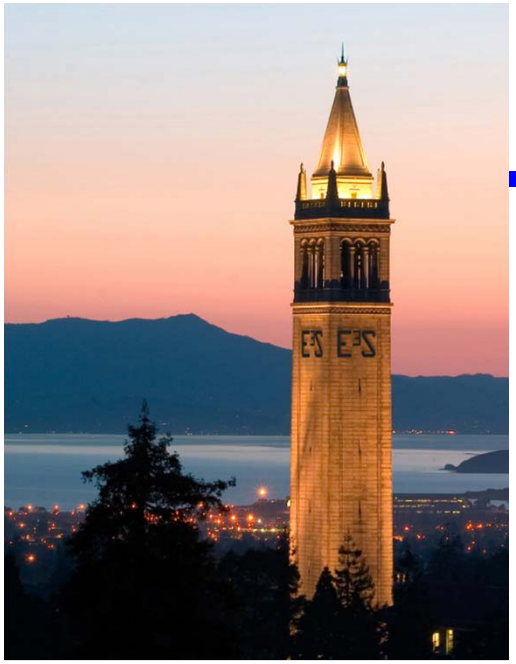
nMOSFET Energy Band Diagram



Ultimately Scaled MOSFETs

M. Luisier *et al.*, *IEDM* 2011





National Science Foundation (NSF)

Science and Technology Center (STC)

for Energy Efficient Electronics Science

Goal: Develop a new switch that can operate with V_{DD} = 1 mV

PI: Eli Yablonovitch (UC Berkeley)

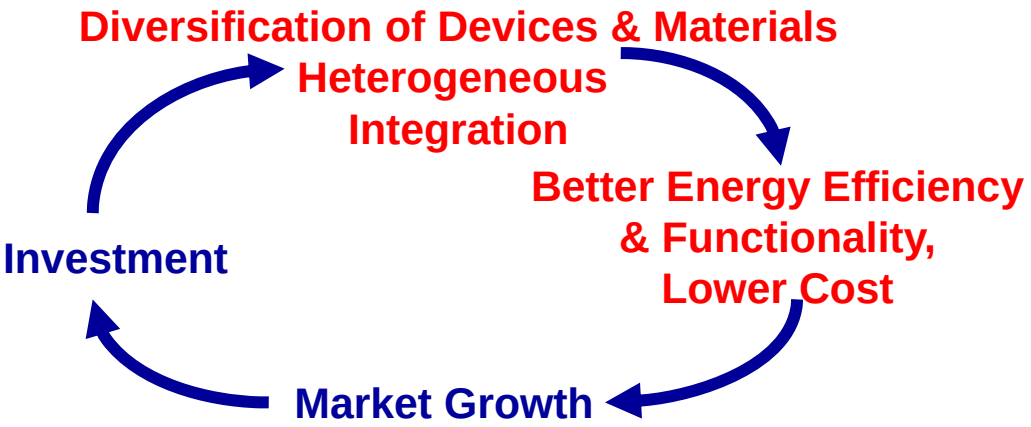
10-yr project, started 15 Sep 2010

- **Theme I: Nanoelectronics** (Prof. Eli Yablonovitch)
- **Theme II: Nanomechanics** (Prof. Tsu-Jae King Liu)
- **Theme III: Nanomagnetics** (Prof. Jeffrey Bokor)
- **Theme IV: Nanophotonics** (Prof. Ming Wu)

Contra Costa-UC Berkeley-MIT-LATTC-Stanford-Tuskegee

A Vision of the Future

J. Rabaey
ASPDAC'08

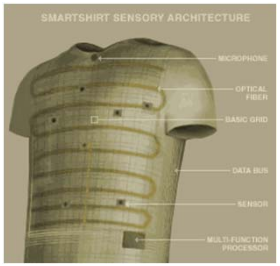


Information technology will be

- **pervasive**
- **embedded**
- **human-centered**
- **solving societal scale problems**

Philips

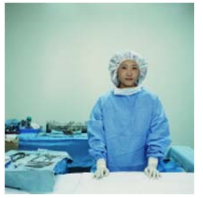
Sensatex



Transportation

Energy

Health care



Environment

Disaster response