**UNIVERSITY OF CALIFORNIA**

**College of Engineering**

**Department of Electrical Engineering and Computer Sciences**

EE 130/230M Prof. Liu & Dr. Xu

Spring 2013

**NMOSFET Design Project**

Due at 5:00PM PDT on Friday May 10, 2013

**Introduction**

In this project, you will use semiconductor device simulation software (Synopsys’ Sentaurus package) to design an n-channel silicon MOSFET with gate length *L*G = 25 nm (relevant for the “20 nm generation” of CMOS technology) to meet specified performance requirements within some practical design constraints. The simulator represents the transistor structure as a mesh of points, keeping track of the material properties and net dopant concentration (within a semiconductor material) at each point and self-consistently solving the Poisson equation and continuity equations to find the mobile charge carrier (electron and hole) concentrations, electric field, electric potential and current flow at each point. Analytical models are used to calculate the effective mass and carrier mobilities, and to account for phenomena such as band gap narrowing, generation-recombination, band-to-band (Zener) tunneling and velocity saturation. For a specified device structure and operating conditions (*i.e.* bias voltages and temperature), then, it can derive the terminal currents. If the device structure is described in only two dimensions (as is the case for this project), then the simulator assumes that the device width (*i.e.* the width of the MOSFET channel) is 1 micron.

MOSFET Structure

The channel region and “body” of the MOSFET are uniformly doped p-type, with dopant concentration ***N*A**. To mitigate the short-channel effect, the MOSFET structure comprises shallow n-type source/drain “extension” regions adjacent to the channel region; to mitigate parasitic series resistance, deeper and more heavily doped junctions are used in the regions where metallic contacts are made to the source and drain.

In practice, the n-type source/drain extension (SDE) regions are formed by implantation of dopants into the Si; the gate electrode blocks this implant from reaching the channel region, so that the SDE regions are naturally aligned to the gate electrode edges. The SDE junction depth ***X*J** is determined by the implantation energy and post-implant thermal annealing conditions. (Annealing at a high temperature – typically greater than 900 degrees Celsius – is necessary to repair the implantation-induced damage to the crystalline lattice, such that dopant atoms reside on Si lattice sites.) Due to lateral “straggle” inherent to the implantation process, and dopant diffusion during the high-temperature annealing step, the channel length *L* is slightly smaller than the gate length *L*G; **the deeper *X*J is, the smaller *L* is**. The deep n+ source/drain regions are also formed by implantation of dopants (but at a higher energy and dosage than used to form the SDE regions), after the formation of dielectric (SiO2 and/or Si3N4) “spacers” of length ***L*SP** along the sidewalls of the gate electrode. The spacers serve to block this implant so that the deep source/drain regions are offset from the channel region. The longer *L*SP is, the longer the length of the SDE regions (which have higher resistivity than the deep source/drain regions).

Fixed Design Parameters

Values for the following transistor parameters are fixed (*i.e.* you will not be allowed to adjust them), based on the *International Technology Roadmap for Semiconductors, 2011 Edition* (Process Integration, Devices, and Structures Chapter) which is available online at <http://www.itrs.net/Links/2011ITRS/Home2011.htm>

* Gate length *L*G = 25 nm
* Effective oxide thickness *T*oxe = 0.9 nm
* For EE130: gate work function = 4.28 eV (corresponding to aluminum)

For EE230M: gate work function = 4.5 eV (corresponding to titanium-nitride)

* Deep source/drain regions:
	+ Dopant concentration *vs*. depth profile is Gaussian
	+ Peak dopant concentration = 2×1020 cm-3
	+ Junction depth (defined as the distance from the Si surface to the depth where the deep source/drain dopant concentration is equal to the body dopant concentration) = 25 nm
* Source/drain extension regions:
	+ Dopant concentration *vs*. depth profile is Gaussian
	+ Peak dopant concentration = 9×1019 cm-3

The power supply voltage *V*DD = 0.8V. The body bias voltage *V*B = 0 V.

**Design Task**

Your assignment is to co-optimize the channel/body dopant concentration *N*A, SDE junction depth *X*J, and spacer length *L*SP to meet the following MOSFET performance specifications:

For EE 130 - low operating power design:

* *I*OFF ≤ 1 nA per micron channel width.
* *I*ON ≥ 400 A per micron channel width.

For EE 230M - low standby power design:

* *I*OFF ≤ 10 pA per micron channel width.
* *I*ON ≥ 200 A per micron channel width.

with the following practical design constraints:

* 5×1017 cm-3 ≤ *N*A ≤ 4×1018 cm-3
* 10 nm ≤ *L*SP ≤ 35 nm
* 4 nm ≤ *X*J ≤ 20 nm

*I*ON is defined to be *I*DS for *V*GS = *V*DS = *V*DD. *I*OFF is defined to be *I*DS for *V*GS = 0 V & *V*DS = *V*DD.

Larger *I*ON provides for faster (or higher frequency) circuit operation, while lower *I*OFF provides for lower static power consumption; therefore, a high *I*ON/*I*OFF ratio is generally desirable. You should explore the trade-offs between *I*ON and *I*OFF by simulating the transfer characteristic (*I*DS *vs*. *V*GS curve) for different combinations of values for the three design parameters:

* Increasing *N*A increases *V*T and hence reduces *I*OFF (unless *N*A is so large that band-to-band tunneling at the drain junction becomes significant) but degrades the effective mobility and hence *I*ON.
* Smaller *X*J depth helps to reduce the short-channel effect and hence *I*OFF but results in larger parasitic series resistance and hence degrades *I*ON.
* Longer spacers help to reduce the influence of the deep source/drain regions on the channel region but result in larger parasitic series resistance.

**Design Report [80 points]**

For your finalized MOSFET design:

1. [20 pts] Illustrate your MOSFET design, labeling and indicating your values for the design parameters. Describe the process (in a paragraph) by which you arrived at your final design.
2. [20 pts] Run the *I*DS-*V*GS simulation for *V*DS = 50 mV (corresponding to the linear region of operation) and for *V*DS = *V*DD (corresponding to the saturation region of operation) and **plot the *I*DS-*V*GS curves for 0 ≤ *V*GS ≤ *V*DD.** Manually extract the following performance parameters from the simulation outputs:
* Minimum subthreshold swing, *S*.
* Linear threshold voltage (*V*Tlin), defined as the value of *V*GS corresponding to *I*DS = 100nA·*W*/*L*G = 4 A for *V*DS = *V*Dlin = 50 mV.

(Note that the saturation threshold voltage (*V*Tsat), defined as the value of *V*GS corresponding to *I*DS = 100nA·*W*/*L*G = 4 A for *V*DS = *V*DD, is automatically extracted for you by the simulation package.)

* Drain-induced barrier lowering, in units of mV per Volt, defined as

$$DIBL={\left(\left|V\_{Tlin}\right|-\left|V\_{Tsat}\right|\right)}/{\left(V\_{DD}-V\_{Dlin}\right)}$$

**Summarize your MOSFET design and performance parameters in tabular format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| ***N*A**[cm-3] | ***X*J**[cm-3] | ***L*SP**[cm-3] | ***I*ON** [A/m] | ***I*OFF** [A/m] | ***S***[mV/dec] | **DIBL** [mV/V] |
| <designed value> | <designed value> | <designed value> | <simulated value> | <simulated value> | <simulated value> | <simulated value> |

1. [20 pts] Run *I*DS-*V*GS simulations with *V*DS = *V*DD (corresponding to the saturation region of operation), for gate length values ranging from 20 nm to 100 nm. Manually extract the saturation threshold voltage (*V*Tsat) for each simulated curve and **plot *V*Tsat *vs*. *L*G for 20 nm ≤ *L*G ≤ 100 nm** to see the short-channel effect.
2. [20 pts]Run *I*DS-*V*DS simulations for *V*GS = 0.5 V, *V*GS = 0.6 V, *V*GS = 0.7 V, and *V*GS = 0.8 V and **plot the *I*DS-*V*DS curves for 0 ≤ *V*DS ≤ *V*DD**. Does your designed MOSFET exhibit a square-law dependence of saturation current on *V*GS? **Explain briefly.**

**Design Project Presentation (for EE 230M students only) [20 points]**

Students taking EE 230M are required to give a short (~10 minute) presentation covering every section of the design report, on May 9th during the regular lecture timeslot (11AM to 12:30PM). All students in EE 130 and EE 230M will be welcome to attend and ask questions. Scoring of the presentation will be based on the following elements:

* Quality of presentation (organization and clarity of slides, clarity and length of oral delivery) [10 pts]
* Ability to answer questions clearly and correctly in a timely manner [10 pts]