UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Final Exam	**EECS 247**
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Name: _____

SID: _____

Total number of pages:_____

Score: **/60**

Problem 1 6	Problem 2 6	Problem 3 10	Problem 4 10	Problem 5 28	Total Score 60point

- **Closed books and class notes, no calculators/computers/PDAs**
- **Mark all final and intermediate results clearly**
- Write solutions on the exam sheets. Add extra pages where needed.
- Simplify algebraic results as much as possible.
- Bring into standard form where applicable, show your work.

Useful Expressions:

$log_{10}\,2=0.3,$ $log_{10}\,3=0.477,$ $log_{2}\,3=0.1.59$

$2^{1/2}=1.41$ $3^{1/2}=1.73$

Problem 1:

Consider three ways to use 64 nominally identical 0.1pF capacitors and a single reference voltage to build a DAC with analog full-scale output voltage 0V to Vref. Conversion consists of one initialization cycle followed by one voltage division or charge redistribution cycle. Capacitors may be connected in parallel groups or otherwise to achieve the desired results. Please do not draw every C and switch. Draw only enough number of components to illustrate the concept. Indicate which architecture is sensitive to parasitic capacitor, assuming capacitors have parasitic capacitance only on the bottom plate. Discuss pros and cons of each scheme in terms of performance and complexity of analog and digital circuits required.

a- Show a 5-bit DAC using a minimum number of switches.

b- Show how to use the capacitors to achieve a 5-bit DAC which is monotonic regardless of any single capacitor ratio error.

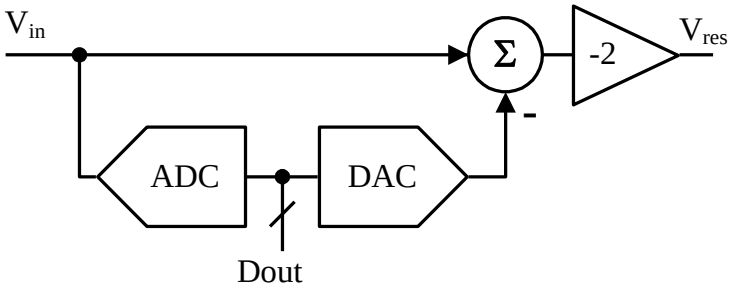
c- How do we use two identical capacitor arrays plus one additional capacitor C_z , to build a 10-bit DAC with monotonic performance regardless of any single capacitor ratio error?

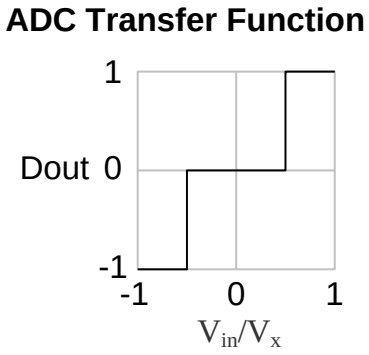
Problem 2. A segmented DAC comprises a unit-element MSB DAC with 5 bits and a binary-weight LSB DAC with 4 bits. The MSB and LSB DAC unit-elements are of the same size, however, since the LSB DAC elements are located in the periphery of the lay out array; they tend to have poorer matching compared to MSB DAC elements. The standard deviation of the unit elements associated with the MSB and LSB DACs are σ_1=1% and $\sigma_2=\sqrt{3}\,\sigma_1$ respectively.

a) Find the standard deviation for the maximum overall DAC DNL (σ_{DNL}).
b) For a product yield of 99.7% (3σ) what is the correct number for the DNL to appear in the product date sheet assuming there are no other non-idealities affecting DNL?

Problem 3:
The single stage of a pipelined ADC is shown below. Assume that the sub-DAC is ideal.

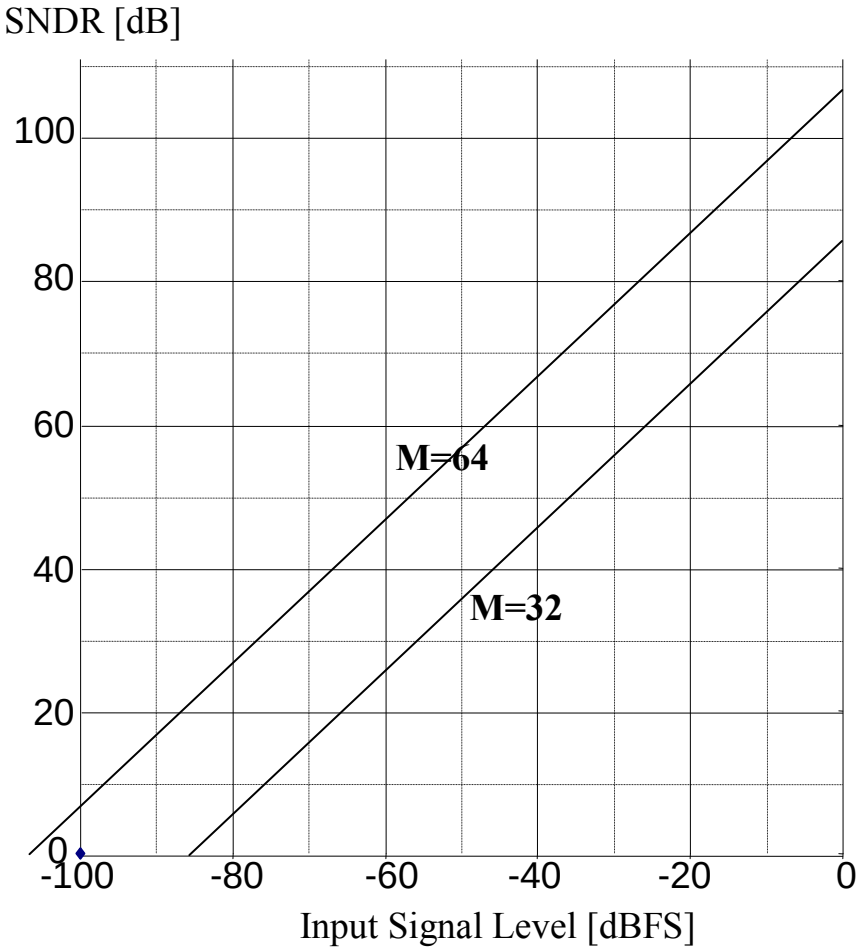
a) How many comparators does each sub-ADC use? What is the raw number of bits per stage? What is the effective number of bits?
b) What is the resolution of a pipelined ADC that uses 9 such stages (the final stage has one less comparator)? What is the overall latency if the stages are designed for minimum delay-per-stage? What is the maximum through-put?
c) On the graph paper provided below, plot the residual voltage V_{res} as a function of the stage input $V_{in}./V_x$
d) What is the maximum input voltage as a function of V_x for this converter that does not result in overloading?
e) What is the maximum tolerable comparator offset? Show your derivation on the graph.
f) Draw the block diagram of an ADC that uses three such stages. Indicate how the digital data from each stage must be scaled to obtain the converter output D_{out}^{Total}.
g) How does offset associated with the last stage comparator affect the converter's quantization error for the ADC in part (f)? What is the resulting conversion error in terms of LSB for a Vx/4 error in the sub-ADC threshold of the last stage, assuming input full-scale is 2Vx?





Problem 4:

The two lines drawn on the graph below indicate the theoretical ideal performance (SQNR) of a low-pass Sigma-Delta ADC with 1-bit digital output to be filtered by a digital filter.



a) Based on the dynamic range difference between the two different oversampling ratios, find the order of the Sigma-Delta ADC. In the two cases, the signal bandwidth is kept constant, the sampling frequency is varied.
b) Name three architectural approaches for the design of this ADC.
c) Choose the architecture which is unconditionally stable and has lower sensitivity to the level of matching of analog/digital blocks. Draw the sampled-data type block diagram.
d) Derive the output of the ADC as the function of input signal and quantization noise at the point of insertion. Note that you may have to use extra delay operators as well as differentiators when combining digital outputs to obtain the final output.
e) What is the analytical expression for the in-band dynamic range (peak signal-to-quantization noise ratio, SQNR) at the output Y(z) as a function of the oversampling ratio, $M=fs/f_N$?
f) Draw the switched-capacitor implementation of the architecture chosen for part c) using bottom-plate type integrators. You can use opamps and comparators & summing circuits at the block diagram level.
g) This ADC is intended to be used at the oversampling ratio of 64. The designer claims the capacitor sizes are chosen such that for the oversampling ratio of M=32, the in-band noise level is at -8dB lower compared to theoretical in-band quantization noise. How

would the thermal noise affect the SNDR curve associated with M=64? Discuss the derivation and draw the curve on the graph above.

h) If the ADC is used at the lower oversampling rate of M=32 do you expect any issues? Explain. What about operating at M=64?

i) Modify the graph for a more realistic SNDR curve for input signal levels close to 0dB for the case of M=64. What aspects of the building blocks performance could affect/limit the peak SNDR?

j) Assuming the signal bandwidth of interest is 10kHz what is the minimum order for the anti-aliasing prefilter required to suppress the out-of-band signal/s aliasing down to the band of interest to at least the same level as in-band noise? Make the following assumptions:

- Incoming signal has equal signal strength across the entire frequency band.
- The anti-aliasing filter corner frequency is 20% higher than bandwidth of interest.
- The filter type is chosen such that it has a roll-off rate of 20dB-per-decade-per-pole.
- The peak SNDR of the ADC considering all impairments is expected to be 80dB.

k) The minimum signal handling capability of a Sigma-Delta type ADC is limited by (name as many effects as possible):

Problem 5:

Please answer the following questions: In the case of ***True/False*** underline either True or False. In the case of _____ fill in the blank.

1. For low-frequency applications such as voice-band telephony (4KHz signal bandwidth) which filter architecture is more commonly used: Switched-capacitor or Continuous-time? In a few words explain why?

2. A bandpass filter with overall Q=10 is built by: (choose one)
   a. Cascade of biquads
   b. Direct conversion of RLC ladder filters to integrator-based structures

   Explain why?

3. In the design of switched-capacitor filters, T-networks are used when _____(complete the sentence). What is the advantage?

4. An otherwise perfect ADC has one missing code. What is the DNL & INL for this converter? Is the necessarily non-monotonic?

5. The INL of a DAC is a function of whether it is binary-weighted or unit-element**.** ***True or False***

6. Name the ADC architecture/s more appropriate for very high-resolution (20bit) applications and explain why briefly.

7. Name the ADC type suitable for measuring DC signals with accuracies in the order of 18 bits.

8. Explain the advantages of using clock boosting in CMOS switches. What are the necessary precaution/s?

9. Advantage of bottom plate sampling in the context of switched-capacitor filters_____ ,and in the area of Track & Hold circuitry is _____.

10. What aspect of Flash ADCs is improved by using Gray encoding?

11. Six identical Flash ADCs each with a sampling frequency of 4Gsample/sec and 5bit resolution are time-interleaved, what is the effective overall Nyquist based signal bandwidth this ADC can handle? What is the overall number of bits?

12. What is the advantage of using interpolation in ADC converters?

13. Name one requirement for interpolative converter preamplifiers.

14. One side-benefit of interpolative converters is improved DNL***. False or True?***

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16. How is the number of components in flash ADCs related to resolution?

17. How is the number of components in pipelined ADCs related to resolution?

18. Name the reason/s for using interstage gain in pipeline ADCs.

19. In a pipelined ADC what would be the trade-offs considered in the choice of number of bits/stage?

20. Comment on the anti-aliasing filter requirements for Nyquist rate ADCs versus oversampled ADCs assuming the same signal bandwidth.

21. What effect does finite integrator opamp gain have on the performance of a Sigma-Delta ADC?

22. How is the performance of Sigma-Delta ADCs measured? Are DNL and INL measurements meaningful for this type of converters?

23. Underline one of the four answers: In a low-pass Sigma-Delta modulator quantization noise is frequency shaped : ***Lowpass- Bandpass- Highpass- Notch (bandreject)***

24. Underline one of the four answers: In a bandpass Sigma-Delta modulator quantization noise is frequency shaped ***: Lowpass- Bandpass- Highpass- Notch (bandreject)***

25. The theoretical SQNR of a single bit, 4^{th} order bandpass Sigma-Delta modulator is the same as _____order lowpass single bit Sigma-Delta modulator.

26. For a 2^{nd} order lowpass Sigma-Delta modulator, underline the building block with the most stringent performance requirements?
    a. 1^{st} integrator - 2^{nd} integrator - comparator
    Briefly state why.