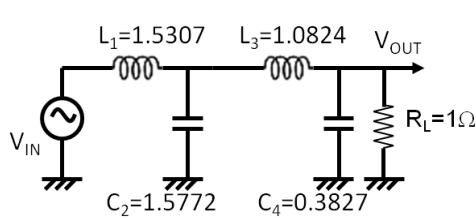

EE247 Analog-Digital Interface Integrated Circuits

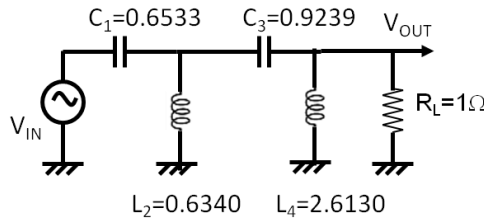
Fall 2010 Homework #2

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Problem 1: Solution



The low pass filter



The high pass version of the filter

(a). The normalized values are obtained as:

$$C_1 = 1/L_1 = 0.6533, \quad C_3 = 1/L_3 = 0.9239, \quad L_2 = 1/C_2 = 0.6340, \quad L_4 = 1/C_4 = 2.6130$$

(b). R is the value of the source and termination resistor and is 10 Ohm now. The -3dB frequency we choose is set to be 50kHz. So we have:

$$L_r = R/\omega_{-3dB} = R/2\pi f_{-3dB} = 3.183 \times 10^{-6} H$$

$$C_r = 1/(R \times \omega_{-3dB}) = 1/(R \times 2\pi f_{-3dB}) = 3.183 \times 10^{-6} F$$

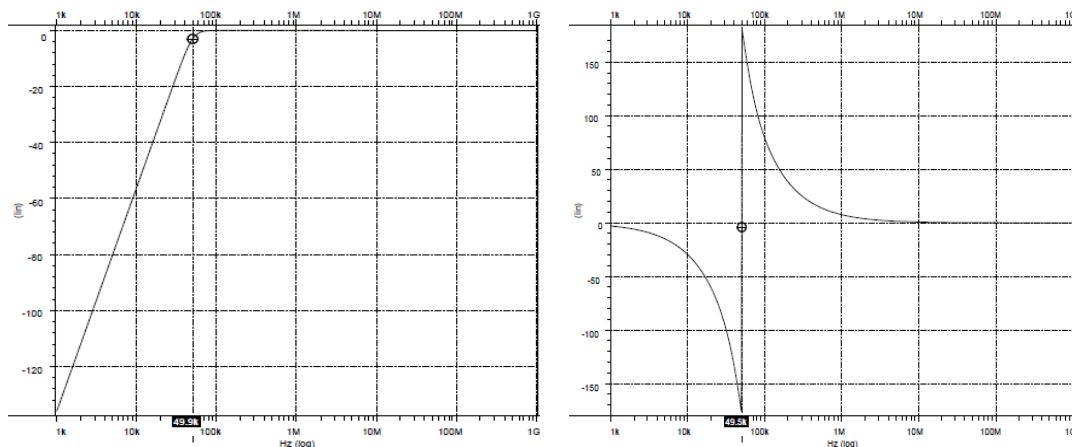
Thus the value of Ls and Cs can be obtained:

$$C_1 = C_r \times C_{norm,1} = 2.08 \times 10^{-6} F, \quad C_3 = C_r \times C_{norm,3} = 2.94 \times 10^{-6} F$$

$$L_2 = L_r \times L_{norm,2} = 2.018 \times 10^{-6} H, \quad L_4 = L_r \times L_{norm,4} = 8.317 \times 10^{-6} H$$

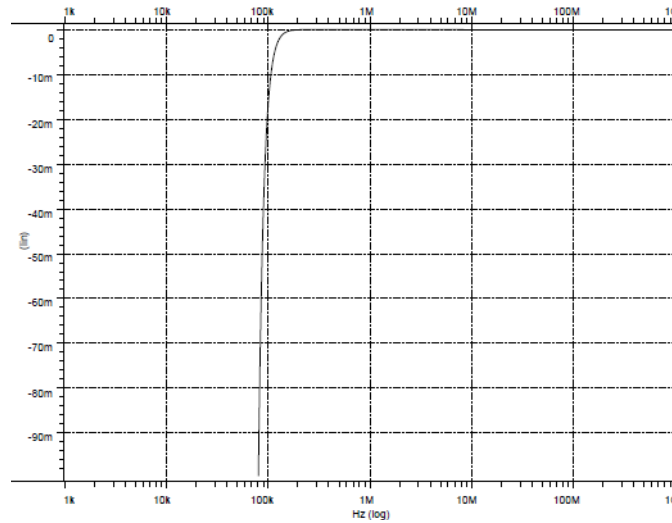
(c). The SPICE file is shown in Appendix-A:

The simulated results are shown below, with both the magnitude response and the phase response:



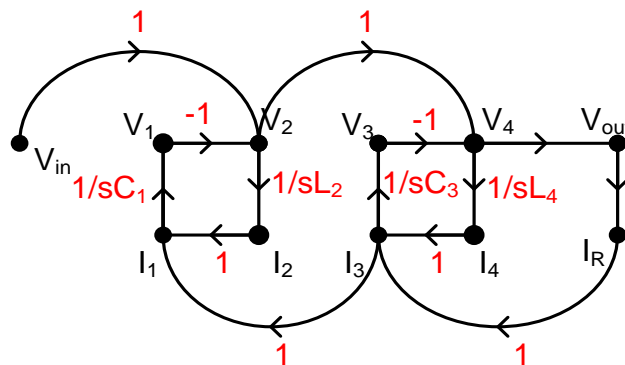
The selected point is at -3.03dB at 49.9kHz. Ideally at -3dB, the corresponding frequency should be a little bit lower but is still approximately at around 50kHz.

(d). The pass-band is shown as below:

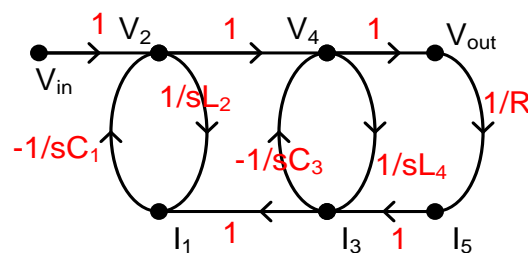


From the pass-band configuration, there's no ripple in pass-band and also no stop-band zero, so that it should be high pass Butterworth type.

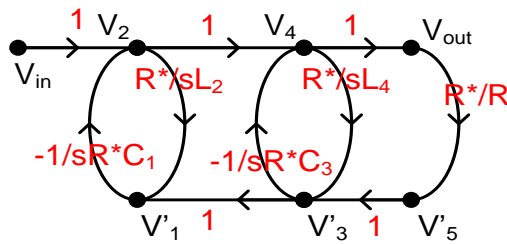
(e). The Signal Flow Graph can be obtained by setup the BMF of each node.



We do some simple simplification to the figure and set BMF directly between I1 and V2, between I3 and V4.

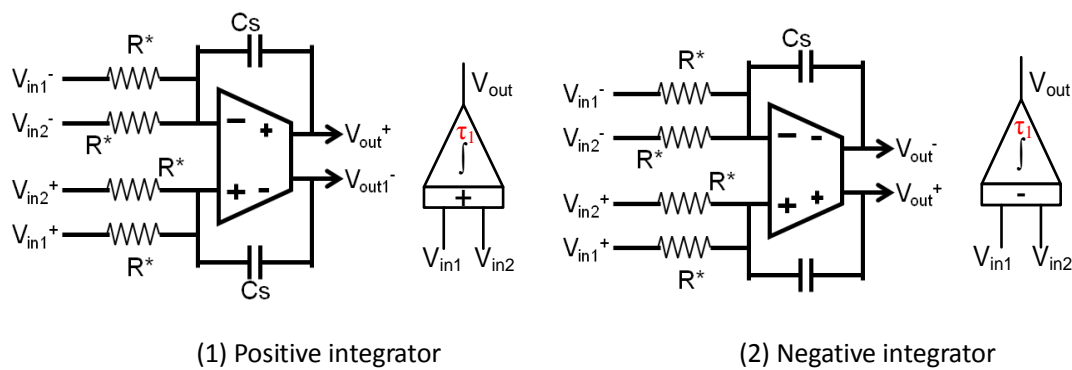


Then, we multiply an arbitrary resistance R^* (here set as 10 Ω) to the current node and also modify the BMF relating to the relevant nodes, the SFG changes to:

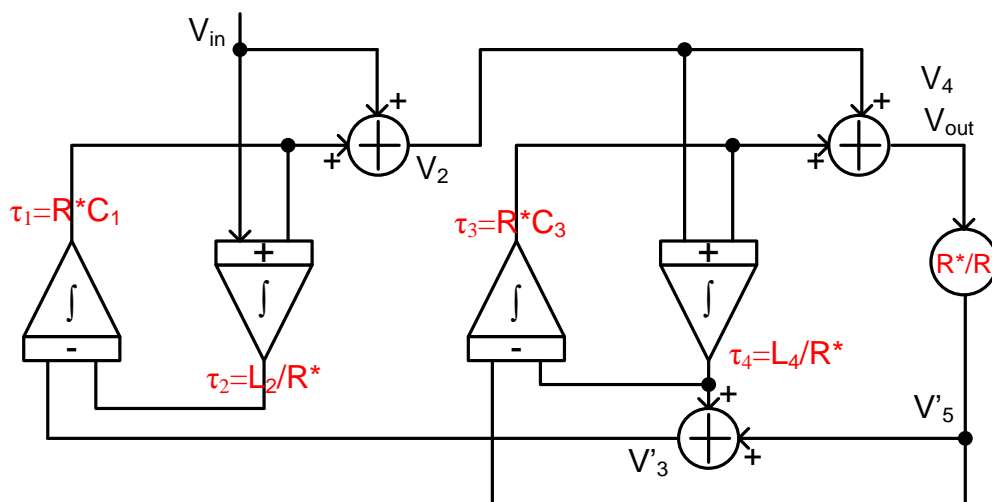


This kind of structure can be realized by Opamp-RC based integrator with different time constant.

(f). Then, we choose the integrator to simulate the RLC network. We use differential Opamp-RC based integrator to realize the different signs. We set the basic differential integrator structure as shown in the figure below, in which we have both the positive and negative integrator:

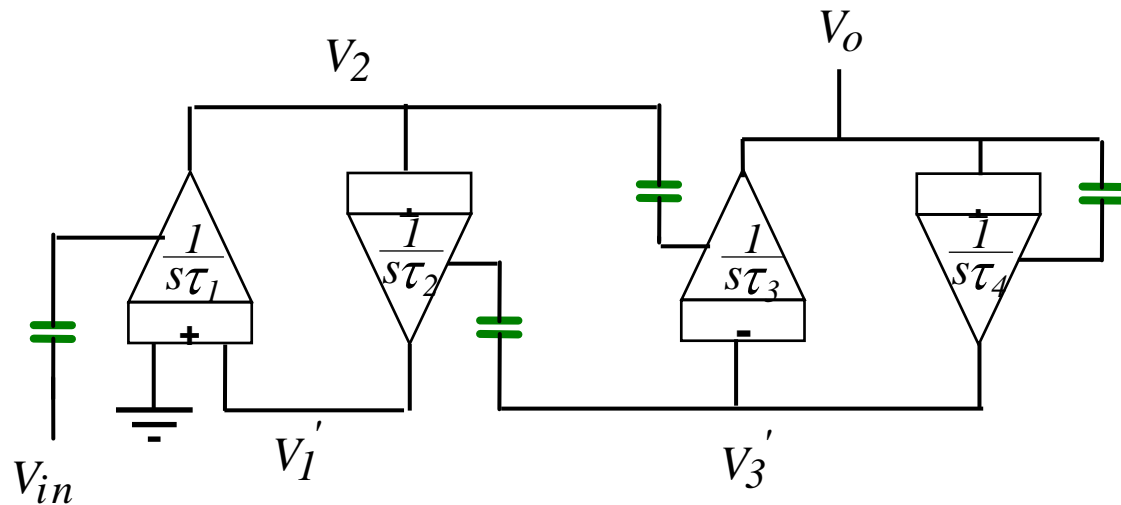


The above integrators implement $V_{out} = \text{Integration}(V_{in1} + V_{in2})$ and $V_{out} = -\text{Integration}(V_{in1} + V_{in2})$, respectively. Furthermore, C_s is just given in the previous SFGs. The integrator-based schematic is shown in the figure below:

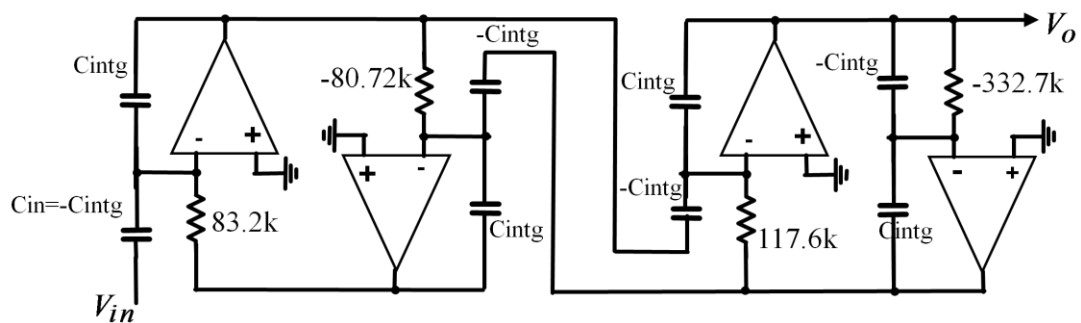


Added by H.K.

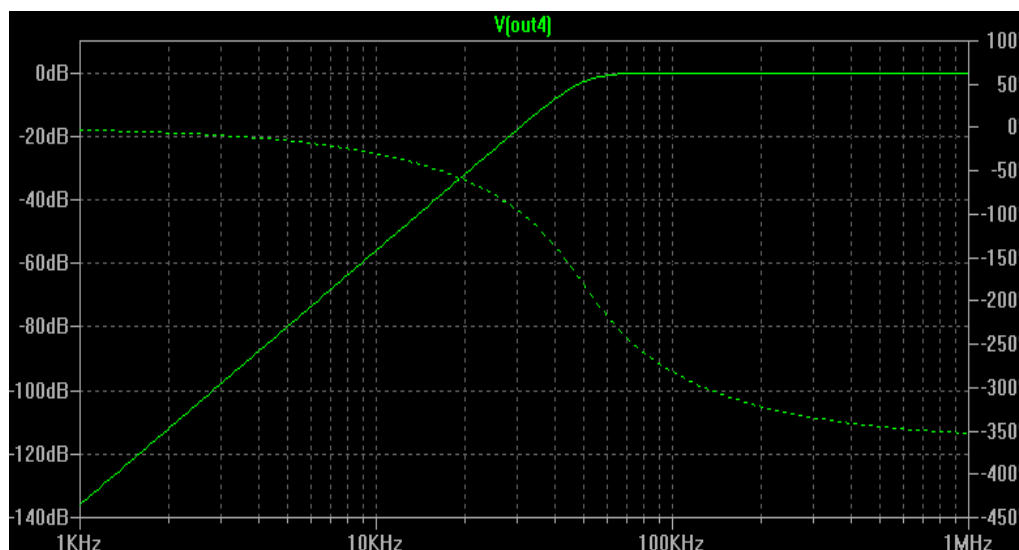
Note that one way of avoiding use of extra opamps is to use capacitors for the requiring summing functions:



The actual implementation then is:

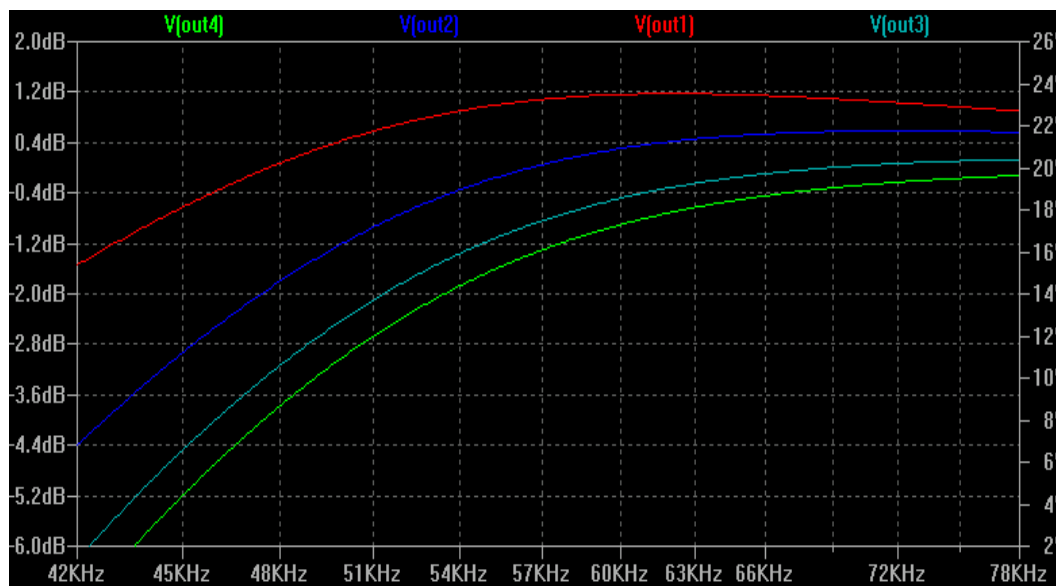


c) Magnitude and phase response:



Since in one decade seems that there 20dB/per_pole attenuation (80dB/decade) and also the passband seems to be maximally flat, the filter is most probably Butterworth type.

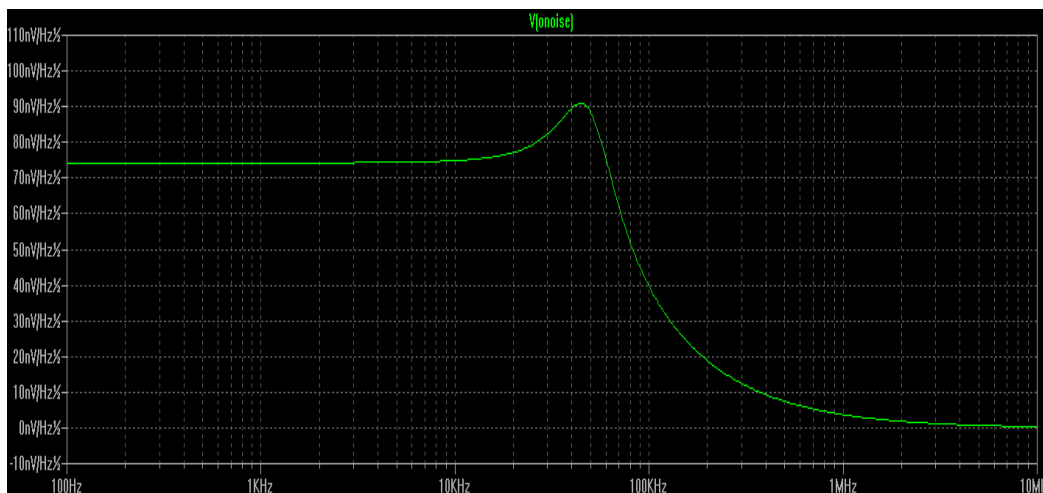
h) In this implementation the internal node magnitude responses are:



The output of the 1st integrator would then be the limiting factor in maximum signal handling capability of this filter. This output has a maximum at 1.2dB above the main output. That is it has a peak about x1.15 above the main output. Input voltage of $0.5V_p / (1.15) = 0.435V_p$ would result in the 1st integrator output to be at the verge of clipping. Since the gain from input to output is 1, this translates to maximum output voltage of $0.435V_p$ or $0.31V_{rms}$.

The maximum signal handling capability can be improved by using node scaling that is scaling the internal integrator output nodes down to a level equal or smaller that the maximum level at the output node.

i) Noise analysis result in term of noise spectral density is shown below.



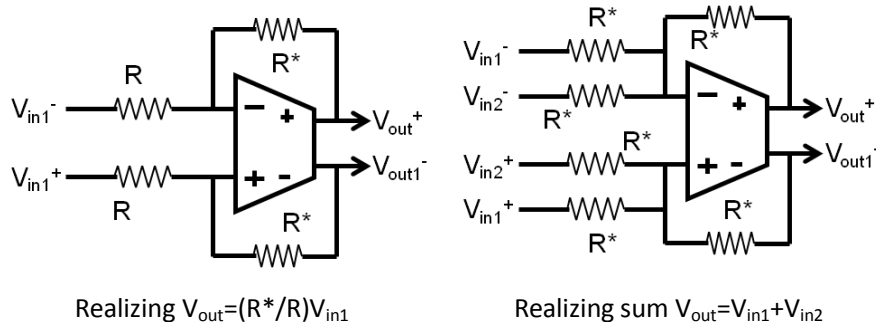
with total integrated output referred noise given by SPICE as:

`INTEG(v(onoise))=2.57125e-005 FROM 100 TO 1e+007`

This give a dynamic range $DR=20\log(0.31V_{rms}/25.7\mu V)=81.63dB$

End H.K. comments

In which we also implement the sum structure to obtain some voltage values as well as the ratio structure to realize R^*/R amplitude shift.



Thus, based on the structures provided before, we can implement the RLC filter with Opamp-RC based Integrator.

(g). previously we set $R^*=10\Omega$. When we choose all the integrator capacitor to be 25pF, we have to change the resistors in order to match the same time constant.

$$\tau_1 = C_1 R^* = 2.08 \times 10^{-6} s, @ C_1 = 25 pF, R = 83.2 k\Omega$$

$$\tau_2 = L_2 / R^* = 2.018 \times 10^{-6} s, @ C_2 = 25 pF, R = 80.72 k\Omega$$

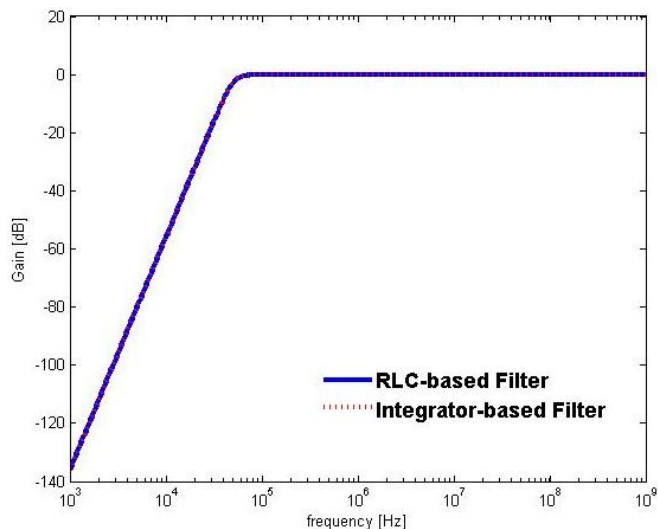
$$\tau_3 = C_3 R^* = 2.94 \times 10^{-6} s, @ C_3 = 25 pF, R = 117.6 k\Omega$$

$$\tau_4 = L_4 / R^* = 8.317 \times 10^{-6} s, @ C_4 = 25 pF, R = 332.7 k\Omega$$

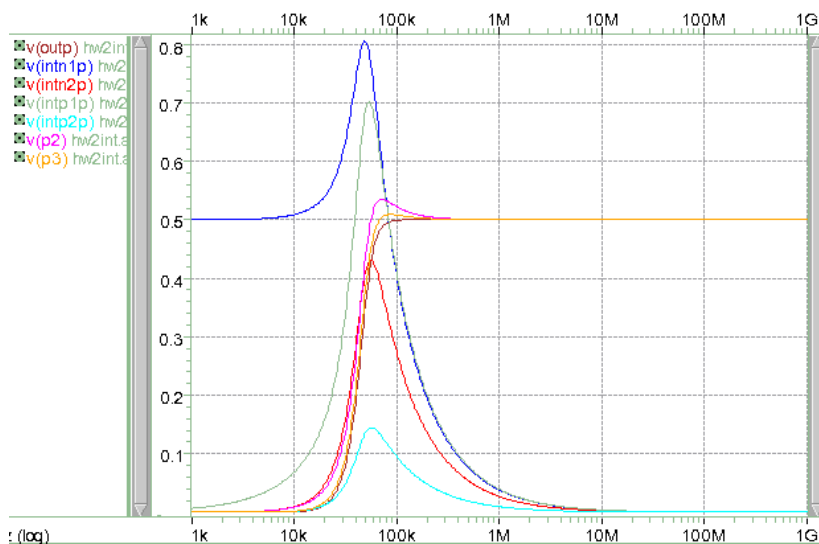
Therefore, the value of the resistor is determined.

(h). Choose the Opamp to be ideal and so that virtual ground can be used in analyzing the circuit.

Therefore, we can simulate the results as shown below:



The red dotted line is the Opamp-RC filter and the blue solid line is the RLC filter, which are almost the same. In order to find the limiting point in the voltage ranging in the circuit, we plot the AC response for all the nodes (half range).



(i) The noise can be obtained also from simulation.

```
**** total output noise voltage = 2.237e-04 volts
**** total equivalent input noise = 11.1035
```

The total noise is measured on one of the output node, under the worst case, the differential output noise would be $\sqrt{2} \times 2.237e-4 = 3.16e-4$ Volts.

Note by H.K.

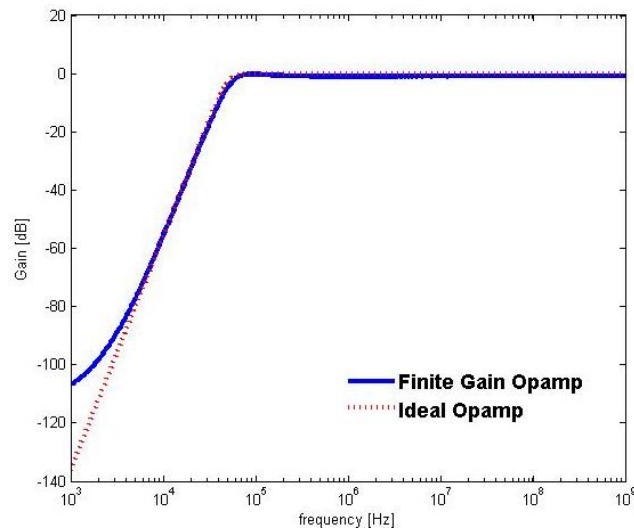
Noise has turned out to be much higher than expected. Could be due to use of the summing amplifiers with the extra resistors.

End note

. The Dynamic Range can be obtained as:

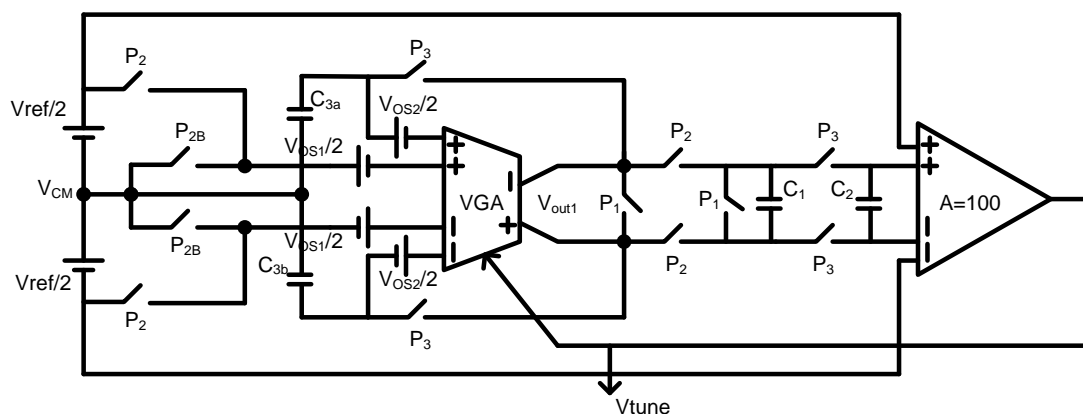
$$DR = 20\log(V_{sig}^{rms}/V_{noise}^{rms}) = 20\log(220mV/316\mu V) = 56.85dB$$

(j) With finite 50 gain of the amplifier, the shape of the magnitude response becomes:

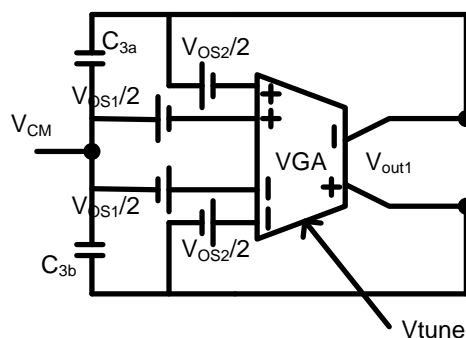


We can see that when the Gain of the Op-amp decreases, the stop-band becomes worse and the transition band has ripples, this is probably due to the decrease in Q of the system. Also, the pass-band value is also slightly smaller than the ideal case, which is caused by the signal attenuation induced by finite Op-amp gain.

Problem 2: Solution



(a) The schematic view of the circuit is shown above, in which the switching MOSFET are simplified by simple switches. Under P3 high, P1 and P2 are both low and P2B is high, therefore, we can draw the equivalent circuit below:



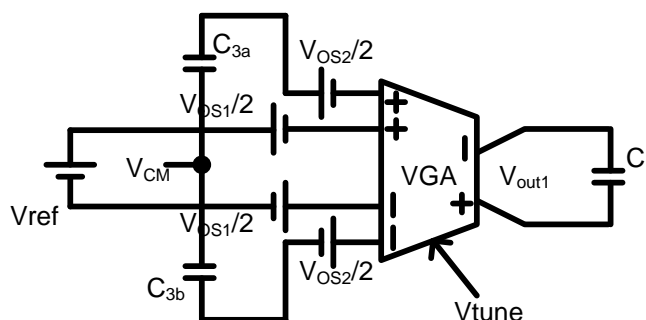
Assuming that the capacitor C_{3a} and C_{3b} don't have initial charge, so that the circuit satisfies the equation:

$$(-V_{OS1})A_{main} + (-V_{out1} - V_{OS2})A_{aux} = V_{out1} \Rightarrow V_{out1} = \frac{-V_{OS1}A_{main} - V_{OS2}A_{aux}}{1 + A_{aux}}$$

Since G_m of A_{aux} is $1/5$ of the main amplifier, thus we can assume that $A_{main} = 5A_{aux}$. Besides, we have both A_{aux} and A_{main} far larger than 1. So we have:

$$V_{out1} \approx -5V_{OS1} - V_{OS2} = -20mV + 10mV = -10mV$$

(b) When P_2 is high, the amplifier is in evaluation state and the equivalent circuit is as follow:

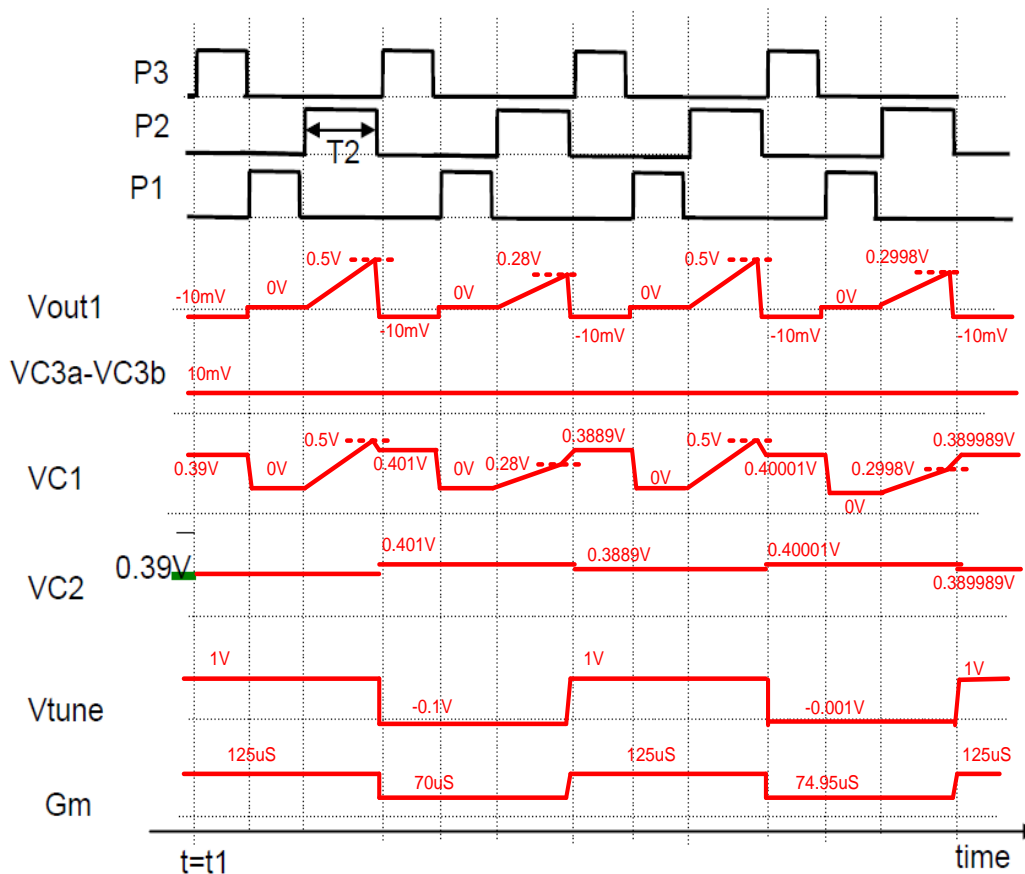


After P_3 , the V_{out1} is stored on C_{3a} and C_{3b} , so that the new output voltage is:

$$\begin{aligned} V_{out1} &= (V_{ref} - V_{OS1})5A_{aux} + (-V_{cap} - V_{OS2})A_{aux} \\ &= 5V_{ref}A_{aux} + (-5V_{OS1} - V_{OS2})A_{aux} + (5V_{OS1} + V_{OS2})A_{aux} \end{aligned}$$

In which V_{cap} is the voltage stored on C_{3a} and C_{3b} in P_3 . Therefore, we can see that the caps can cancel both the offset voltage from the main amplifier and the auxiliary amplifier.

(c) The schematics are listed below:



Here we made some simple analysis. In P3 (Offset Cancellation Stage), we just assume that the charge sharing is undergoing for C1 and C2, in which they satisfies:

$$C_1 V_{out1} + C_2 (V_{C2} [n-1]) = (C_1 + C_2) (V_{C2} [n])$$

On the other hand, the output of VGA is -10mV as calculated before due to the offset voltages and this voltage will store on C3a and C3b, and the voltage on C3a and C3b should always to 10mV to cancel the offset voltage.

In P1 (Pre-charge Stage), however, output of VGA goes to zero, and the voltage on C1 also goes to zero. Then in P2 (Evaluation Stage) the circuit is in evaluation step, and the C1 is charged by the voltage-tuned integrator that is determined by V_{tune} from the output of the final amplifier. Furthermore, regarding the impact of V_{tune} , it will increase the Gm of the main amplifier and make the initial charge on C1 larger and larger, until to the point that the voltage on C2 is equal or larger to V_{ref} . In P2, the evaluation current is:

$$I_{REF} = V_{REF} G_{main} = 0.4 \times (75 \times 10^{-6} + V_{tune} \times 50 \times 10^{-6})$$

V_{tune} is initially assumed to be in saturation 1V since normally at the beginning the settling is

not completely finished and the discrepancy is the largest. Then, since $T_2=10ns$, then at the end of P2, the voltage on C1 will linearly go to:

$$V_{P2} = \frac{I_{REF} T_2}{C_1} = \frac{0.4 \times (125 \times 10^{-6}) A \times 10 ns}{1 pF} = 0.5V$$

Then, repeat these steps and we can obtain the data on the figure.

(d) no, actually the circuit will go to steady in the next cycle.

(e) For steady state, there should no charge transfer from C1 to C2 in P3. So that we have:

$$V_{P2} = \frac{V_{REF} \times G_m \times T_2}{C_1} = V_{C2} = \frac{V_{REF} T_2}{C_1} (75 \times 10^{-6} + V_{tune} 50 \times 10^{-6})$$

$$V_{tune} = 100(0.4 - V_{C2}) = 40 - 100V_{C2}$$

Solve the two equations together and we can obtain: $V_{tune}=0.4762V$, and $V_{C2}=0.3952$. The values are listed in the table below

| Vout1 | $\Delta V_{c3a,b}$ | VC1 | VC2 | Vtune | Gm |
|---------|--------------------|---------|---------|---------|---------|
| 0.3952V | 10mV | 0.3952V | 0.3953V | 0.4762V | 98.81uS |

Therefore, it seems that the circuit is not entirely running at steady state the same to $V_{ref}=0.4V$. Due to the fact that the constant Gm of the main amplifier is 75uS rather than 100uS, the voltage at C2 can only be holding constant under other voltage. However, after all, this circuit can still run at a steady-state.

Appendix-A

```
.OPTIONS post acct
Vin in 0 dc 0 ac 1
C1 in 1 2.08u
L2 1 0 2.018u
C3 1 out 2.94u
L4 out 0 8.317u
RL out 0 1
.AC DEC 100 1 1G
.TF V(out) Vin
.END
```

Appendix-B

```
.options post acct ingold=1
.subckt DiffAmp vip vin vop von % Fully differential Amplifier
Ep vop gnd vip vin 25
En von gnd vin vip 25
.ends

.subckt intg in1p in1n in2p in2n outp outn Rv=1 Cv=25p % Integrator
R1 in1p vp Rv
R2 in1n vn Rv
R3 in2p vp Rv
R4 in2n vn Rv
Xamp vp vn outp outn DiffAmp
C1 outn vp Cv
C2 outp vn Cv
.ends

.subckt sum in1p in1n in2p in2n outp outn % Sum stage
R1 in1p vp 1k
R2 in1n vn 1k
R3 in2p vp 1k
R4 in2n vn 1k
Xamp vp vn outp outn DiffAmp
Ro1 outp vn 1k
Ro2 outn vp 1k
.ends

xp1 inp inn n1p n1n p1p p1n intg Rv=80.72k Cv=25p
xn1 n3 p3 p1n p1p n1p n1n intg Rv=83.2k Cv=25p
xp2 p2 n2 n2p n2n p2p p2n intg Rv=332.7k Cv=25p
xn2 outn outp p2n p2p n2p n2n intg Rv=117.6k Cv=25p
xsum1 inp inn n1p n1n p2 n2 sum
xsum2 p2 n2 n2p n2n outp outn sum
xsum3 outp outn p2p p2p p3 n3 sum

Vin inp inn AC 1
.ac dec 100 1k 1G
.print gain=par('db(2*v(outp))')
.end
```