UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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	Homework 2	**EECS 247**
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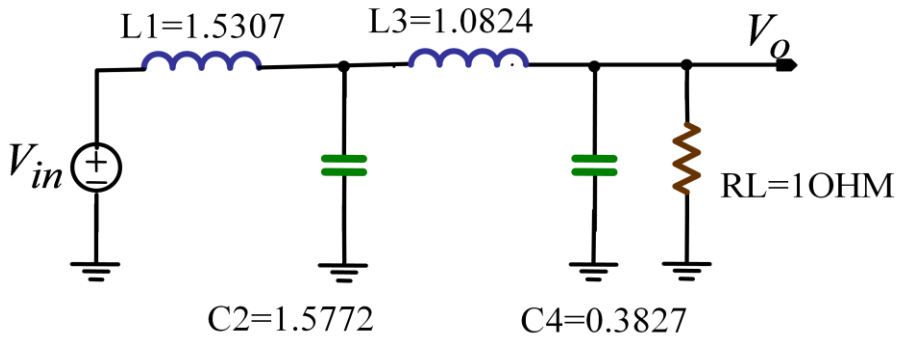
Problem 1:

The figure below shows a 4th order singly-terminated RLC lowpass filter. The normalized lowpass values for Ls and Cs are as indicated on the figure.

a. Draw the **highpass** version of this filter; find the normalized Ls and Cs based on the lowpass values.
b. Find values for Ls and Cs for a -3dB frequency of **50KHz.**
c. Simulate the magnitude response in terms of dB with coarse and fine y-axis. Submit a copy of your SPICE input file and final results.
d. From the shape of the passband, guess the type of the filter (e.g. Chebshev etc).
e. Find the signal flowgraph for this filter intended for integrator-based implementation. Show your work.
f. Draw the schematic for the integrator based version of this filter. Use Opamp-RC type integrators, either single-ended or differential. If you use single-ended structure, then you are allowed to use negative components to facilitate signal sign inversion.
g. Choose all the integrating capacitors to be **25pF**, find values for the integrator resistors.
h. Simulate the magnitude response (both coarse and fine y-axis) for the final integrator based filter. Monitor the response of the all integrator outputs. If the opamp output clips at **+-0.5V** (assuming signal is centered around 0V), which output would determine the maximum input signal for which the output is still viable? Based on this factor, what is the maximum output signal within the band of interest? Explain how can you increase the maximum output signal? Submit a copy of your SPICE input file and final results.
i. Simulate and find the total output noise. Compute the dynamic range using (h).
j. Resimulate the filter this time assume the integrator opamps have finite gain of 50. How does the passband change? Why?
k. What is the optimum unity-gain frequency for the opamp, assuming single opamp pole, to compensate for the impairment in section (i)? Add a pole to the opamp by using VCVS and R and C choose values for R & C accordingly. Prove your calculation result by simulating the magnitude

response with both non-idealities incorporated; submit the detail of the passband. Explain.



Problem 2:

Consider the circuit shown in below (lecture 7). Assume the following:

1. The circuit is turned on and has been operating for enough clock cycles for *VC2=0.39V at t=t1*.
2. *C1= 1pF, C2=9pF, Vref=0.4V*
3. The auxiliary input pair added for offset cancellation purposes has input tranconductance equal to *1/5* compared to the main input tranconductance. The DC gain ($g_m x r_o$) associated with both main and auxiliary is >>1
4. In this example, the main input has an input-referred offset voltage (V_{os1}=*4mV*) while the auxiliary input has an offset voltage of (V_{os2}=*-10mV*), for simplicity, assume offset referred to the input appears on the both set of inputs as a differential signal (pay attention to the polarity of the voltage source shown in the figure below).
5. *T2=10nsec*, and P2B denotes inverted P2.
6. Use the following expression for the integrator transconductance: $Gm=75x10^{-6}[A/V]+(Vtune.(50x10^{-6}[A/V^2]))$
7. Assume amplifier A has a gain of 100 (Vtune=100xVin) and the output saturates at Vtune=1V . That is:

   Vtune =1V for Vin >10mV
   Vtune=100xVin for Vin <10mV
   Note that *Vin=Vref-VC2*

a- Compute Vout1 during the time that P3 is high.
b- Determine whether the voltage stored on Vc3a,b cancels one or both offset components. Try to prove your point.
c- Fill in the diagram shown below for four cycles starting at *t=t1 (VC2=0.39V)*. Pay attention to charge conservation during charge sharing between the capacitors *C1 & C2*. Show values for: Show values for *Vout1,*

(VC3a-Vc3b), VC1, VC2, Vtune, and *Gm* for four cycles starting *t=t1* on the diagram provided.

d- Is the circuit close to steady-state at the end of the fourth cycle?

e- Compute the value for the above voltages and *Gm* in steady-state. Note that for simplicity the lowpass filter typically appearing at the output of the amplifier A has been eliminated. Thus, if you attempt simulating this circuit, it is likely that *Vtune* would not reach steady state and will oscillate.