UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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	Homework 3	**EECS 247**
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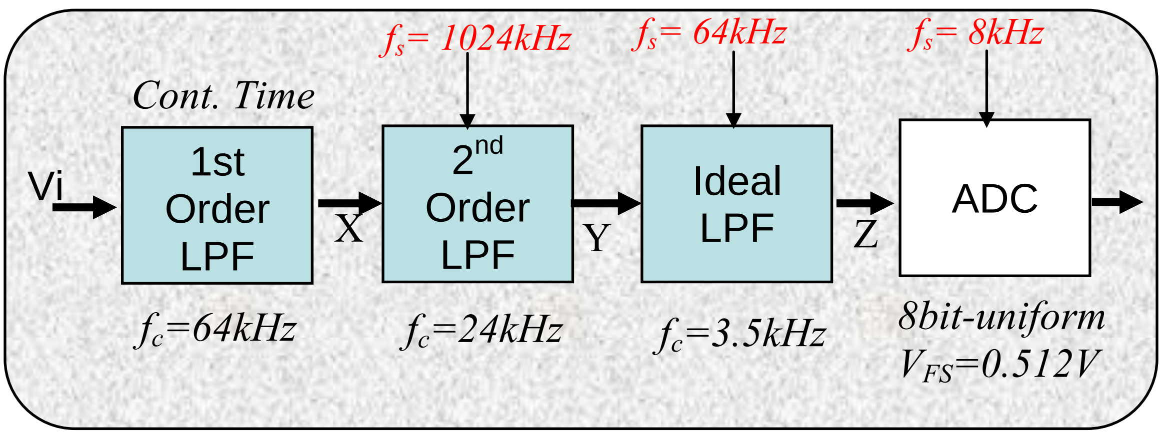
Problem 1: Aliasing

A simplified block diagram for the transmit path of a CODEC chip is shown bellow. The first stage is a 1st order continuous-time filter. The 2nd stage is a 2nd order S.C. filter. The third stage the high order main filter and uses double-sampling. For simplicity assume the main filter has a brick-wall magnitude response with infinite out-of-band rejection.



A composite signal composed of the wanted voice-band component:
$A1x\sin(2\pi f_1 t)$
Plus unwanted signals:
$A2x\sin(2\pi f_2 t) + A3x\sin(2\pi f_3 t) + A4x\sin(2\pi f_4 t) + A51x\sin(2\pi f_5 t)$
Where: $f_1 = 2kHz, f_2 = 129kHz, f_3 = 122kHz, f_4 = 893kHz, f_5 = 1156kHz$

a)

1- Which of the above components do you expect to appear at the input of the ADC (node Z) and at what frequency?
2- Assuming gain of 1 for all of the building blocks except for the main filter which has an inband gain of 2. Compute A1 for the wanted signal to have peak-to-peak amplitude equal to ½ of the full-scale associated with the ADC (node Z).
3- Find the peak amplitude (Ax) of the unwanted signals such that their peak-to-peak magnitude for each component is equal to 1/2LSB of the ADC

(thus undetectable). For simplicity of computation, you can assume the attenuation associated with the first two stages is given by:

$$|H(f)| \sim (f_c/f)^n \text{ for } f > f_c$$

Where n is the order of the filter. Also, you can ignore the sinx/x droop effect due to the hold function.

b) Recompute part a) section 3 assuming the 1st stage (continuous-time filter) is removed.

c) Recompute part b) assuming the 2nd stage (2nd order SC filter) is also removed.

d) Discuss and compare the results in part a,b, and c.

Problem 2: Gm Cell Design Considerations

A gm-cell is made of a bipolar emitter-couple pair at the input. The differential output current as a function of the input voltage is derived:

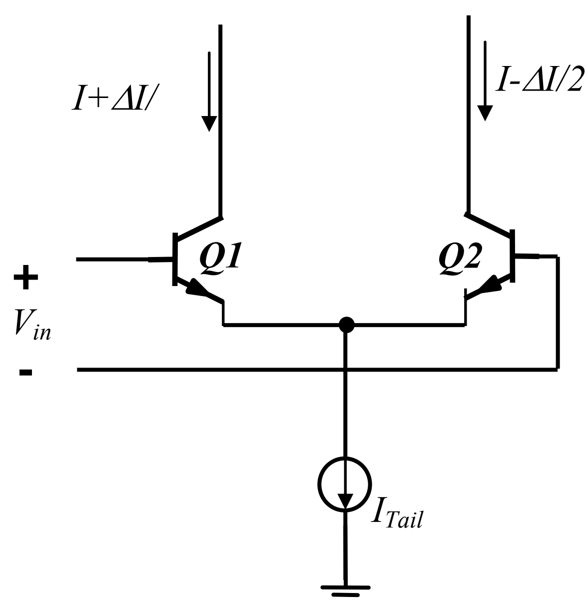
$$\Delta I = I_{Tail} \times \tanh\left(\frac{V_{in}}{2V_T}\right) \quad \text{where } V_T = {}^{kT}\!/_{q} = 26mV \text{ @ room temp.}$$

$$\text{Use taylor expansion: } \tanh(x) \approx x - \frac{x^3}{3}$$

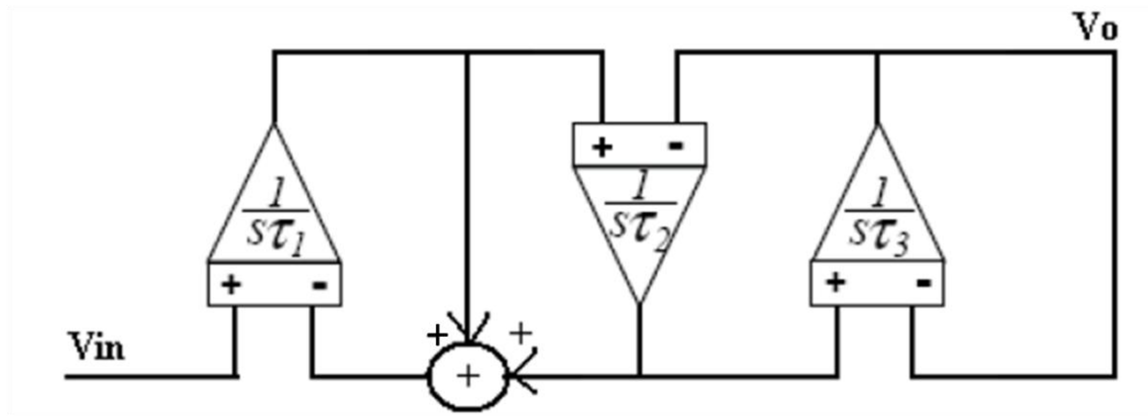
a- Find the peak input voltage for which HD3=2%

b- Find the peak input voltage for which IM3=1%

c- Can you make any suggestions in order to increase the maximum signal handling capability of the emitter-coupled pair based gm-cell?



Problem 3: Switched-Capacitor Filter Design



The diagram above, shows the integrator implementation of a 3rd order lowpass filter with a corner frequency of 18KHz and sampling frequency of 3.6MHz.

Assuming $\tau1= \tau3=16.48$usec and $\tau2=11.32$usec

Submit

- a- The schematic for the switched-capacitor filter using bottom-plate LDI integrators. You have the option of using single-ended or differential structure.
- b- Choose all integrating CI=5pF, find all the other capacitor sizes.
- c- Proof LDI operation in the form of either a z-domain block diagram using the model from Lecture 10, page 14 or performing Periodic AC analysis and plotting the magnitude response both with coarse y-axis and detail of the passband.
- d- Name one advantage and one disadvantage of using switched-capacitor filter technique.
- e- Find the minimum value for the op-amp slew rate for the final stage such that the third order harmonic distortion at signal frequency 5kHz is at -40dB compared to the signal for an output signal of 1V-peak.