Solution to Homework 5

Problem 1.

a- Since

$$\sigma_{DNL} = \sigma_{\frac{\Delta R}{R}} \quad (1)$$

$$\sigma_{INL} \approx \frac{1}{2}\sqrt{2^B}\sigma_{\frac{\Delta R}{R}} \quad (2)$$

Given B=14, $\sigma_{\frac{\Delta R}{R}}$=0.2%, we get $\sigma_{DNL} = 0.2\%, \sigma_{INL} = 12.8\%$

So INL is the constraint on yield. To meet INL<0.5LSB, the expected yield $P\left(\frac{0.5}{\sigma_{INL}}\right) \approx$ 99.99%

b- If the expected yield is changed to 99%, then we can get $\frac{0.5}{\sigma_{INL}} > 2.6$

Combine with (2), B<15.2

So maximum achievable resolution is B=15

Problem 2.

a- $$LSB = \frac{Vref - \frac{R+(N-1)\Delta R}{NR+\frac{\Delta RN(N-1)}{2}}Vref}{N-1} = \left(\frac{R+\frac{\Delta R(N-2)}{2}}{NR+\frac{\Delta RN(N-1)}{2}}\right)Vref \approx \left(\frac{R+\frac{\Delta R(N-2)}{2}}{NR}\right)Vref \quad (3)$$

So for tap m, its ideal voltage

$$Videal(m) = \left(\frac{mR+(N-1)R+\frac{\Delta R(m-1)(N-2)}{2}}{NR+\frac{\Delta RN(N-1)}{2}}\right)Vref \quad (4)$$

$$Vreal(m) = \frac{[mR+\sum_{k=1}^{m}(\mathrm{N-k})\Delta R]*Vref}{NR+\frac{\Delta RN(N-1)}{2}} \approx \frac{\left(\mathrm{mR+mN}\Delta R-\frac{\Delta Rm(m+1)}{2}\right)*Vref}{NR} \quad (5)$$

So

$$DNL(m) = \frac{Vreal(m)-Vreal(m-1)-LSB}{LSB} \approx \frac{(\mathrm{N/2-m+1})\Delta R}{R} \quad (6)$$

$$INL(m) = \frac{Vreal(m)-Videal(m)}{LSB} \approx \frac{\sum_{k=2}^{m}(\mathrm{N-k})\Delta R-\frac{\Delta R(m-1)(N-2)}{2}}{R} = \frac{(m-1)(N-m)\Delta R}{2R} \quad (7)$$

For DNL, when m=1 or N, DNLmax= $\frac{\mathrm{N}\Delta R}{2R}$ LSB

For INL, if N is even, then when m=N/2 or N/2+1, INLmax=$\frac{N(\mathrm{N-2})\Delta R}{8R} \approx \frac{N^2\Delta R}{8R}$ LSB

b- For 12-bit DAC, N=4096, so from part a),

$$\frac{N(\mathrm{N-2})\Delta R}{8R} < 0.5 \quad (8)$$

Therefore $\frac{\Delta R}{R} < 2.4 \cdot 10^{-7}$

Problem 3 - Study the publication below:

Chi-Hung Lin and Klaas Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2"

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 12, DECEMBER 1998

1. *What application is this DAC intended for?*

This DAC is intended to be used as an embedded high-speed high-resolution data converter for cable modem applications in which small area and large wide-band SFDR are important design considerations.

2. *What are the special system requirements for the DAC discussed in this paper and why?*

This DAC must be able to transmit signal frequencies anywhere from 5-65 MHz with true 10-bit resolution at sampling speeds up to 200MHz. The total harmonic distortion of the system is required to be less than 47 dB below the fundamental signal, which translates to a SFDR of more than 52 dB.

3. *What are the advantages and disadvantages of utilitizing thermometer-coded DAC compared to binary-weighted DAC?*

The major advantage of the binary-weighted DAC over the thermometer-coded DAC is its low overhead, since no decoding logic is required. At higher bit resolutions, the digital logic required to run a thermometer-coded DAC begins to dominate area constraints because the number of switches and decoding logic increases exponentially with resolution. However, in contrast to binary-weighted DACs, thermometer-coded DACs are inherently monotonic, and have less stringent matching requirements for the same DNL. In addition, the glitching problem that happens at mid-code in binary-weighted DACs is eliminated since only one current source is switching on or off. Furthermore, harmonic distortion due to level-dependent glitching is eliminated since any glitching at the output is only linearly dependent on the input signal magnitude.

4. *Explain why the authors perform 100 MATLAB simulations (Fig.7.)?*

The authors perform multiple simulations in order to obtain statistical DNL and INL measurements. In each simulation, the unit current sources were varied (with mean value of 1 LSB and sigma of 0.02 LSB) and DNL and INL measurements were taken for each variation of the circuit. With 100 groups of measurements, the more meaningful RMS values of DNL and INL could be studied.

5. *How did they obtain results shown in Fig. 8? Do the results agree with the ones discussed in the lectures?*

At each input code across the 100 MATLAB simulation results, the DNL and INL values were squared, summed, and then square-rooted, resulting in the RMS DNL and INL values of each code. As discussed in class, for the binary-weighted DAC, the worst case DNL occurs at mid-code where the most current sources are being switched, and has RMS value: $\sigma_{DNL} \approx 2^{B/2} \sigma$, whereas for the unit-element DAC, the worst case DNL has RMS value: $\sigma_{DNL} \approx \sigma$. Also, the INL RMS values agree with what

was discussed in class as both types of DACs have a worst case INL RMS value at $\sigma_{INL} = .5 * \sqrt{(2^B - 1)}$ σ.

6. In Fig. 9 what do the authors mean by 0% segmentation and 100% segmentation (x-axis)?
The percentage of segmentation of the DAC is the percentage of the total bits that are generated by thermometer-coded current sources, starting from the MSB. A 0% segmented DAC is purely-binary weighted while a 100% segmented DAC is purely thermometer-coded. As an example, a 20% segmentation of a 10-bit DAC would be made up of a 2-bit thermometer-coded DAC at the top two MSBs and an 8-bit binary-weighted DAC at the bottom 8 bits.

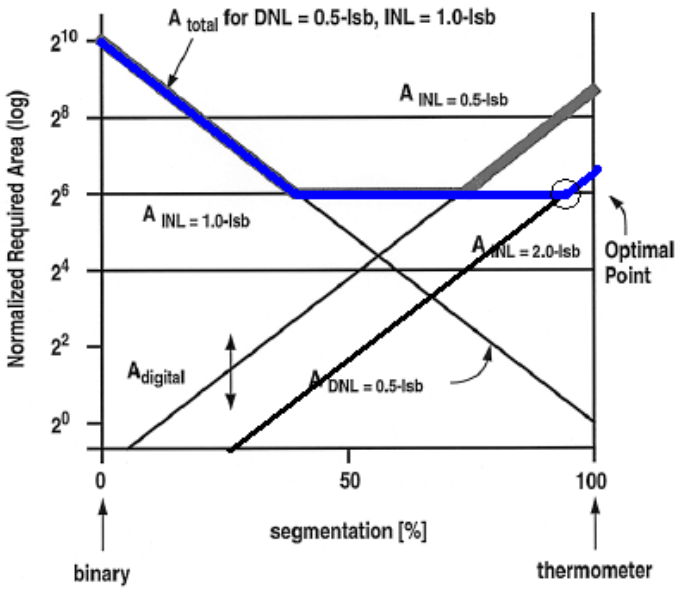
7. Explain the considerations for the optimal point in Fig. 9.
Figure 9 shows normalized required area versus percentage of segmentation for certain DNL and INL performance constraints. When only taking into account miminum area, the optimal segmentation can be chosen anywhere on the flat part of the curve as this corresponds to the same area and thus INL. However, as segmentation is increased (and the DAC shifts towards more of a thermometer-coded design) the DNL of the DAC improves and THD due to glitch distortion is also minimized. Thus, the optimal point shown on the plot meets the specified INL requirement at minimum area, while also minimizing distortion and worst-case DNL. Also, note that at this point, the digital overhead area associated with the thermometer-coded design is equal to the analog area.

8. Assume equation (2) can be expressed as:

$$\sigma^2 = k / Area$$

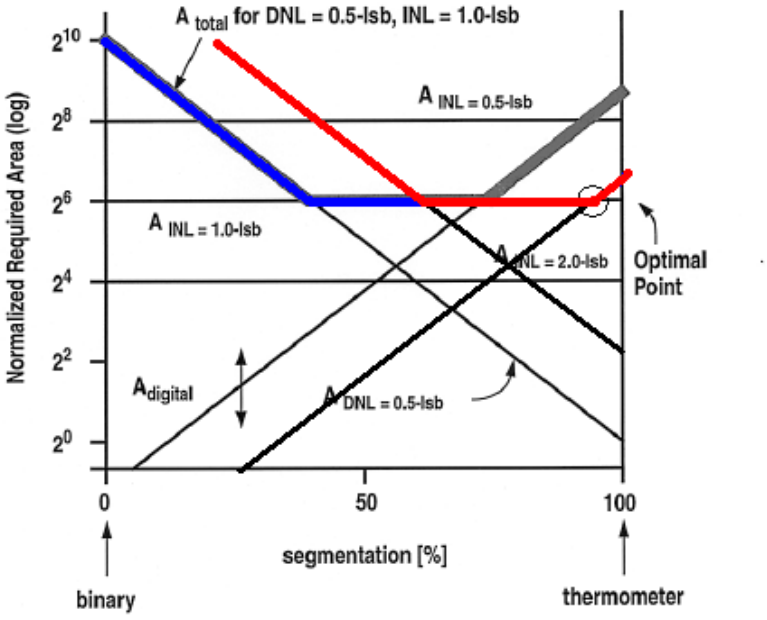
This DAC is going to be implemented in a more advanced technology, with all minimum feature sizes scaled by a factor of 1/2 compared to the 0.35µ tecnology used by the authors. Assuming k remains the same for the new technology, on the copy of Fig. 9 shown below, draw the portions, which will change for the new technology. Based on your new drawing, would the choice of segmentation be any different for the new technology? If the answer were positive, then would it be more towards 100% or 0% segmentation on the x-axis?

If we assume that we want the same INL and DNL behavior, the analog portion of the DAC would not be scaled with the technology; only the digital circuitry supporting the thermometer-coded DAC would decrease by a factor of 4 in area:



From the new curve, the optimal segmentation point is closer to 100%. This makes intuitive sense, since the limiting factor on moving to an entirely thermometer-coded approach is the overhead area of the digital decoding circuitry.

9. *Add the curve associated with the more stringent DNL requirement of 0.25LSB. Would this affect the choice of segmentation percentage found in the previous part?*



No, a more stringent DNL requirement would not affect the choice of segmentation since it is only the INL and digital circuitry area requirements that set the optimal point. If the DNL were required to be even more stringent such that the area required supercedes the INL requirement (at perhaps 1/16 LSB) then there would be a new optimal segmentation point.

10. Explain why in Fig. 22. the measured SFDR drops for the extremes of I_{BIAS}.
At the low extreme of I_{BIAS}, SFDR drops because threshold mismatch becomes more noticeable with the drop in V_{GS}. At the high extreme of I_{BIAS}, SFDR drops because the current source becomes headroom limited with the increase in V_{GS}.