UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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	Homework 6	**EECS 247**
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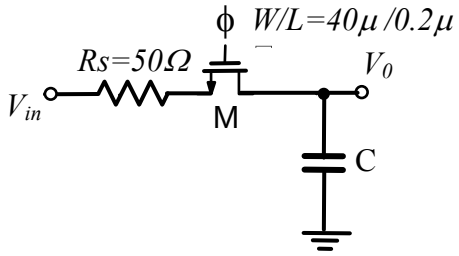
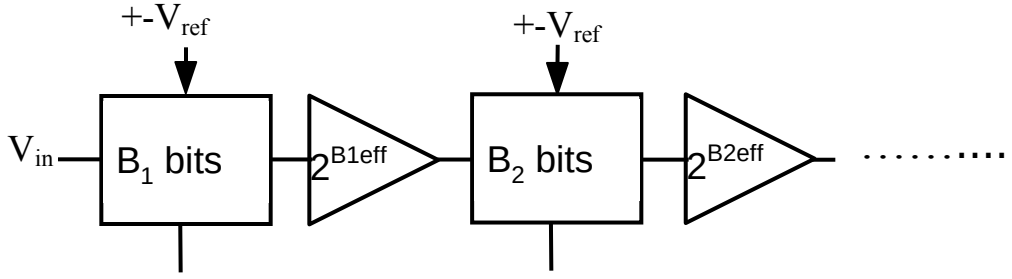
1. A basic NMOS track and hold circuit is shown below. The clock applied to the gate of the transistor swings from V_{SS}=0V to V_{DD}=1.5V. Assume an ideal square law model for the transistor with V_{TH}=0.2V and μC_{ox}=250μA/V^2. Ignore body effect.
   a) Suppose this circuit precedes a 14-bit ADC. How large should we choose C so that the input referred rms noise from the sampler is equal to 0.25LSB of the ADC at T = 27°C? Compared to the case where only quantization noise is present, how much is the overall SNR degraded by the input-referred kT/C noise.
   b) If the clock has a 50% duty cycle, calculate the maximum clock frequency at which inputs between 0…1.0V input can be sampled to within 1/8 LSB accuracy at 14 bit resolution. Assume C =15pF . You can use the average resistance for M1.
   c) In practice, what are the other factors affecting the accuracy of this sampling front-end?

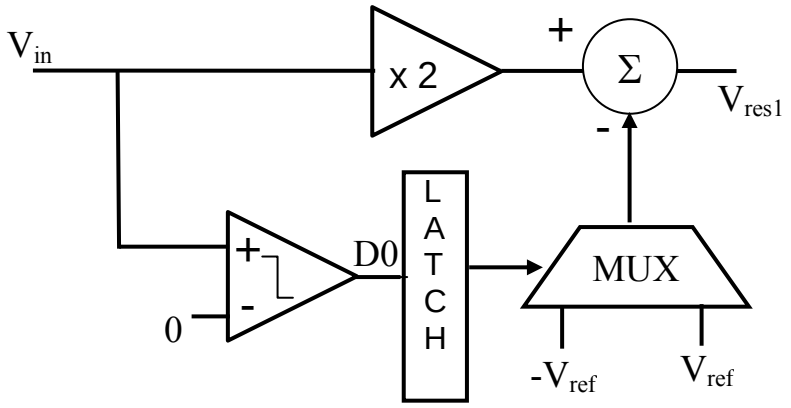


2. Consider a 6-bit flash ADC with an ideal reference resistor string and V_{ref}=1V. Assume that the comparators have an offset voltage with standard deviation σ_{OS}=3mV. What are the standard deviations of the converter's worst case DNL and INL?

3. Shown below is the block diagram of a pipelined ADC. Note that the input voltage is centered around ground level.

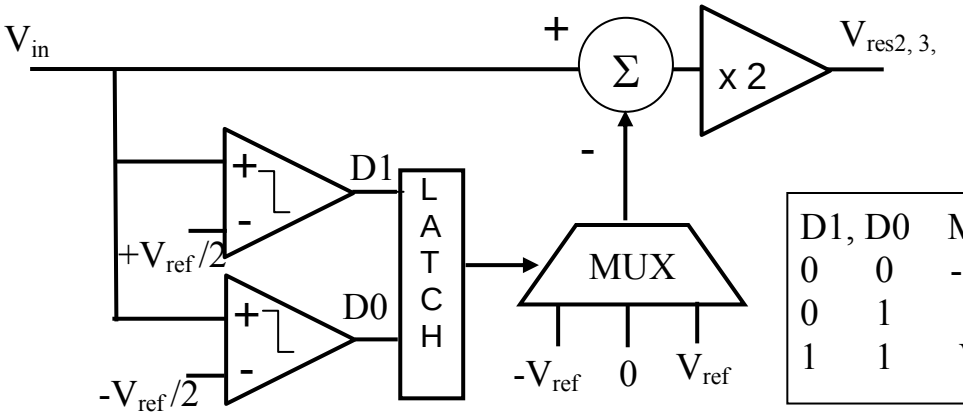


The first stage has the following block diagram:



D0	MUX_{output}
0	-Vref
1	Vref

The rest of the stages have the block diagram shown bellow:



D1, D0		MUX_{output}
0	0	$-V_{ref}$
0	1	0
1	1	V_{ref}

a) What is the effective number of bits for stage 1 and the following stages? What is the raw number of bits for each stage?
b) How many stages are needed to implement a 12bit ADC?
c) If each stage takes one clock cycle per conversion, what is the minimum signal latency from the analog input to the digital output?
d) Derive the residue plot for the first and the following stages.
e) What is the maximum tolerable comparator offset in the 1st stage (assume all other stages are ideal)? Show your derivation on the residue plot/s.
f) What is the maximum tolerable comparator offset in the 2nd stage (assume all other stages are ideal)? Show your derivation on the residue plot/s. b