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	Homework 6 Solution	**EECS 247**
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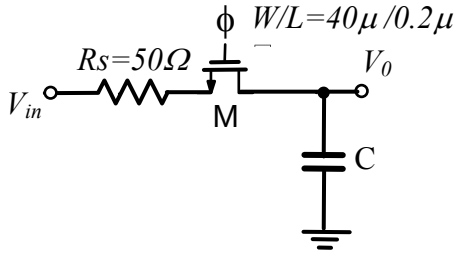
1. A basic NMOS track and hold circuit is shown below. The clock applied to the gate of the transistor swings from V_{SS}=0V to V_{DD}=1.5V. Assume an ideal square law model for the transistor with V_{TH}=0.2V and μC_{ox}=250μA/V^2. Ignore body effect.
   a) Suppose this circuit precedes a 14-bit ADC. How large should we choose C so that the input referred rms noise from the sampler is equal to 0.25LSB of the ADC at T = 27°C? Compared to the case where only quantization noise is present, how much is the overall SNR degraded by the input-referred kT/C noise.
   b) If the clock has a 50% duty cycle, calculate the maximum clock frequency at which inputs between 0…1.0V input can be sampled to within 1/8 LSB accuracy at 14 bit resolution. Assume C =15pF . You can use the average resistance for M1.
   c) In practice, what are the other factors affecting the accuracy of this sampling front-end?



Solution:

a) For KT/C noise to be 1/4LSB & VFS=1V and considering B=14bit:

$$\sqrt{KT/C} = 1/4\frac{V_{FS}}{2^B} \qquad \rightarrow C = \frac{2^{2B}KT}{0.25^2 x V_{FS}^{\ 2}} = \frac{2^{2x14}KT}{0.25^2 x1^2} = 17.9\,pF$$

Loss of SNR can be computed as:

$$SNR - SQNR = 10\log\frac{\Delta^2/12}{\Delta^2/12 + (0.25\Delta)^2} = -2.43dB$$

b) During the track mode, C is charged with the time constant RC, thus:

$$V_{out}(t) = V_{in}\left(1 - e^{-\frac{t}{RC}}\right)$$

To compute the error associated with the not fully settled output at the end of track ½ clock cycle:

$$\varepsilon = V_{in} - V_{out}\big|_{@Ts/2} = V_{in}e^{\frac{Ts}{2RC}}$$

In this case, the total resistance consists of the source Rs and equivalent switch resistance.

In the lectures, switch resistance was found as:

$$R_{sw} = \frac{R_0}{1 - \frac{V_{in}}{V_{DD} - V_{th}}} \qquad with \quad R_0 = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{th})} = 15.3\Omega$$

Then:

Rsw

$$Rsw|_{average} = \left(Rsw|_{Vin=0} + Rsw|_{Vin=1V}\right)/2 = 40.8\Omega$$

$$\varepsilon = V_{in} e^{\frac{1}{2\,fsC(Rs+Rsw))}}$$

$$\rightarrow \varepsilon = 1xe^{\frac{1}{2\,fsC(Rs+Rsw))}} = e^{\frac{367MHz}{fs}}$$

Since it is required that $\varepsilon < 1/8LSB$:

$$e^{\frac{367MHz}{fs}} \leq \frac{1}{8x2^{14}}$$

$$\rightarrow f_s \leq \frac{367MHz}{ln\,2^{17}} = 31.1MHz$$

C) In practice other factors affecting the accuracy of the sampling process includes switch charge injection and clock feedthrough.

2. Consider a 6-bit flash ADC with an ideal reference resistor string and V_{ref}=1V. Assume that the comparators have an offset voltage with standard deviation σ_{OS}=3mV. What are the standard deviations of the converter's worst case DNL and INL?

Assuming that the DAC generates ideal level values, the uncertainty for each decision threshold is only due to comparator offset. In particular, each decision level is affected by the offset associated with only the comparator connected to the corresponding tap and is independent of the offset due to the rest of the comparators. Since INL is the deviation of the transition from its ideal position measured in terms of LSB:

$$INL = \frac{V_{actual} - V_{ideal}}{\Delta}$$

Then :

$$\sigma_{INL} = \frac{\sigma_{OS}}{\Delta} = \frac{\sigma_{OS}}{\frac{V_{FS}}{2^B}} = \frac{3mV}{\frac{1V}{2^6}} = 0.19LSB$$

DNL is defined as the deviation of the width of each code from 1LSB:

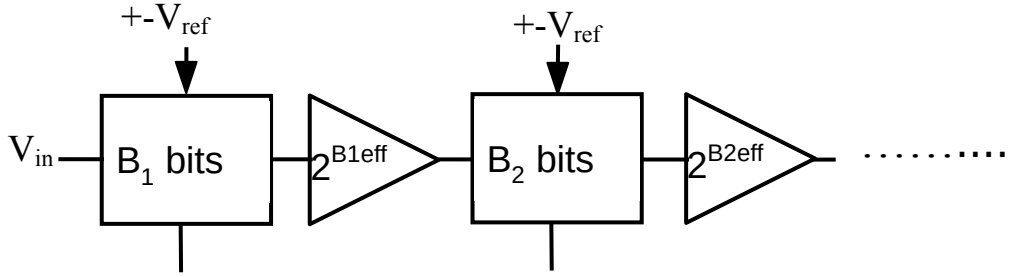
$$DNL = \frac{V_{i+1}^{actual} - V_i^{actual}}{\Delta} - 1$$

Assuming the offset associated with two consecutive comparator is uncorrelated then:

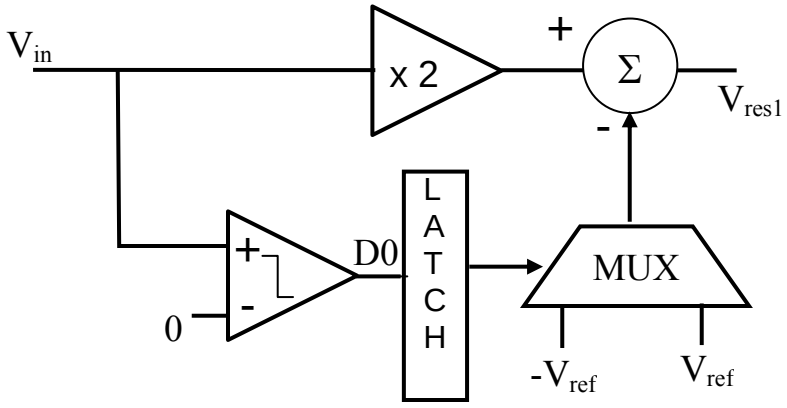
$$\sigma_{DNL} = \frac{\sqrt{2\sigma_{OS}^2}}{\Delta} = \frac{\sqrt{2}\,\sigma_{OS}}{\frac{V_{FS}}{2^6}} = \frac{\sqrt{2}\,x3mV}{\frac{1V}{2^6}} = 0.27LSB$$

Note that DNL is worse than INL in this case.

3. Shown below is the block diagram of a pipelined ADC. Note that the input voltage is centered around ground level.

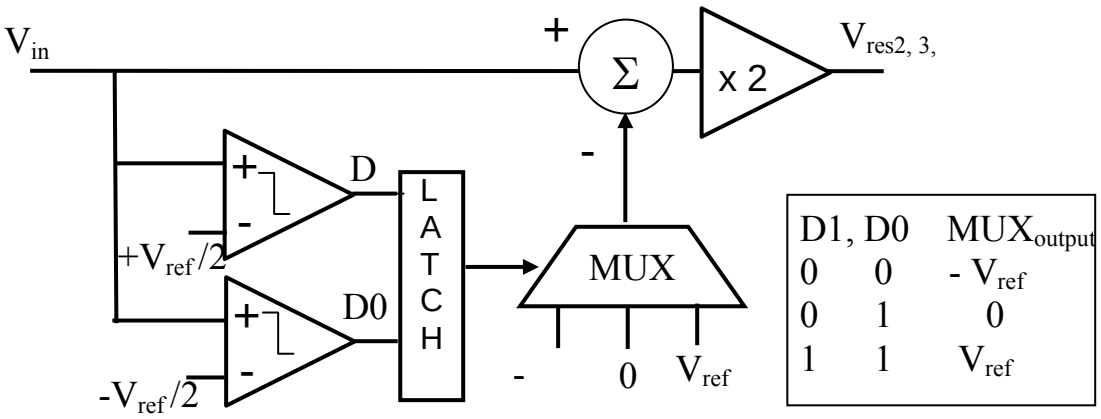


The first stage has the following block diagram:



D0	MUX_{output}
0	-Vref
1	Vref

The rest of the stages have the block diagram shown bellow:



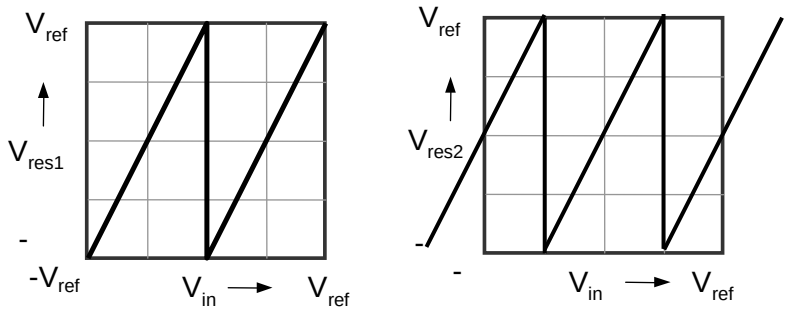
a) What is the effective number of bits for stage 1 and the following stages? What is the raw number of bits for each stage?
b) How many stages are needed to implement a 12bit ADC?
c) If each stage takes one clock cycle per conversion, what is the minimum signal latency from the analog input to the digital output?
d) Derive the residue plot for the first and the following stages.
e) What is the maximum tolerable comparator offset in the 1st stage (assume all other stages are ideal)? Show your derivation on the residue plot/s.
f) What is the maximum tolerable comparator offset in the 2nd stage (assume all other stages are ideal)? Show your derivation on the residue plot/s. a

Bonus extra credit section:

g) Simulate a 3-stage version of this ADC first assuming no comparator offset. Derive the transfer curve and DNL/INL. Second, apply ½ offset you found in part f) and prove no missing codes. Third, apply enough comparator offset to have missing codes.

Solution:

a) Effective # of bits is $\log_2(2)$=1bit and the raw is $\log_2(1+1)$=1bit for stage 1. For the other stages effective $\log_2(2)$=1bit and raw is $\log_2(2+1)$=1.58bit.
b) No of stages needed are 12.
c) Latency is 12 clock cycles. Depending on the architecture the minimum would be ½ clock cycle per stage or 6 clock cycles.
d)



Stage 1 Stage 2,3,….

e&f) as shown in the figure: The 2nd stage can correct for Vref/4 offset associated with the 1st stage. The 3rd stage can correct for the same amount of offset in the 2nd stage comparator. Note that if the criteria are for no missing code in the overall transfer curve then peak to peak residue of +-LSB can be considered which translates to maximum allowable offset of +-Vref/2 for single errors.