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Solution to HW – 7

Problem 1

The first step of the design is to determine the correct oversampling ratio M to achieve the desired SQNR for both topologies. We use the following formula:

$$DR = 10log\left(\frac{3(2L+1)}{2\pi^{2L}}\right) + (2L+1) * 10 * logM$$

For the second order modulator, we get M=105, so we choose $\boldsymbol{M = 2^7 = 128}$, which results in SQNR = 94.26dB and

For the third order modulator, we get M = 36, so we choose $\boldsymbol{M = 2^6 = 64}$, which results in SQNR = 106.8dB.

Since the signal bandwidth is $B = 80kHz$, we get: $\begin{cases} f_s = 20.48MHz\ (2^{nd} order) \\ f_s = 10.24MHz\ (3^{rd} order) \end{cases}$

We also compute the in-band quantization noise power with the formula:

$$\overline{S_Q} = 10log\left(\frac{\pi^{2L}}{2L+1}\frac{1}{M^{2L+1}}\frac{\Delta^2}{12}\right)dBW$$

And we get:

$$\boldsymbol{\overline{S_Q} = -97.26dBW} \text{ for the second order modulator}$$

$$\boldsymbol{\overline{S_Q} = -109.8dBW} \text{ for the third order modulator}$$

To suppress in band spurious tones due to low input DC levels, the power of $\frac{kT}{C}$ noise is designed to be higher than the power of quantization noise, yet still lower than the desired SNR ratio. Since the power of the input signal is:

$$\overline{S_X} = 10log\left(\frac{1}{2}\left(\frac{\Delta}{2}\right)^2\right)dBW = -3dBW$$

We need $S_N < -93dBW$. We chose $S_N = -94dBW$, for both modulators.

The main contribution to $\frac{kT}{C}$ noise is given by the sampling capacitor at the input of the first integrator, while the noise of subsequent integrators is shaped out-of-band, and it will be neglected. The in-band noise of the modulators is:

$$\overline{S_N} = 10\log\left(\frac{2kT}{C_S M}\right) = -94dBW \Rightarrow \begin{cases} C_S = 162.5fF\ (2^{nd} order) \\ C_S = 325fF\ (3^{rd} order) \end{cases}$$

We opted for doubling this value to compute the actual integrator capacitance, assuming that the signal at the input of the integrator is attenuated by a factor of 2, in order to limit the integrator output voltage swing and improve the actual DR of the modulator. Nevertheless, we note that the actual attenuation factor should be evaluated differently for each design, with the help of simulation. We thus get:

$$\begin{cases} \boldsymbol{C_{INT} = 325fF\ (2^{nd}order)} \\ \boldsymbol{C_{INT} = 650fF\ (3^{rd}order)} \end{cases}$$

Since the design is slew limited, we can now compute the current required by the first integrator to drive the above calculated capacitors. We get:

$$SR = 1.2 * \Delta * f_s = \frac{I_y}{C_{INT}} \Rightarrow \begin{cases} I_y = 16\mu A\ (2^{nd}order) \\ I_y = 16\mu A\ (3^{rd}order) \end{cases}$$

We note that the current consumption is equal in both designs, since the integrator in the second order modulator needs to drive half the capacitance at twice the frequency of the third order modulator. As a consequence, the power consumption of the first integrator of both devices is equal to:

$$\boldsymbol{P = 2 * I_y * V_{DD} = 80\mu W}$$

The total power consumption, considering 1 more integrator and the analog circuitry in the second order modulator, and 2 more integrators and the analog circuitry in the third order integrator, is:

$$\begin{cases} \boldsymbol{P = 128\mu W\ (2^{nd}order)} \\ \boldsymbol{P = 168\mu W\ (3^{rd}order)} \end{cases}$$

Finally, we need to design the anti-aliasing filter. From the signal spectrum, and considering that $\begin{cases} f_s = 20.48MHz\ (2^{nd}order) \\ f_s = 10.24MHz\ (3^{rd}order) \end{cases}$, the components that may alias in-band have an input power equal to $-50dBc$. The anti-aliasing filter needs to guarantee that the signal at $f = f_s - B$ gets attenuated below $-95dBc$. Since the signal power at that frequency is already $-50dBc$, we need an extra attenuation equal to $-45dB$, to meet the specs. Finally, we assume that the digital backend can compensate for the in-band droop caused by the filter, since the specifications do not mention the maximum allowed in-band droop: we thus choose $f_{-3dB,filter} = f_{in} = 80kHz$. We can use the approximated formula:

$$attenuation = 20 * log\left(\frac{f_{-3dB,filter}}{f_s - B}\right)^N = -45dB$$

Where N is the required filter order. We get:

$$\begin{cases} N = 0.9375 \\ N = 1.07 \end{cases} \Rightarrow \begin{cases} \boldsymbol{N = 1\ (2^{nd}order)} \\ \boldsymbol{N = 2\ (3^{rd}order)} \end{cases}$$

Thus the power consumption in the filter is:

$$\begin{cases} \boldsymbol{P_{filter} = 0\ (2^{nd} order)} \\ \boldsymbol{P_{filter} = 80\mu W\ (3^{rd} order)} \end{cases}$$

For a total power of:

$$\begin{cases} \boldsymbol{P_{total} = 128\mu W\ (2^{nd} order)} \\ \boldsymbol{P_{total} = 248\mu W\ (3^{rd} order)} \end{cases}$$

Which would suggest, in first analysis, to opt for the second order modulator.

Problem 2

First, we note that $DR = 110dB$ is required to get a resolution of 18 bits.

For the plain oversampling converter, since we gain only 3dB for extra octave of oversampling then fs=2Bx$2^{110/3}$ =4.44x10^{15} of to have it a factor of requires 2^{37} makes the required sampling frequency fs=5.5 x10^{15}

We can again use the following formula to determine the required oversampling ratio for architectures b) and c), where $L = 1{,}2$ respectively.

$$DR = 10log\left(\frac{3(2L+1)}{2\pi^{2L}}\right) + (2L+1) * 10 * logM$$

We get:

$$\begin{cases} M = 1.717 * 10^{10} \\ M = 6080 \\ M = 264 \end{cases} \Rightarrow \begin{cases} M = 2^{34} \\ M = 8192 \\ M = 512 \end{cases}$$

Where all oversampling ratios have been chosen to be a power of 2 to allow margin for the thermal noise to dominate, and to ease the design of the backend digital filter.

So:

$$\begin{cases} \boldsymbol{f_s = 4.44 * 10^{15} Hz\ for}\ M = 1.717 * 10^{10} \\ \boldsymbol{f_s = 243 MHz}\ for\ M = 6080 \\ \boldsymbol{f_s = 10.63 MHz\ \ for}\ M = 264 \end{cases} \Rightarrow M\ factor\ of\ 2 \begin{cases} \boldsymbol{f_s = 5.5\ x10^{15} Hz, (a)} \\ \boldsymbol{f_s = 327.68 MHz, (b)} \\ \boldsymbol{f_s = 20.48 MHz, (c)} \end{cases}$$

Option (c) is preferable because it requires a slower clock frequency, which ease the requirement of the analog blocks and dissipates less power due to the reduced switching activity, and it better rejects limit cycles due to input DC components, due to the higher randomizing effect caused by the 2 integrators.