Solution EE247 HW4 2010

Problem No. 1: DAC Static Characteristics

a. Assume the transition points of the ideal 3-bit DAC are

$$TP_i = LSB \times i\text{, where i=0, 1, 2, ..., 7.}$$

For end points, TP_0=0 and TP_7=350mV. Since the actual test measures TP'_0=-2mV and TP'_7=363mV,

$$Offset\ Error = -2mV - 0 = -2mV\text{, or } -0.04LSB$$
$$Full\ Scale\ Error = 363mV - 350mV = 13mV\text{, or } 0.26LSB$$

b. The ideal gain is obviously 1 LSB/code. The actual gain is however

$$Gain' = \frac{TP_7 - TP_0}{7} = \frac{365\,mV}{7} = 52.14\ {}^{mV}\!/_{code}\text{, or } 1.04\ {}^{LSB}\!/_{code}$$

Gain error is therefore

$$\varepsilon_{gain} = Gain' - Gain = 0.04\ {}^{LSB}\!/_{code}$$

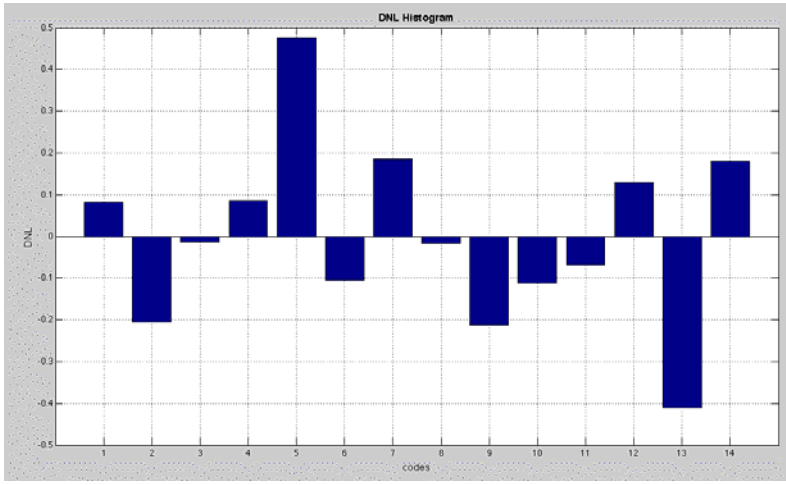
c. Now that the actual LSB size (52.14mV) is computed, the measurement data can be tabulated as follows to calculate DNL and INL.

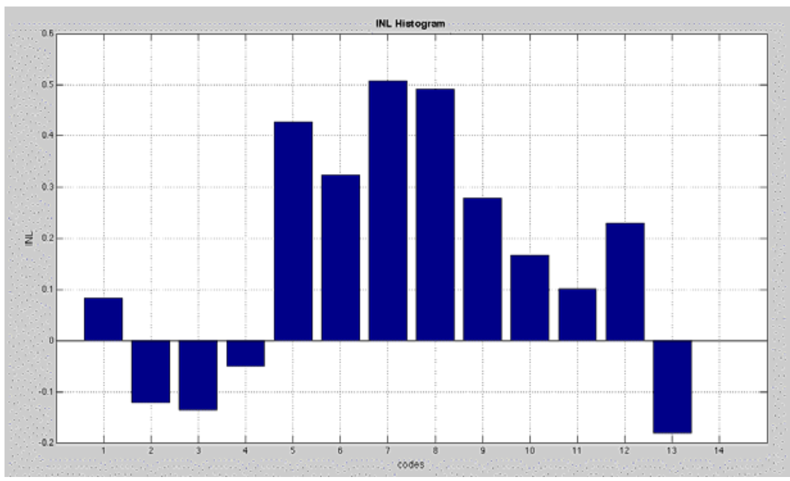
Code	**End-Point Corrected Codes**	**Transition Point**	**Segment Size**	**DNL**	**INL**
000	0	-2mV	–	–	0
001	52.14mV	52mV	54mV	1.86mV, 0.04LSB	0.04LSB
010	104.28mV	98mV	46mV	-6.14mV, -0.12LSB	-0.08LSB
011	156.42mV	160mV	62mV	9.86mV, 0.19LSB	0.11LSB
100	208.56mV	205mV	45mV	-7.14mV, -0.14LSB	-0.03LSB
101	260.7mV	245mV	40mV	-12.14mV, -0.23LSB	-0.26LSB
110	312.84mV	305mV	60mV	7.86mV, 0.15LSB	-0.11LSB
111	365mV	363mV	58mV	5.86mV, 0.11LSB	0

d. From above table maximum DNL is |-0.23LSB|=0.23LSB.
Maximum INL is |-0.26LSB|=0.26LSB.

Problem No. 2: Ramp Histogram Test

a. From the given ramp histogram, DNL and INL (except the first and last codes) can be calculated using Matlab:





b. From above charts, peak positive DNL =0.477LSB, peak negative DNL =-0.411LSB; Peak positive INL =0.508LSB, peak negative INL=-0.181LSB.

c. Matlab code is listed below:

```
clear;
y = [1102 810 1005 1106 1504 912 1207 1001 802 905 950 1150
600 1203];
avg = sum(y)/length(y);
dnl = y/avg-1;
inl = cumsum(dnl);
```

d. Histogram test in general does not guarantee monotonicity. Severe ADC flows such as code flipping are not detected in histogram test.

Problem No. 3:

1- fs/fx=N/cycle=4096/211=19.41...Integer number of cycles elliminates the need for windowing since the peroidic nature of the signal is preserved in FFT.
Prime number of cyclesrandomizes the quantization noise and hence better accuracy in the output spectrum.

2- From above FFT, it is obvious that the SFDR of the ADC is 42dB.

3-The FFT plot only shows fundamental and 3rd harmonic tones. It is therefore plausible to assume that main source of nonlinearity is 3rd distortion:

$$v_{out} = a_1 v_{in} + a_3 v_{in}^3$$

Infinite number of ADC bits is assumed in above transfer characteristic for simple calculation. With a single-tone input,

$$v_{in} = \frac{1}{2} V_{FS} \sin(\omega t)$$

$$v_{out} = a_1 \frac{V_{FS}}{2} \sin(\omega t) + a_3 \frac{V_{FS}^3}{8} \sin^3(\omega t) = a_1 \frac{V_{FS}}{2} \sin(\omega t) + a_3 \frac{V_{FS}^3}{8} \frac{3\sin(\omega t) - \sin(3\omega t)}{4}$$

$$v_{out} = \left(\frac{a_1 V_{FS}}{2} + \frac{3 a_3 V_{FS}^3}{32} \right) \sin(\omega t) - \frac{a_3 V_{FS}^3}{32} \sin(3\omega t)$$

Given that amplitude of the 3rd harmonic is 42dB below that of fundamental

$$\frac{\frac{a_3 V_{FS}^3}{32}}{\frac{a_1 V_{FS}}{2} + \frac{3 a_3 V_{FS}^3}{32}} \approx \frac{\frac{a_3 V_{FS}^3}{32}}{\frac{a_1 V_{FS}}{2}} = 10^{-\frac{42}{20}}$$

$$a_3 = \frac{a_1 \times 16 \times 10^{-\frac{42}{20}}}{V_{FS}^2} = 0.127 \frac{a_1}{V_{FS}^2}$$

The input-to-output transfer function is then transformed to

$$v_{out} = a_1 v_{in} + \frac{0.127 a_1}{V_{FS}^2} v_{in}^3 \quad \text{— [1]}$$

End points of above transfer function are

$$v_{out}(v_{in} = -\frac{V_{FS}}{2}) = -\frac{a_1 V_{FS}}{2} - \frac{0.127 a_1 V_{FS}}{8}, \quad v_{out}(v_{in} = \frac{V_{FS}}{2}) = \frac{a_1 V_{FS}}{2} + \frac{0.127 a_1 V_{FS}}{8}$$

The ideal (linearized) transfer function is then

$$v_{out} = \frac{v_{out}(\frac{V_{FS}}{2}) - v_{out}(-\frac{V_{FS}}{2})}{V_{FS}} v'_{in} = \left(1 + \frac{0.127}{4}\right) a_1 v'_{in} = 1.032 a_1 v'_{in} \quad \text{— [2]}$$

Substituting v_{out} in Equation [1] with that in Equation [2],

$$1.032 a_1 v'_{in} = a_1 v_{in} + \frac{0.127 a_1}{V_{FS}^2} v_{in}^3$$

$$INL = v_{in} - v'_{in} = v_{in} - \frac{a_1 v_{in} + \frac{0.127 a_1}{V_{FS}^2} v_{in}^3}{1.032 a_1} = \frac{0.032 v_{in} - \frac{0.127}{V_{FS}^2} v_{in}^3}{1.032}$$

To find maximum INL,

$$\frac{\partial INL}{\partial v_{in}} = 0 \Rightarrow \frac{0.032}{1.032} - \frac{3 \times 0.127 \times v_{in}^2}{1.032 V_{FS}^2} = 0 \Rightarrow v_{in,m} = \pm 0.29 V_{FS}$$

$$|INL|_{\max} = \frac{0.032 \times 0.29 V_{FS} - \frac{0.127}{V_{FS}^2}(0.29 V_{FS})^3}{1.032} = 0.006 V_{FS}$$

Since the size of LSB is $\frac{V_{FS}}{2^B} = \frac{V_{FS}}{2^9}$

$$|INL|_{\max} = \frac{0.006 V_{FS}}{\frac{V_{FS}}{2^9}} = 3.1 LSB$$

4- SFDR=20log2^9/3.1=44.3dB not too far from 42dB

5-The total quantization noise amplitude of a 9-bit ADC is

$$\sqrt{\overline{n}_Q^2} = -(6.02 \times 9 + 1.76) = -55.94\, dBFS$$

Given 4096 FFT points, quantization noise floor on the spectrum plot should be

$$nf_Q = \sqrt{\overline{n}_Q^2} - 10\log_{10}\left(\frac{4096}{2}\right) = -55.94 - 33.11 = -89.05\, dBFS$$

But the actual FFT shows noise floor of about -80dBFS. The difference is then contributed by circuit noise, which can be assumed uncorrelated with quantization noise:

$$\overline{n}_Q^2 + \overline{n}_C^2 = -80 + 33.11 = -47\, dBFS$$

where $\overline{n}_Q^2 = 10^{\frac{-55.94}{10}} = 2.547 \times 10^{-6}$ with respect to full-scale input signal power (0dBFS). Estimated circuit noise is therefore

$$\overline{n}_C^2 = 1.995 \times 10^{-5} - 2.745 \times 10^{-6} = -47.6\, dBFS\,.$$

6-If there were no circuit noise (quantization noise only) 47dB SNR is equivalent to

$$\frac{SNR - 1.76}{6.02} = \frac{47 - 1.76}{6.02} = 7.5b$$

Since the actual number of bits is 9, circuit noise contributes to loss of resolution by 1.5 bit LSB.

7- Finally given that total noise is -47dBFS, and harmonic distortion of -42dBFS

$$SNDR = \frac{1}{10^{-\frac{47}{10}} + 10^{-\frac{42}{10}}} = 40.8dB$$

$$ENOB = \frac{SNDR - 1.76}{6.02} = 6.5b$$