UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Midterm Exam	**EECS 247**
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Name: _____

SID: _____

Score: **/40**

Problem 1 6	Problem 2 6	Problem 3 6	Problem 4 22	Total Score 40point

- **Closed books and class notes, no calculators/computers/PDAs**
- **Mark all final and intermediate results clearly**
- Write solutions on the exam sheets. Add extra pages where needed.
- Simplify algebraic results as much as possible.
- Bring into standard form where applicable, show your work.

Useful Expressions:

$\log_{10} 2=0.3, \quad \log_{10} 3=0.477, \quad \log_2 3=1.59$

$2^6=64, \quad 2^7=128, \quad 2^8=256, \quad 2^9=512, \quad 2^{10}=1024$

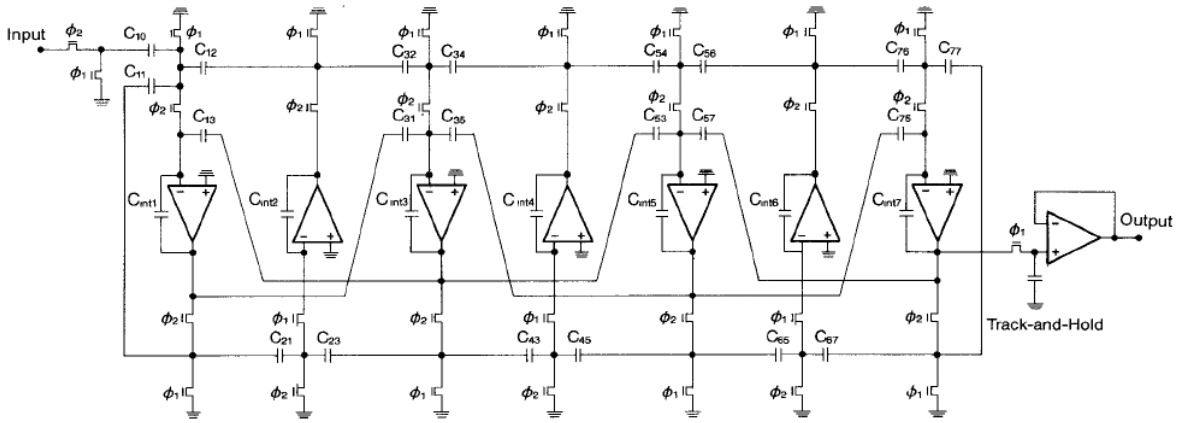
decade=x10

$\frac{1}{1+x} \approx 1-x$ for x small

$\sqrt{1+x} \approx 1+\frac{x}{2}$ for x small

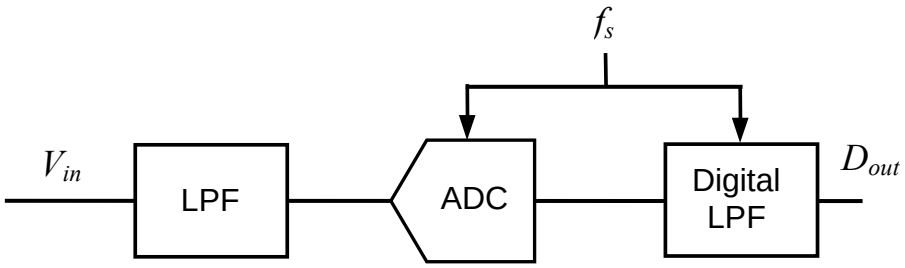
Problem 1: The circuit shown below is a filter.

a) Identify the filter type (low/high/band pass).
b) What is the order of the filter?
c) Does it include transmission zeros? If the answer is positive, which components are added for this purpose?
d) Is it utilizing bottom-plate integrator technique?
e) Is it an LDI implementation? Show your answer.
f) How would low opamp gain affect the magnitude response of the filter?
g) How would opamp non-dominant poles affect the overall magnitude response of the filter?
h) Identify the components whose values influence the total output noise, assuming the opamp noise is negligible (no derivation necessary).
i) To reduce the overall thermal noise by a factor of 2 without changing internal node transfer functions what should be done?
j) To scale the gain of the output node by a factor of 1.5 how would you change the output stage?
k) If double-sampling is to be added to this design, show how it is done by drawing only two stages.
l) What would the effect of double-sampling be on the performance of the filter, assuming the clock frequency and all capacitor values remain the same? What is the advantage of double-sampling?



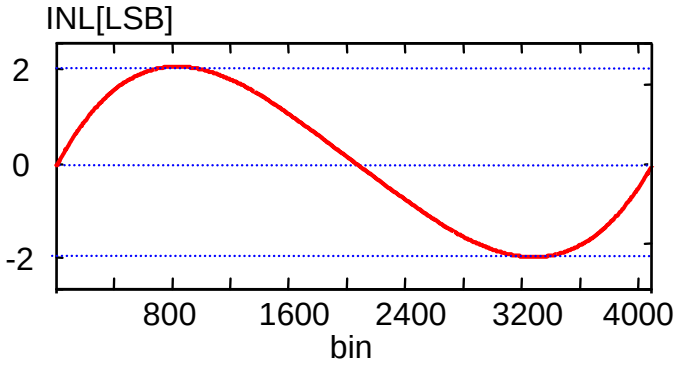
Problem 2- The receive path of a system comprises a continuous-time lowpass filter followed by an ADC converter. Assume the following:
The signal bandwidth of interest spans from **0 to** f_B.
The incoming signal is wideband with equal signal magnitude for all frequencies.
The filter has a roll-off starting at $2f_B$ with ***20dB-per-decade-per-pole*** and with **2 poles**.
The digital filter cuts sharply at f_B.
First, an ADC with very high resolution is used. The measured highest aliased component at the output D_{out} is at ***-40dB*** level with respect to the in-band signal. Ignore magnitude response shaping due to the sample/hold effect.

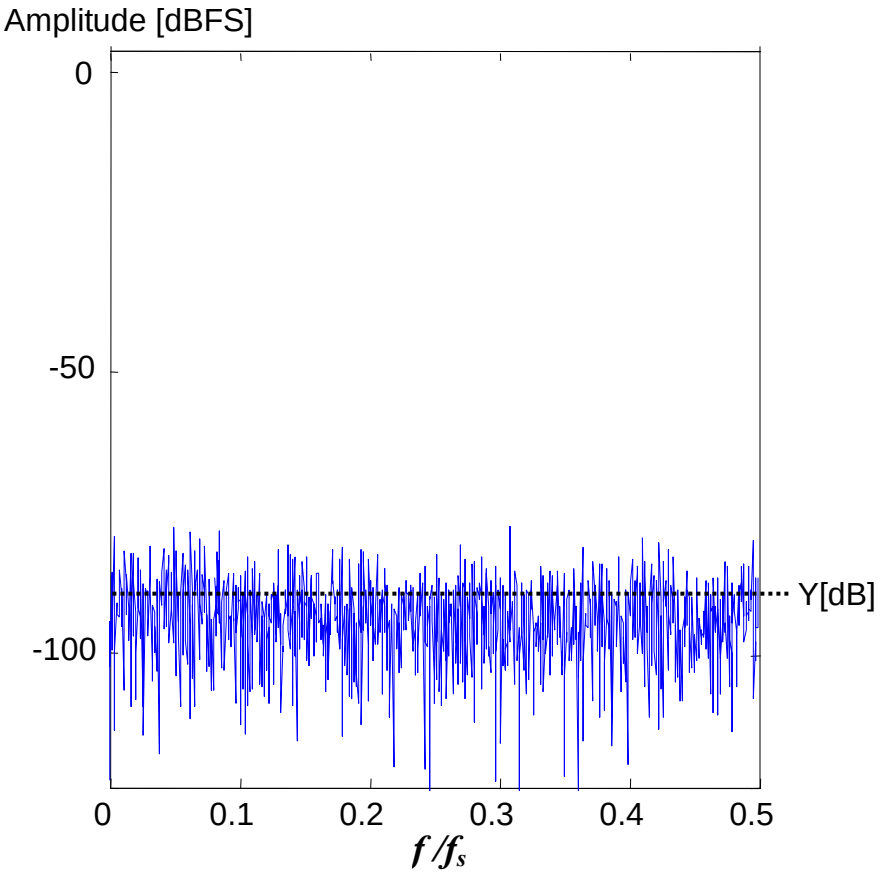
Find the ADC sampling frequency, f_s, as a function of f_B.
What is the maximum number of bits (resolution) for the ADC such that the aliased in-band components do not show up at the digital output?



Problem 3: You are to complete the spectral test graph for a **12bit** ADC converter with sampling frequency ~ **1MHz**. Spectral testing is performed by using a full-scale **sinusoidal input at 300kHz** and Fast Fourier analysis (FFT) with number of samples $\mathbf{N=2^{10}}$.

a) Draw the input signal on the spectral test graph assuming no windowing required.
b) Compute the ideal **SQNR** for this ADC.
c) The measured INL is shown in the figure below and $\mathbf{DNL^{max}}$ is measured to be **0.5LSB**. Compute the overall **SQNR** using the results for DNL or INL (whichever affects SQNR).
d) By raising the chip temperature and remeasuring the SNR, the effect of thermal noise is estimated as **5dB extra SNR degradation** at the ambient temperature. Find the overall SNR at the ambient temperature.
e) Using the results found in d), find the value for the noise floor level shown as **Y** on the spectral test graph.
f) What is the **SFDR** of this converter in terms of dB? Add the dominant distortion component within the band of interest on the spectral test graph.
g) Compute the SNDR for the above input signal and find **ENOB** based on **SNDR**.
h) Is this ADC monotonic?





Problem 4:
Please answer the following questions: In the case of ***True/False*** underline either True or False

1. The time delay for 3 sinusoidal signals applied to the input of a low pass filter at different frequencies was measured to be all equal to 2msec. If all 3 signals are within the passband of the filter:
    a. What is the most likely type of the filter among all EE247 filters (e.g. Chebychev, Butterworth…..)?
    b. What is the relationship between phase and frequency within passband?
    c. What is the group delay within the passband?

2. Name a filter type which includes transmission zeros. What is the advantage of adding zeros?

3. Among the filter topologies studies in EE247 which one/s are more suited for operation at higher frequencies? Name an application where this filter topology is used.

4. Among the entire continuous-time filter topologies studied in EE247, which one has the potential for highest linearity performance?

5. Name one major advantage of switched-capacitor filters over continuous-time filters in the integrated form?

6. What is the main disadvantage of switched-capacitor filters?

7. In switched-capacitor networks, signal distortion due to slew-limited settling of the integrator is more severe compared to the distortion associated with exponential settling. ***True or False?***

8. Addition of an integrator in the feedback path of a lowpass filter results in:
    a. The addition of a **pole** or **zero** (choose one) in the transfer function.
    b. Therefore changes the shape to:_____
    c. Can be used to cancel _____

9. A continuous-time filter is tuned by operating in conjunction with a master-slave style continuously operating tuning circuit. Name one factor which could potentially limit the minimum signal handling capability of the slave filter.

10. An RLC lowpass filter is transformed to bandpass by:_____ _____. The resulting bandpass filter order is _____compared to the original lowpass prototype.

11. For an ADC, DNL: is measured to be [0 -0.5 0 -1 +0.5 +0.5 +0.5 0], Find the INL vector. Comment on the ADC performance.

12. What are the advantages and disadvantages of binary-weighted versus unit-element DACs?

13. A segmented DAC is made of B_2 MSB bits with _____architecture and B_1 LSB bits with _____architecture. The overall DNL is equal to the DNL of _____.

14. Typically, what limits the maximum achievable resolution in Nyquist rate ADCs and to about how many bits?

15. Histogram testing using ramp signal is typically limited to ___bit ADCs due to ____ _____

16. Using a sinusoidal signal instead of a ramp in histogram testing of ADCs has the advantage of: _____ _____

17. What are the disadvantage/s of histogram testing?

18. In the context of ADC spectral testing, under what conditions windowing is used?

19. Considerations for performing spectral testing without using windowing: are:
    a. To avoid spectral leakage_____
    b. Avoid periodical quantization noise and thus lose of measurement accuracy by_____
    c. To speed up the computation choose:_____