UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Midterm Exam & Solution **EECS 247**
H. Khorramabadi **Thurs, October 28, 2010** **FALL 2010**

Name: _____

SID: _____

Score: **/40**

Problem 1 6point	Problem 2 6point	Problem 3 6point	Problem 4 22point	Total Score 40point

- **Closed books and notes, no calculators allowed**
- **Mark all results with a box around.**
- Write solutions on the exam sheets. Add extra pages where needed.
- Simplify algebraic results as much as possible.
- Bring into standard form where applicable.
- Show derivations.

Useful Expressions:

$log_{10}\,2=0.3, \quad log_{10}\,3=0.477, \quad log_2\,3=1.59$

$2^6=64, \quad 2^7=128, \quad 2^8=256, \quad 2^9=512, \quad 2^{10}=1024$

decade=x10

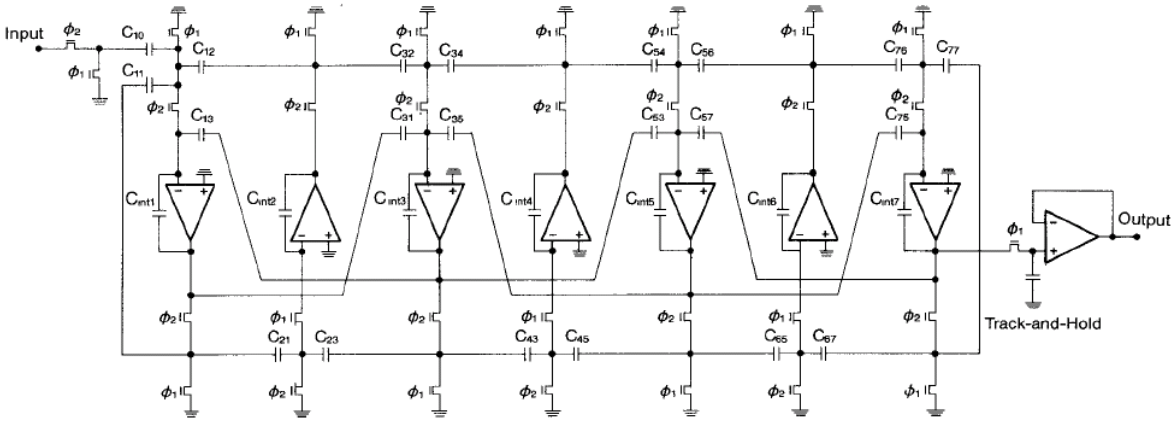
$\frac{1}{1+x} \approx 1-x$ for x small

$\sqrt{1+x} \approx 1+\frac{x}{2}$ for x small

Problem 1: The circuit shown below is a filter.

a) Identify the filter type (low/high/band pass). **Low-pass**
b) What is the order of the filter? **7**
c) Does it include transmission zeros? If the answer is positive, which components are added for this purpose? **Yes, C13, C31, C35,C53,C57,C75**
d) Is it utilizing bottom-plate integrator technique? **Yes**

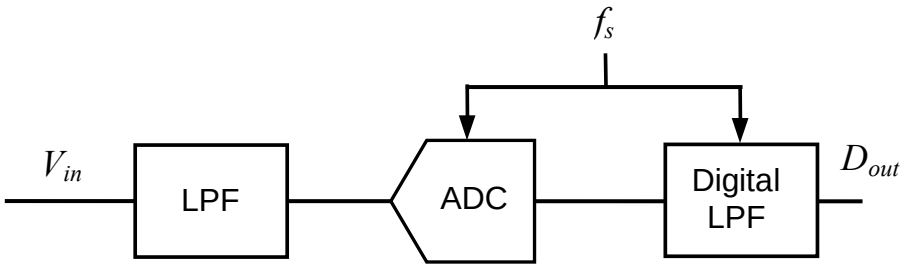
e) Is it an LDI implementation? Show your answer. **Yes. For example the first two integrators are connected in: $[1/(1-Z^{-1})]x[Z^{-1}/(1-Z^{-1})]$ which results in an LDI loop**
f) Identify the components whose values influence the total output noise, assuming the opamp noise is negligible (no derivation necessary). Cint1 thru Cint7
g) To reduce the overall thermal noise by a factor of 2 without changing internal node transfer functions what should be done? **To decrease output noise voltage by 2 increase all Cs by X4**
h) To scale the gain of the output node by a factor of 1.5 how would you change the output stage?
All Capacitors connected to the output node x1/1.5→ Cint7, C57, C67, C77 divided by 1.5
i) If double-sampling is to be added to this design, show how it is done by drawing only two stages. A 2nd set of sampling Cs and switches is added in parallel with the original ones while the clock phases would be reversed.
j) What would the effect of double-sampling be on the performance of the filter, assuming the clock frequency and all capacitor values remain the same? **What is the advantage of double-sampling? The effective sampling rate is double the clock frequency, in other words, if all Cs remain the same, the bandwidth of the filter is doubled, while the opamp requirements remains the same as before. Results in lower power dissipation and Si area.**



Problem 2: The receive path of a system comprises a continuous-time lowpass filter followed by an ADC converter. Assume the following:

- The signal bandwidth of interest spans from 0 to f_B.
- The incoming signal is wideband with equal signal magnitude for all frequencies.
- The filter has a roll-off starting at $2f_B$ with ***20dB-per-decade-per-pole*** and with **2 poles**.
- The digital filter cuts sharply at f_B.
- First, an ADC with very high resolution is used. The measured highest aliased component at the output D_{out} is at ***-40dB*** level with respect to the in-band signal. Ignore magnitude response shaping due to the sample/hold effect.

a) Find the ADC sampling frequency, f_s, as a function of f_B.
b) What is the maximum number of bits (resolution) for the ADC such that the aliased in-band components do not show up at the digital output?



a) Since LPF roll-off is 40dB/decade, there should be one decade or x10 ratio between and the largest aliasable signal which is at (f_s -f_B)and filter roll-off $2f_B$:

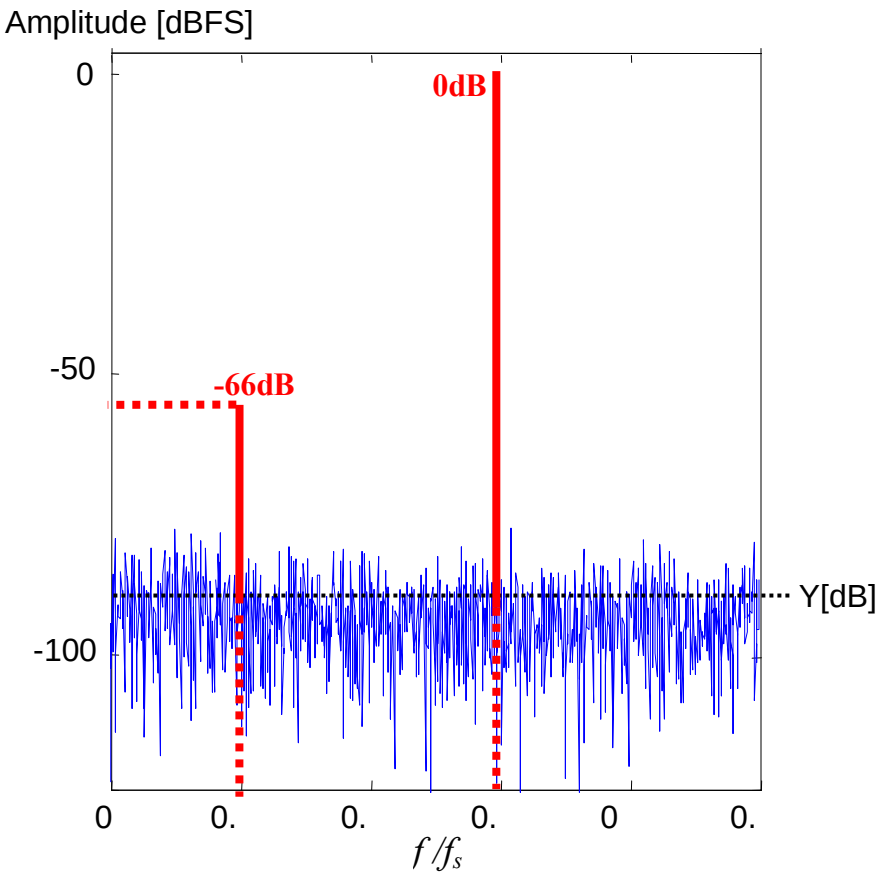
$(f_s-f_B)/2f_B=10$ → $\underline{f_s=21f_B}$

b) Maximum ADC resolution: 1LSB should be smaller than aliased component→1LSB smaller than 1/100 of full-scale → 1/128<LSB <1/64 → **6bit ADC**

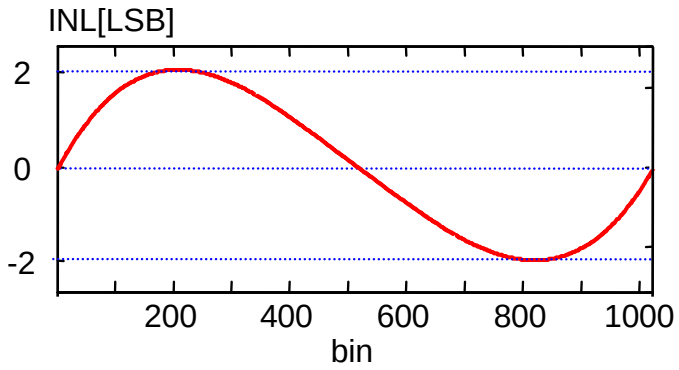
Problem 3: You are to complete the spectral test graph for a **12bit** ADC converter with **sampling frequency 1MHz**. Spectral testing is performed by using a full-scale **sinusoidal input at 300kHz** and Fast Fourier analysis (FFT) with number of samples $\mathbf{N=2^{10}}$.

a) Indicate the input signal on the spectral test graph.
b) Compute the ideal **SQNR** for this ADC.
c) The measured INL is shown in the figure below and DNL^{max} is measured to be 0.5LSB. Compute the overall **SQNR** using the results for DNL or INL (whichever affects SQNR).
d) By raising the chip temperature and remeasuring the SNR, the effect of thermal noise is estimated as **5dB extra SNR degradation** at the ambient temperature. Find the overall SNR at the ambient temperature.
e) Using the d) result, find the value for the noise floor level shown as **Y** on the spectral test graph.
f) What is the **SFDR** of this converter in terms of dB. Add the dominant distortion component which falls within the band of interest on the spectral test graph.
g) Compute the SNDR for the above input signal and find **ENOB** based on **SNDR**.

h) Is this ADC monotonic?



a) The signal normalized to sampling freq: → **0.3**
b)SQNR=6.02x12+1.76=74dB
c)DNL causes increase in quantization noise. 1/2LSB DNL → -3dB loss is SNR
→ SNR=71dB
d)Thermal noise add 5dB to the total noise SNR=71-5=**66dB**
e)Noise floor lower by: $10\log N/2=10\log 2^{10}/2=10x9\log 2=27dB$
→ noise floor @ -66-27=-93dB → **Y=-93dB**
f)SFDR=$20\log 2^{12}$/INL=$20\log 2^{12}/2=20x11\log 2=66dB$ → **SFDR=66dB**
Due to the shape of the INL, dominant distortion mostly 3rd order harmonic → f3rd/fs=0.9
causing inband aliased component at (fs-f3rd)/fs=1-0.9=**0.1** normalized to fs
g) To compute SNDR, noise and distortion is vector added since they seem to have the same value individually, power addition would result in 66dB-3dB→ **SNDR= 63dB**
ENOB=(63-1.76)/6.02→ **ENOB=10.1bit**
h) Since DNL<1 **ADC is monotonic**.



Problem 4:

Please answer the following questions: In the case of ***True/False*** underline either True or False

1. The time delay for 3 sinusoidal signals applied to the input of a low pass filter at different frequencies was measured to be all equal to 2msec. If all 3 signals are within the passband of the filter:
   a. What is the most likely type of the filter among all EE247 filters (e.g. Chebychev, Butterworth…..)? **Bessel**
   b. What is the relationship between phase and frequency within passband? **$\theta(\omega)=-2msec x\omega$**
   c. What is the group delay within the passband? **-2msec**

2. Name a filter type which includes transmission zeros. What is the advantage of adding zeros? **Elliptic or Chebychev II. Advantage: creates nulls which could be used to eliminate interfering signal/s. Shaper transition band.**

3. Among the filter topologies studies in EE247 which one/s are more suited for operation at higher frequencies? Name an application where this filter topology is used.
   Gm-C type filters. Disk drive applications, xDSL filters….

4. Among the entire continuous-time filter topologies studied in EE247, which one has the potential for highest linearity performance? **Opamp-RC type.**

5. Name one major advantage of switched-capacitor filters over continuous-time filters in the integrated form**? Critical frequency inherently accurate since it is a function of clock freq. & C ratios. Long time-constants can be implemented in small area.**

6. What is the main disadvantage of switched-capacitor filters? **Since it is a sampled system to avoid aliasing an anti-aliasing filter is required.**

7. In switched-capacitor networks, signal distortion due to slew-limited settling of the integrator is more severe compared to the distortion associated with exponential settling. ***True or False?***

8. Addition of an integrator in the feedback path of a lowpass filter results in:
   a. The addition of a **pole** or **zero** (choose one) in the transfer function.
   b. Therefore changes the shape to:_**Bandpass**_____
   c. Can be used to cancel _**DC offset**_____

9. A continuous-time filter is tuned by operating in conjunction with a master-slave style continuously operating tuning circuit. Name one factor which could potentially limit the minimum signal handling capability of the slave filter. **Reference signal feedthrough via parasitic coupling to the output of the slave filter.**

10. An RLC lowpass filter is transformed to bandpass by:_**Replacing all Cs parallel by combination of L&C and all Ls by series L &C. The resulting bandpass filter order is _x2_compared to the original lowpass prototype.**

11. For an ADC, DNL: is measured to be [0 -0.5 0 -1 +0.5 +0.5 +0.5 0], Find the INL vector. Comment on the ADC performance. **INL:[_0 -0.5 -0.5 -1.5 -1 -0.5 0 _]. One missing code.**

12. What are the advantages and disadvantages of binary-weighted versus unit-element DACs? **Binary-weighted: Advantages, lower number of switched required, incoming binary digital input can be directly used w/o decoding. Disadvantage is poor DNL performance.**
Unit-element: Advantages, excellent DNL performance. Disadvantage : large number of switched required, incoming binary digital input cannot be directly used and needs a decoder.

13. A segmented DAC is made of B_2 MSB bits with **unit-element** architecture and B_1 LSB bits with **binary-weighted** architecture. The overall DNL is equal to the DNL of a **B1+1 bit binary-weighted DAC.**

14. Typically, what limits the maximum achievable resolution in Nyquist rate ADCs and to about how many bits? **KT/C noise associated with the switch R and sampling C of the sampling network mandates large C for high resolution ADCs. Limit is about 14bits.**

15. Histogram testing using ramp signal is typically limited to **8 to 10** bit ADCs **due to linearity limitations of a ramp signal.**

16. Using a sinusoidal signal instead of a ramp in histogram testing of ADCs has the advantage of: _**Any non-linearity related harmonic content of the sinusoidal signal source can be filtered out.**

17. What are the disadvantage/s of histogram testing? **Flipped codes can not be detected. Non-monotonicity not detected. Slow**

18. In the context of ADC spectral testing, under what conditions windowing is used? **If the provisions to lock sampling signal frequency to input signal is not available.**

19. Considerations for performing spectral testing without using windowing: are:
    a. To avoid spectral leakage_**Integer number of cycles of input signal is used.**

    b. Avoid periodical quantization noise and thus lose of measurement accuracy by_**having f_s/f_{in} non-integer number.**

    c. To speed up the computation choose:_**$N=2^n$ with n an integer**