UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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Due Tues., Nov. 30th (or earlier), 2010 **FALL 2010**

Objective

The objective of this project is to obtain experience with design of ADC converters. Using the 65nm technology with models obtained from the website:

http://www.eas.asu.edu/~ptm/modelcard/65nm_bulk.txt

You can explore the technology device characteristics at:

http://www.eas.asu.edu/~ptm/

Design an ADC converter with the following specifications:

Supply voltage is 1.1V.

Signal bandwidth spans from DC to 150MHz.

The overall number of bits for the ADC is 6 and you can use architecture of your choice (e.g. Flash, Flash + folding and/or interpolation, Pipelined…….).

The reference voltage starts from 0V and 1LSB=10mV, target your design for 0.5LSB accuracy and 3σ yield.

If you are using a latched comparator, you can make the following assumptions:

- The latch only portion has a 1sigma offset of 25mV. Ignore all latch actual device offset.
- For amplifier design, device matching is a function of device area only (neglect the effect of threshold voltage mismatch) and is governed by: $\sigma_{Voffset}$=8mV/sqrt(WxL) [μ], for device L equal or greater than 0.10μ. Device matching degrades rapidly for smaller device lengths. Ignore load device mismatch effects and only consider the input device offset.
- You can use ideal current sources where needed.
- If your design uses a comparator, the Yukawa comparator is a good starting point. The preamp gain must be high enough to reduce the effect of latch offset to a tolerable level. Too high of a preamp gain would result in not enough bandwidth and thus slow settling. The input device minimum area is based on the input referred offset. If you are using interpolation, note that preamp gain must be chosen accordingly.
- You have the option of using offset cancellation. However, consider the fact that you may have to allocate part of the clock signal duration for this purpose.

Resistive material available is polysilicon with 20OHM/square sheet resistivity and is formed on top of 1micron silicon dioxide. Include the associated parasitic capacitance (if it affects your design) in your simulations by adding half of the capacitance to each side.

From resistor matching point of view, each resistor should have a minimum area of $100\mu m^2$ with minimum width of 1μ and from area limitation point of view, maximum area of $500\mu m^2$.

If you use precision capacitors, the capacitive material has bottom plate parasitic to ground in the order of 10% of capacitor value.

If you are using capacitors, assume Cs can be matched to better than 0.2% by choosing minimum unit C > or = 0.1pF.
Please simulate the dynamic power dissipation and add it to static power dissipation.
Report both contributions as well as the total power dissipation.

Beware of comparator kickback and input signal feedthrough affecting the resistive DAC tap voltages if you are using Flash architecture. This could affect your choice of resistor value for the DAC.

The main objective of this project is to come up with a design for the 6bit ADC with minimum static+dynamic power dissipation.

The design is to be performed considering only nominal model conditions and nominal temperature of 27degree C (in real designs worst case conditions are identified and designed for).

You can use software coding to emulate the digital backend. In other words, your actual circuit level design stops at thermometer code level if you are using Flash architecture.

Assume the backend conversion takes up no extra time. You have the option of converting the thermometer code back to analog via a simple software DAC. Note that after the output of the latches are fully settled to "1"s and "0"s, by adding up all the output codes and scaling the final result accordingly, the digitized signal is converted back to analog. Spectral testing on the analog output reveals ADC non-idealities. In other architectures, the digital signal processing can be performed in software as needed.

Project report structure:

You are to submit a concise project report that documents your design procedure and obtained results. Your report should be formatted as indicated below:

(1): Hand calculations and analysis that leads to the design.

(2): Circuit schematics.

(3): Simulation results for the following:

a) If applicable comparator performance e.g. overload recovery simulated assuming the full 6-bit worst-case signal scenario.

b) Input a sinusoidal signal with full-scale amplitude via an ideal voltage source with 50OHM source impedance (you can repeat your simulation with 0 source impedance to explore the effect of finite source resistance). Measure distortion and noise by performing FFT preferably without requiring windowing (choose the number of input signal cycles to be a prime number such as 61 cycles and $N=2^8$ so that there are enough unique samples for the required measurement accuracy) for the following cases:

- Incoming signal frequency close to 15MHz first and then the full bandwidth signal and amplitude close to full-scale and no non-idealities added (to check the correctness of your FFT procedure, perform a spectrum analysis on the input voltage source first).
- Same as the above, plus 2.5xσ offset added to 4 of the comparators and latches at random. (you need to compute the preamp offset based on the input device size). If you are not using a Flash architecture perform a similar analysis relevant to your particular architecture.
- Same as the above, but 6σ offset added to 4 of the amplifiers, comparators, and latches at random. If you are not using a Flash architecture perform a similar analysis relevant to your particular architecture.

Compare the performance with respect to noise and distortion for the three above cases.

(4): Final results for minimum power dissipation for the 6-bit ADC and conclusions.

Appendix: Code used for simulation.

Teamwork

It is preferred that you work in groups of two and submit a joint report. Discussions with others and the instructor are encouraged, but each group should submit a genuine design.

Presentation

- The reports are due latest Nov 30th. When you are finished with the design/simulation/report, make an appointment with the instructor via email to discuss your work in person on Dec. 1st.
- Prepare a 10 minute PowerPoint presentation per person to be presented to the class during the Dec. 2nd or Dec. 7th sessions. Please plan to attend both sessions.