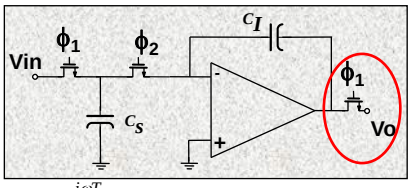
EE247
Lecture 10

- Switched-capacitor filters (continued)
  - DDI integrators
  - LDI integrators
    - Effect of parasitic capacitance
    - Bottom-plate integrator topology
  - Switched-capacitor resonators
  - Bandpass S.C. filters
  - Lowpass S.C. filters
  - Switched-capacitor filter design considerations
    - Termination implementation
    - Transmission zero implementation
    - Effect of non-idealities
  - Switched-capacitor filters utilizing double sampling technique

DDI Switched-Capacitor Integrator



$$\frac{V_O}{V_{in}}(z) = -\frac{C_S}{C_I} \times \frac{z^{-1}}{1-z^{-1}} = \frac{C_S}{C_I} \times \frac{1}{1-z}, \quad z = e^{j\omega T}$$

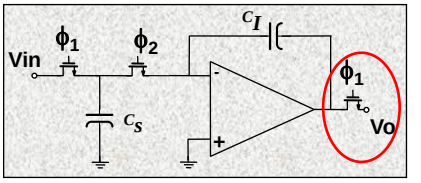
$$= \frac{C_S}{C_I} \times \frac{1}{1-e^{j\omega T}} = \frac{C_S}{C_I} \times \frac{e^{-j\omega T/2}}{e^{-j\omega T/2}-e^{j\omega T/2}} \quad since: \quad \sin\alpha = \frac{e^{j\alpha}-e^{-j\alpha}}{2j}$$

$$= -j\frac{C_S}{C_I} \times e^{-j\omega T/2} \times \frac{1}{2\sin(\omega T/2)}$$

$$= -\frac{C_S}{C_I}\frac{1}{j\omega T} \times \frac{\omega T/2}{\sin(\omega T/2)} \times e^{-j\omega T/2}$$

Ideal Integrator — Magnitude Error — Phase Error

DDI Switched-Capacitor Integrator



$$\frac{V_O}{V_{in}}(z) = = -\frac{C_S}{C_I}\frac{1}{j\omega T} \times \frac{\omega T/2}{sin(\omega T/2)} \times e^{-j\omega T/2}$$

Magnitude Error

Phase Error

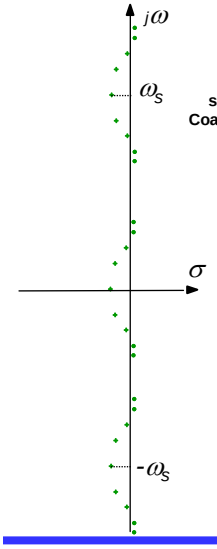
Example: Mag. & phase error for:

1- f/f_s=1/12 → Mag. error = 1% or 0.1dB
Phase error=15 degree
Q_{intg} = -3.8

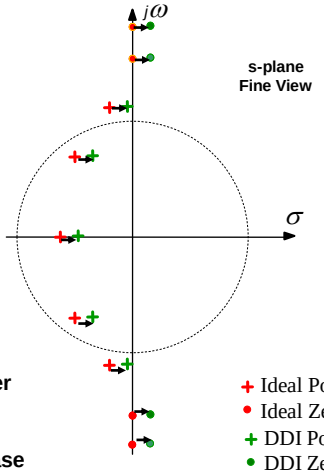
2- f/f_s=1/32 → Mag. error=0.16% or 0.014dB
Phase error=5.6 degree
Q_{intg} = -10.2

DDI Integrator:
→ magnitude error no problem
phase error major problem

5th Order Low-Pass Switched Capacitor Filter Built with DDI Integrators



s-plane
Coarse View

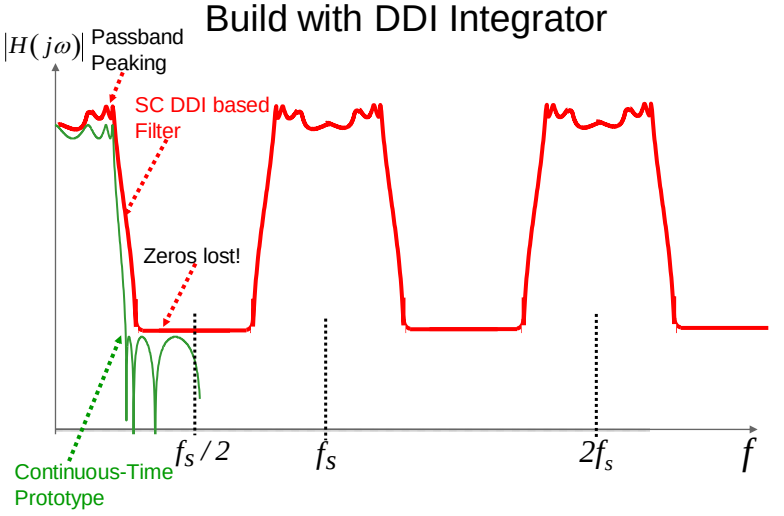


s-plane
Fine View

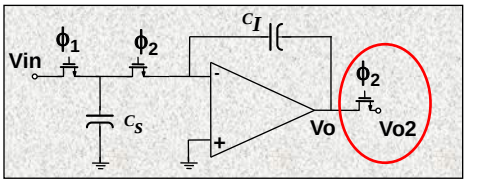
Example:
5th Order Elliptic Filter
Singularities pushed towards RHP due to integrator excess phase

+ Ideal Pole
• Ideal Zero
+ DDI Pole
• DDI Zero

Switched Capacitor Filter Build with DDI Integrator



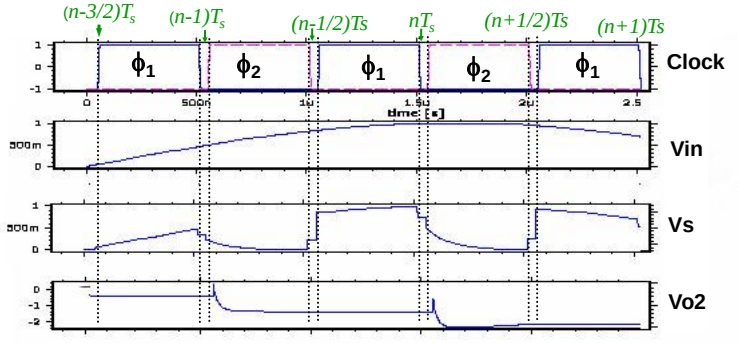
Switched-Capacitor Integrator Output Sampled on $\phi 2$



Sample output ½ clock cycle earlier

→ Sample output on ϕ_2

Switched-Capacitor Integrator
Output Sampled on ϕ2



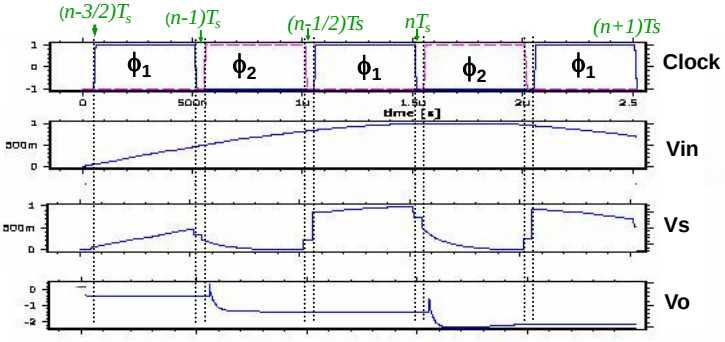
$\Phi_1 \rightarrow$ $Q_s[(n-1)T_s] = C_s V_i[(n-1)T_s]$, $Q_I[(n-1)T_s] = Q_I[(n-3/2)T_s]$

$\Phi_2 \rightarrow$ $Q_s[(n-1/2)T_s] = 0$, $Q_I[(n-1/2)T_s] = Q_I[(n-3/2)T_s] + Q_s[(n-1)T_s]$

$\Phi_1 \rightarrow$ $Q_s[nT_s] = C_s V_i[nT_s]$, $Q_I[nT_s] = Q_I[(n-1)T_s] + Q_s[(n-1)T_s]$

$\Phi_2 \rightarrow$ $Q_s[(n+1/2)T_s] = 0$, $Q_I[(n+1/2)T_s] = Q_I[(n-1/2)T_s] + Q_s[nT_s]$

Switched-Capacitor Integrator
Output Sampled on ϕ2



$Q_I[(n+1/2)T_s] = Q_I[(n-1/2)T_s] + Q_s[nT_s]$

$V_{o2} = -Q_I/C_I$ & $V_i = Q_s/C_s \rightarrow C_I V_{o2}[(n+1/2)T_s] = C_I V_{o2}[(n-1/2)T_s] - C_s V_i[nT_s]$

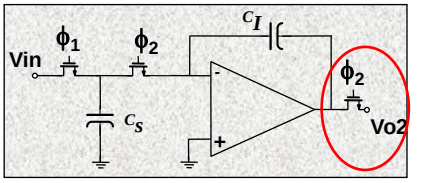
Using the z operator rules:

$\rightarrow C_I V_{o2} z^{1/2} = C_I V_{o2} z^{-1/2} - C_s V_i$

$$\frac{V_{o2}}{V_{in}}(z) = -\frac{C_s}{C_I} \times \frac{z^{-1/2}}{1-z^{-1}}$$

LDI Switched-Capacitor Integrator

LDI (Lossless Discrete Integrator) → same as DDI but output is sampled ½ clock cycle earlier



LDI

$$\frac{V_{o2}}{V_{in}}(z) = -\frac{C_S}{C_I} \times \frac{z^{-1/2}}{1-z^{-1}}, \quad z = e^{j\omega T}$$

$$= -\frac{C_S}{C_I} \times \frac{e^{-j\omega T/2}}{1-e^{-j\omega T}} = \frac{C_S}{C_I} \times \frac{1}{e^{-j\omega T/2} - e^{+j\omega T/2}}$$

$$= -j\frac{C_S}{C_I} \times \frac{1}{2\sin(\omega T/2)}$$

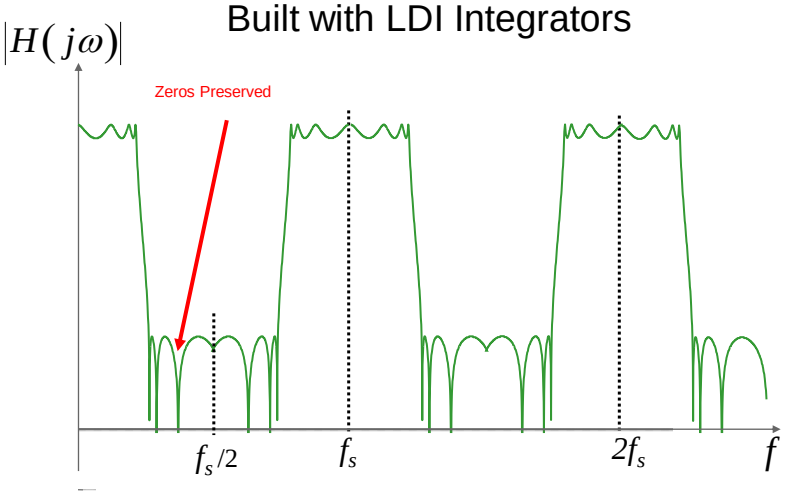
$$= -\frac{C_S}{C_I}\frac{1}{j\omega T} \times \frac{\omega T/2}{\sin(\omega T/2)}$$

Ideal Integrator

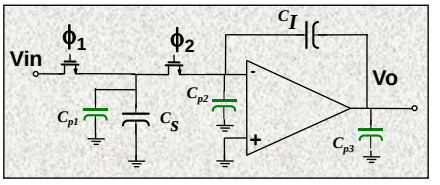
Magnitude Error

No Phase Error!
For signals at frequencies << sampling freq.
→ Magnitude error negligible

Switched-Capacitor Filter Built with LDI Integrators



Switched-Capacitor Integrator
Parasitic Capacitor Sensitivity



Effect of parasitic capacitors:

1- C_{p3} – driven by opamp o.k.

2- C_{p2} – at opamp virtual gnd o.k.

3- C_{p1} – Charges to Vin & discharges into C_I,

– C_{p1} includes the MOS switch junction capacitors which are voltage dependent, not only affects C ratios but results in non-linearities

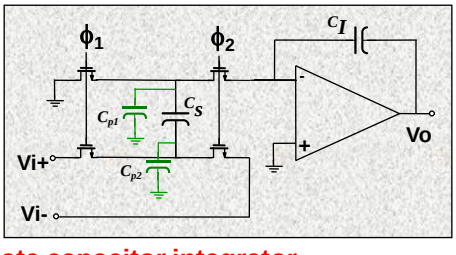
→ Problem parasitic capacitor sensitivity

Parasitic Insensitive
Bottom-Plate Switched-Capacitor Integrator

Sensitive parasitic cap. → C_{p1} → rearrange circuit so that C_{p1} does not charge/discharge

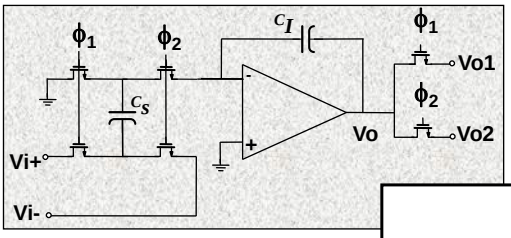
ϕ1=1 → C_{p1} grounded

ϕ2=1 → C_{p1} at virtual ground



Solution: Bottom plate capacitor integrator

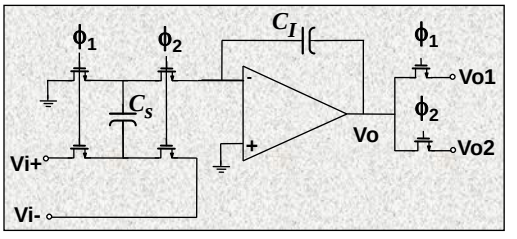
Bottom Plate Switched-Capacitor Integrator

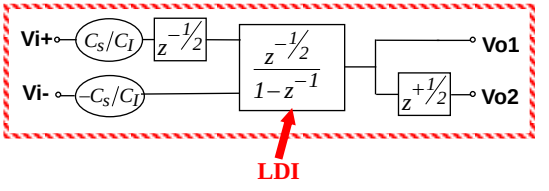


Output/Input *z*-Transform		
	Vo1 on ϕ_1	Vo2 on ϕ_2
Vi+ on ϕ_1	$\frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}}$	$\frac{C_S}{C_I}\frac{z^{-1/2}}{1-z^{-1}}$
Vi- on ϕ_2	$-\frac{C_S}{C_I}\frac{z^{-1/2}}{1-z^{-1}}$	$-\frac{C_S}{C_I}\frac{1}{1-z^{-1}}$

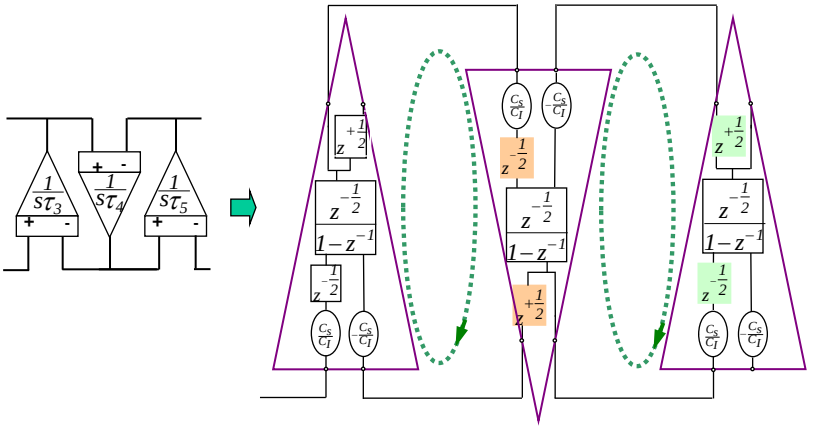
Note:
Different delay from Vi+ & Vi- to either output
→ Special attention needed for input/output connections to ensure LDI realization

Bottom Plate Switched-Capacitor Integrator z-Transform Model





LDI Switched-Capacitor Ladder Filter

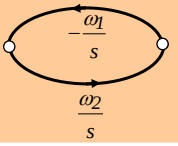


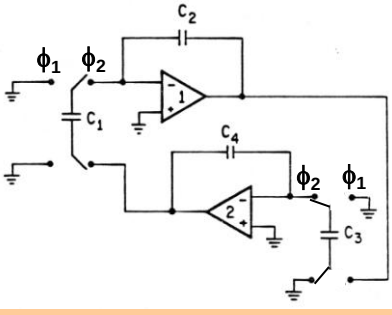
To test whether LDI or DDI → Need to examine delay around the integrator loop

Delay around integrator loop is ($z^{-1/2} \cdot z^{+1/2} = 1$) → LDI function

Switched-Capacitor LDI Resonator

Resonator Signal Flowgraph



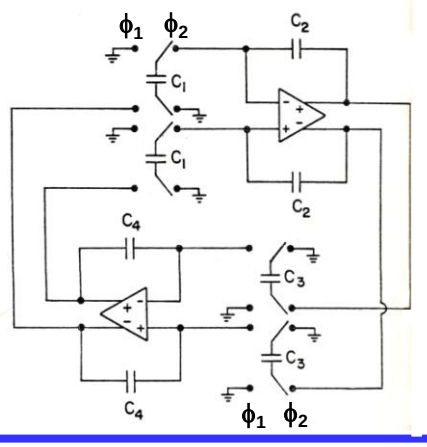


$$\omega_1 = \frac{1}{R_{eq1} C_2} = f_s \times \frac{C_1}{C_2}$$

$$\omega_2 = \frac{1}{R_{eq3} C_4} = f_s \times \frac{C_3}{C_4}$$

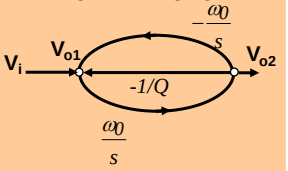
Fully Differential Switched-Capacitor Resonator

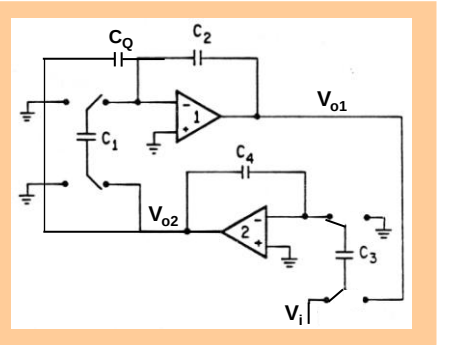
• Note: Two sets of S.C. bottom plate networks for each differential integrator



Switched-Capacitor LDI Bandpass Filter Utilizing Continuous-Time Termination

Bandpass Filter Signal Flowgraph



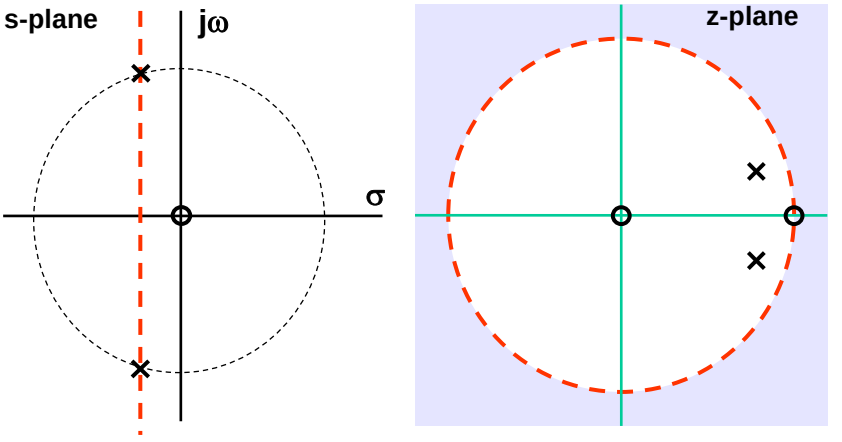


Feedback in the amount of *-1/Q* provided from V_{o2} to V_{o1} via the addition of capacitor C_Q

$$\omega_0 = f_s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2}$$

$$Q = \frac{C_2}{C_Q}$$

Example: 2nd Order S.C. Bandpass Filter s-Plane versus z-Plane



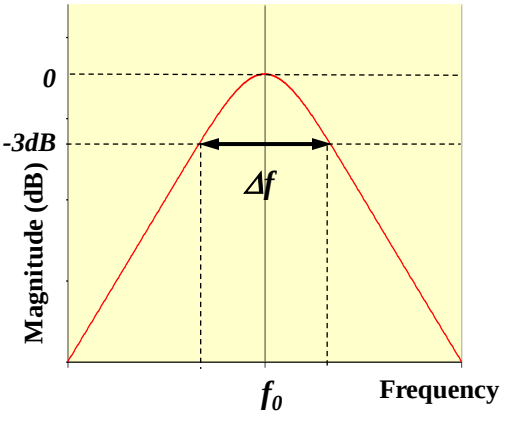
Switched-Capacitor LDI Bandpass Filter Continuous-Time Termination

$$f_0 = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2}$$

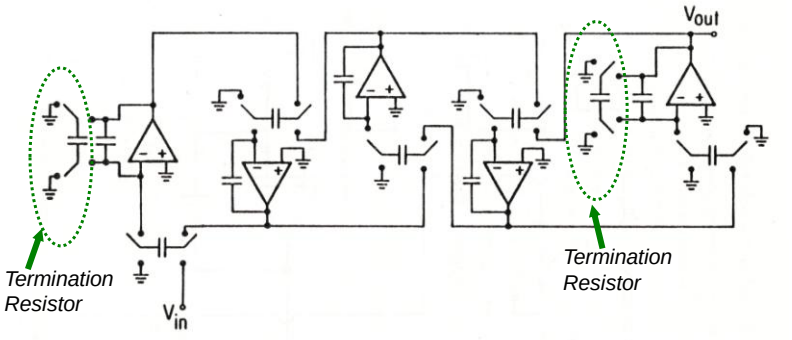
$$\Delta f = \frac{f_0}{Q}$$

$$= \frac{1}{2\pi} f_s \times \frac{C_1 C_Q}{C_2 C_2}$$

Both f_0 and Δf accurately determined by cap ratios & clock frequency



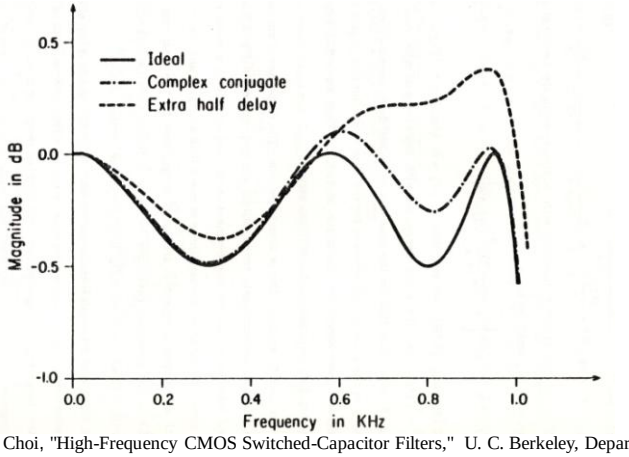
Fifth Order All-Pole LDI Low-Pass Ladder Filter
Complex Conjugate Terminations



- Complex conjugate terminations (alternate phase switching)

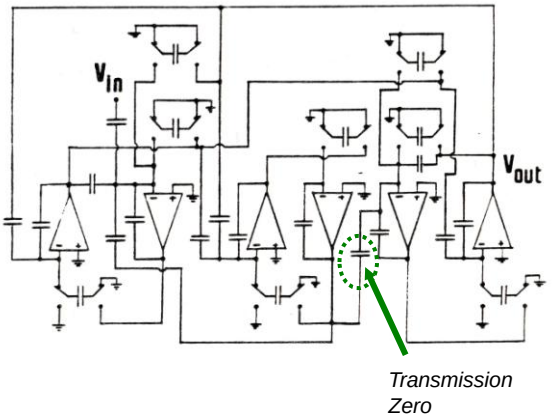
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Fifth-Order All-Pole Low-Pass Ladder Filter
Termination Implementation



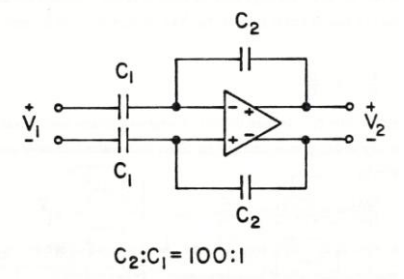
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth-Order Elliptic LDI Bandpass Filter

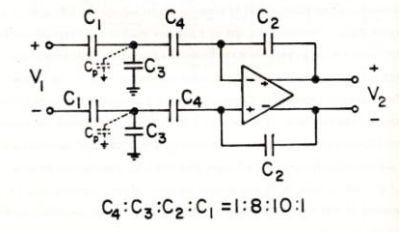


Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Use of T-Network



$$\frac{V_2}{V_1} = -\frac{C_1}{C_2}$$

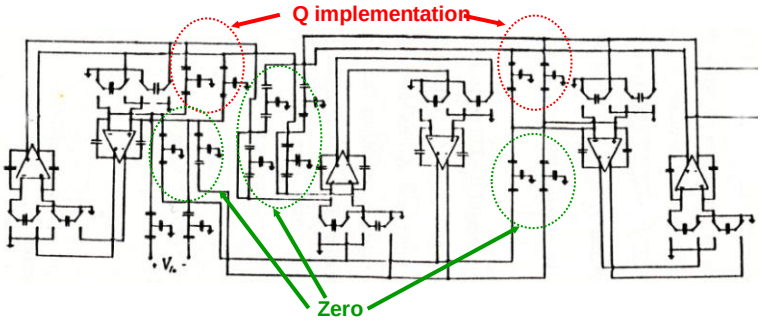


$$\frac{V_2}{V_1} = -\frac{C_1}{C_2} \times \frac{C_4}{C_1 + C_3 + C_4}$$

High Q filter → large cap. ratio for Q & transmission zero implementation
To reduce large ratios required → T-networks utilized

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth Order Elliptic Bandpass Filter Utilizing T-Network



- **T-networks utilized** for:
  - **Q implementation**
  - **Transmission zero implementation**

Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Effect of Opamp Nonidealities on Switched Capacitor Filter Behavior

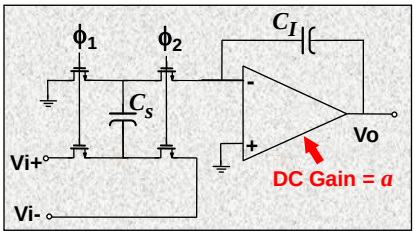
- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity- usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

Effect of Opamp Non-Idealities
Finite DC Gain

$$H(s) \approx -f_s \frac{C_S}{C_I} \frac{1}{s + f_s \frac{C_S}{C_I} \times \frac{1}{a}}$$

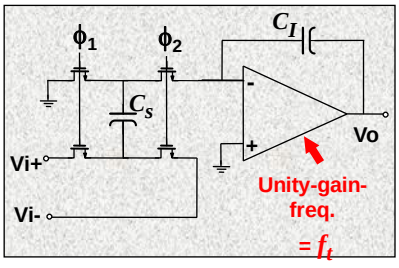
$$H(s) \approx \frac{-\omega_o}{s + \omega_o \times \frac{1}{a}}$$

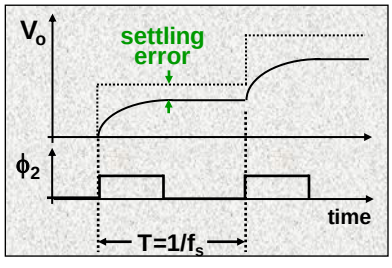
$$\Rightarrow \boxed{Q_{intg} \approx a}$$



- **Finite DC gain same effect in S.C. filters as for C.T. filters**
- **If DC gain not high enough → lowing of overall Q & droop in passband**

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





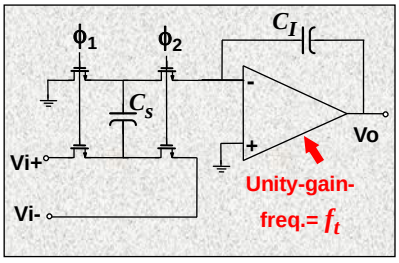
Assumption-

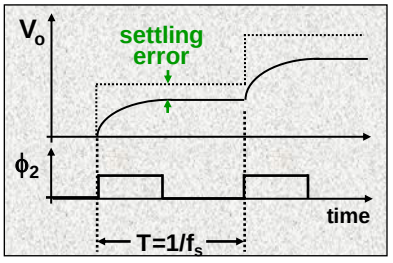
Opamp → does not slew (will be revisited)

Opamp has one pole only → exponential settling

Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Non-Idealities
Finite Opamp Bandwidth





$$H_{actual}(Z) \approx H_{ideal}(Z)\left[1 - e^{-k} + e^{-k} \times \frac{C_I}{C_I + C_S} Z^{-1}\right]$$

$$where \quad k = \pi \times \frac{C_I}{C_I + C_S} \times \frac{f_t}{f_s}$$

$f_t \rightarrow$ *Opamp unity-gain-frequency* , $f_s \rightarrow$ *Clock frequency*

Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Effect of Opamp Finite Bandwidth on Filter Magnitude Response

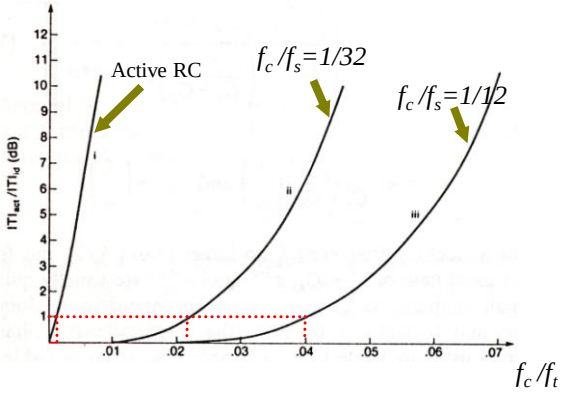
$|T|_{non-ideal} / |T|_{ideal}$ *(dB)*

Example:
For 1dB magnitude response deviation:

1- $f_c/f_s=1/12$
$f_c/f_t \sim 0.04$
→ $f_t > 25 f_c$

2- $f_c/f_s=1/32$
$f_c/f_t \sim 0.022$
→ $f_t > 45 f_c$

3- *Cont.-Time*
$f_c/f_t \sim 1/700$
→ $f_t > 700 f_c$



Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

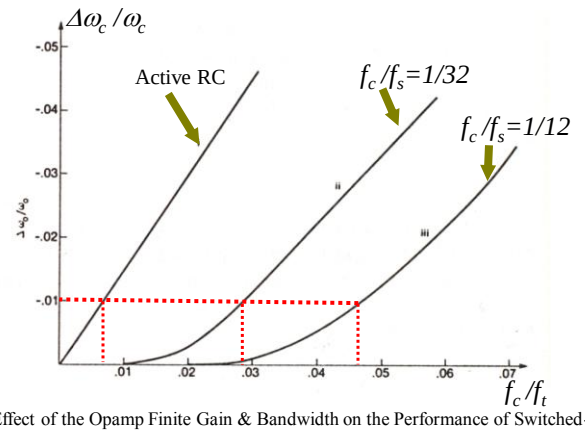
Effect of Opamp Finite Bandwidth on Filter Critical Frequency

Example:
For maximum critical frequency shift of <1%

1- $f_c/f_s=1/32$
$f_c/f_t\sim0.028$
→ $f_t>36f_c$

2- $f_c/f_s=1/12$
$f_c/f_t\sim0.046$
→ $f_t>22f_c$

3- *Active RC*
$f_c/f_t\sim0.008$
→ $f_t>125f_c$



Ref: K.Martin, A. Sedra, "Effect of the Opamp Finite Gain & Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug 1981.

Opamp Bandwidth Requirements for Switched-Capacitor Filters Compared to Continuous-Time Filters

- Finite opamp bandwidth causes phase lag at the unity-gain frequency of the integrator for both type filters
  → Results in negative intg. Q & thus increases overall Q → results in peaking in the passband of interest
- For given filter requirements, opamp bandwidth requirements much less stringent for S.C. filters compared to cont. time filters
  → Lower power dissipation for S.C. filters (at low freq.s only since other nonidealities dominate at high freq.s)
- Finite opamp bandwidth causes down shifting of critical frequencies in both type filters
  – Since cont. time filters are usually tuned→ tuning accounts for frequency deviation
  – S.C. filters are untuned and thus frequency shift could cause problems particularly for narrow-band filters

Effect of Opamp Nonidealities on Switched-Capacitor Filter Performance

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion

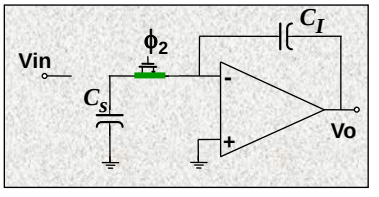
➡ – Finite slew rate of the opamp

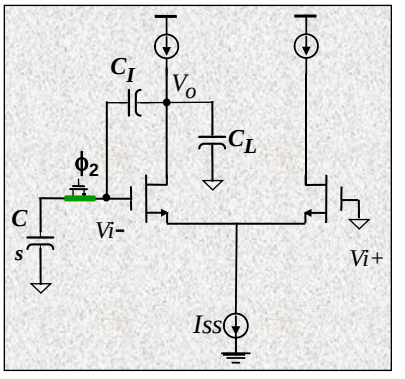
  – Non-linearity associated with opamp output/input characteristics

  – Capacitor non-linearity- usually insignificant, similar to cont. time filters

  – Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

What is Slewing?

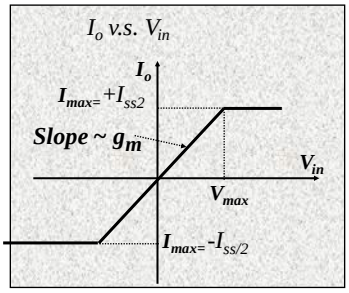


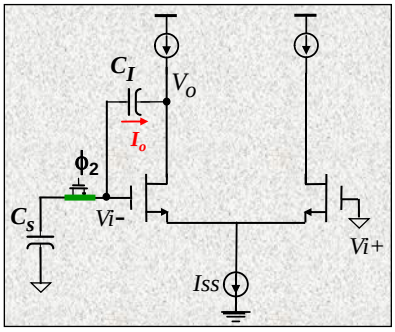


Assumption:

Integrator opamp is a simple class A transconductance type differential pair with fixed tail current, *Iss=const.*

What is Slewing?





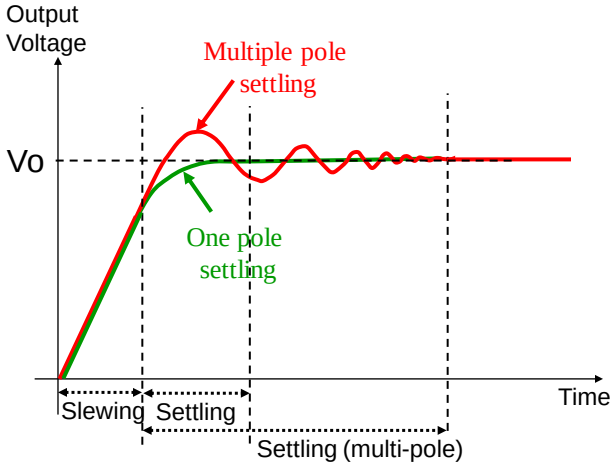
$|V_{Cs}| > V_{max}$ → Output current constant I_o=*Iss/2 or –Iss/2*

→ Constant current charging/discharging C_I: V_o ramps down/up → Slewing

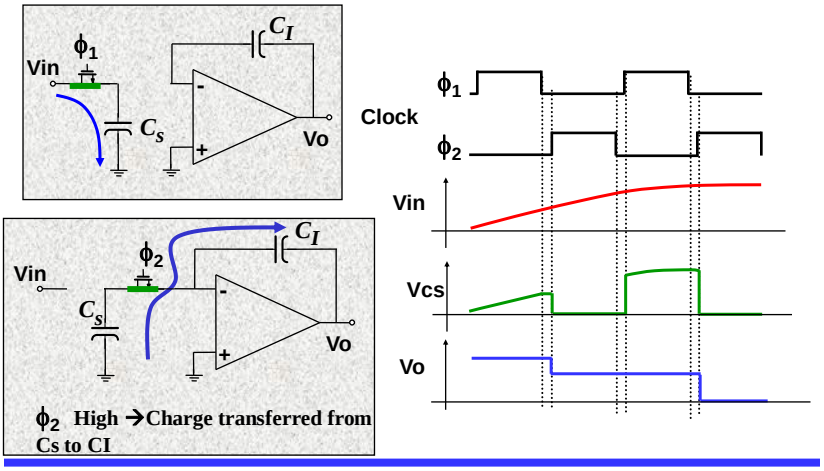
After V_{Cs} is discharged enough to have:

$|V_{Cs}|<V_{max}$ → $I_o=gm\ V_{Cs}$ → Output→ Exponential or over/under-shoot settling

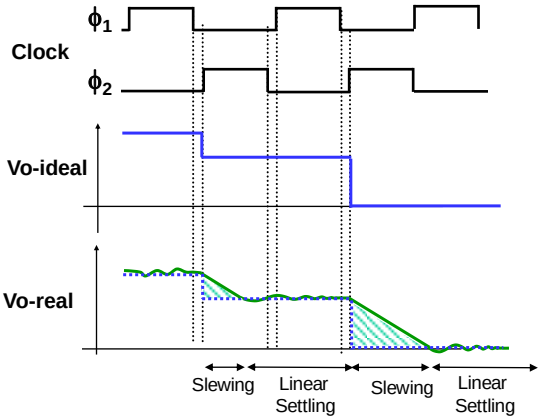
Distortion Induced by Opamp Finite Slew Rate



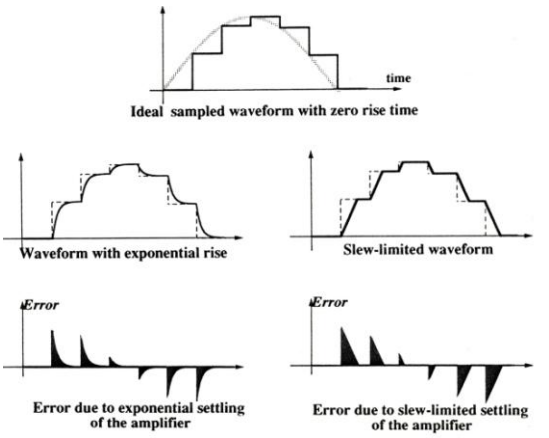
Ideal Switched-Capacitor Output Waveform



Slew Limited Switched-Capacitor Integrator Output Slewing & Settling



Distortion Induced by Finite Slew Rate of the Opamp



Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Distortion Induced by Opamp Finite Slew Rate

- Error due to exponential settling changes linearly with signal amplitude
- Error due to slew-limited settling changes non-linearly with signal amplitude (doubling signal amplitude X4 error)

  →For high-linearity need to have either high slew rate or non-slewing opamp

$$HD_k = \frac{V_o}{S_r T_s} \frac{8\left(sin\, \omega_o T_s/2\right)^2}{\pi k\left(k^2-4\right)}$$

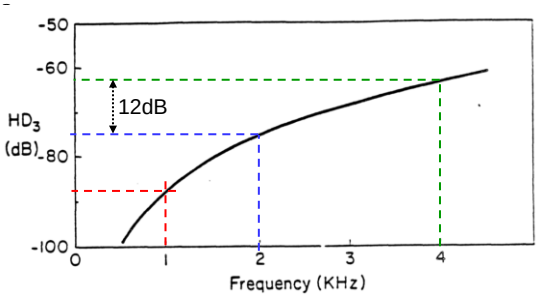
$$\rightarrow HD_3 = \frac{V_o}{S_r T_s} \frac{8\left(sin\, \omega_o T_s/2\right)^2}{15\pi} \quad for \quad f_o << f_s \rightarrow \quad HD_3 \approx \frac{8\pi V_o}{15 S_r} \frac{{f_o}^2}{f_s}$$

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

Example: Slew Related Harmonic Distortion

$$HD_3 = \frac{V_o}{S_r T_s}\,\frac{8\left(\sin \omega_o T_s/2\right)}{15\pi}$$

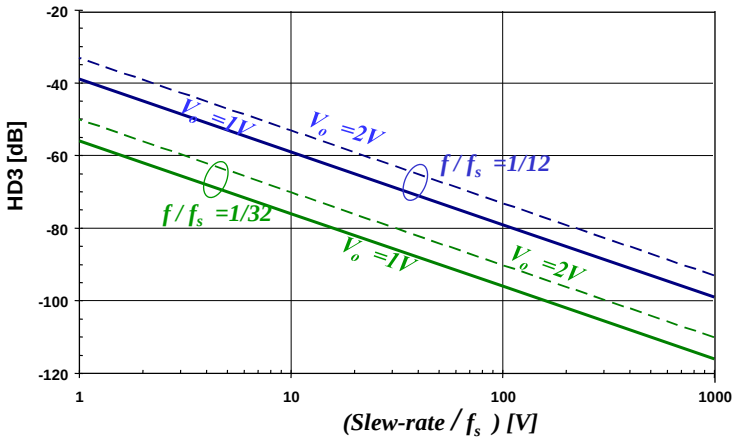
$$HD_3 \approx \frac{8\pi V_o}{15 S_r}\,\frac{{f_o}^2}{f_s}$$



Switched-capacitor filter with *4kHz* bandwidth, f_s=*128kHz*, S_r=*1V/μsec*, V_o=*3V*

Ref: K.L. Lee, "Low Distortion Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12).

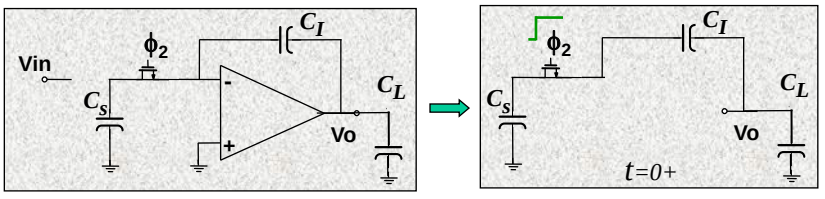
Distortion Induced by Opamp Finite Slew Rate Example



Distortion Induced by Finite Slew Rate of the Opamp

- Note that for a high order switched capacitor filter → only the last stage slewing will affect the output linearity (as long as the previous stages settle to the required accuracy)
  - → Can reduce slew limited non-linearities by using an amplifier with a higher slew rate *only* for the last stage
  - → Can reduce slew limited non-linearities by using class A/B amplifiers
    - Even though the output/input characteristics is non-linear as long as the DC open-loop gain is high, the significantly higher slew rate compared to class A amplifiers helps improve slew rate induced distortion in S.C. filters
- In cases where the output is sampled by another sampled data circuit (e.g. an ADC or a S/H) → no issue with the slewing of the output as long as the output settles to the required accuracy & is sampled at the right time

More Realistic Switched-Capacitor Circuit Slew Scenario



At the instant C_s connects to input of opamp (t=0+)

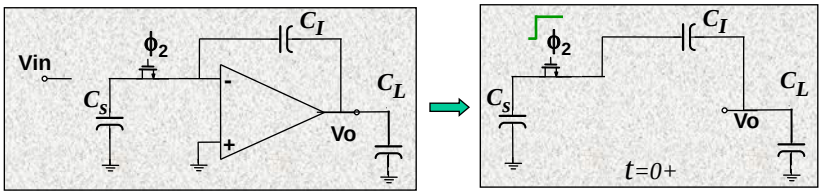
→ Opamp not yet active at t=0+ due to finite opamp bandwidth → delay

→ Feedforward path from input to output generates a voltage spike at the output with polarity opposite to final Vo step- spike magnitude function of C_I, C_L, C_s

→ Spike increases slewing period

→ Eventually, opamp becomes active - starts slewing followed by subsequent settling

Switched-Capacitor Circuit
Opamp not Active @ $t=0+$



$$Charge\ sharing: C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right) \quad where\ C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

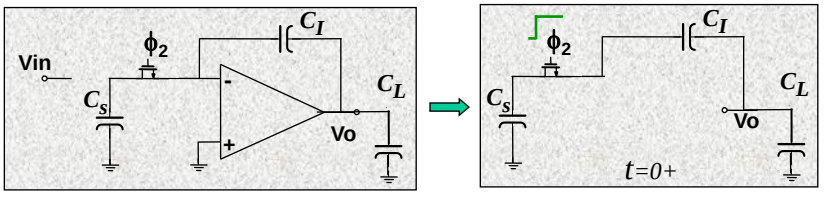
$$\Delta V_{out}^{t0+} = V_{Cs}^{t0+}\frac{C_I}{C_I + C_L} = V_{Cs}^{t0-}\frac{C_s}{C_s + C_{eq}} \times \frac{C_I}{C_I + C_L}$$

$$Assuming\ C_L << C_s << C_I \rightarrow C_{eq} \approx C_L \rightarrow C_s V_{Cs}^{t0-} \approx V_{Cs}^{t0+}\left(C_s + C_L\right) \rightarrow V_{Cs}^{t0-} \approx V_{Cs}^{t0+}$$

$$\rightarrow \Delta V_{out}^{t0+} \approx V_{Cs}^{t0-}\frac{C_s}{C_s + C_L} \times \frac{C_I}{C_I + C_L} \approx V_{Cs}^{t0-}$$

$$Note\ that\ \ \Delta V_{out}^{final} \approx -\frac{C_s}{C_I} V_{Cs}^{t0+} \approx -\frac{C_s}{C_I} V_{Cs}^{t0-}$$

More Realistic Switched-Capacitor Circuit Slew Scenario



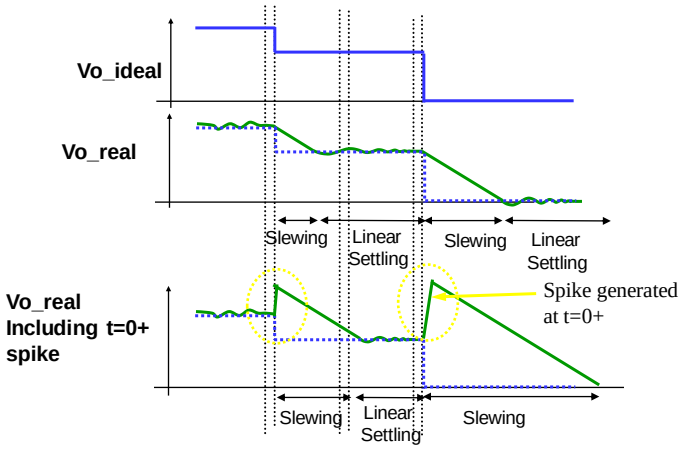
Notice that if C_L is large → some of the charge stored on Cs is lost prior to opamp becoming effective → operation looses accuracy

$$Charge\ sharing: C_s V_{Cs}^{t0-} = V_{Cs}^{t0+}\left(C_s + C_{eq}\right) \quad where\ C_{eq} = \frac{C_I C_L}{C_I + C_L}$$

$$V_{Cs}^{t0+} = V_{Cs}^{t0-}\frac{C_s}{C_s + C_{eq}} = V_{Cs}^{t0-}\frac{C_s}{C_s + \dfrac{C_I C_L}{C_I + C_L}}$$

→ Partly responsible for S.C. filters only good for low-frequency applications

More Realistic S.C. Slew Scenario



Ref: R. Castello, "Low Voltage, Low Power Switched-Capacitor Signal Processing Techniques," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, Aug. '84 (ERL Memorandum No. UCB/ERL M84/67).

Effect of Opamp Nonidealities on Switched Capacitor Filter Behavior

- Opamp finite gain
- Opamp finite bandwidth
- Sources of distortion
  - Finite slew rate of the opamp
  - Non-linearity associated with opamp output/input characteristics
  - Capacitor non-linearity- usually insignificant, similar to cont. time filters
  - Charge injection & clock feedthrough (will be covered in the oversampling data converter section)

Sources of Noise in Switched-Capacitor Filters

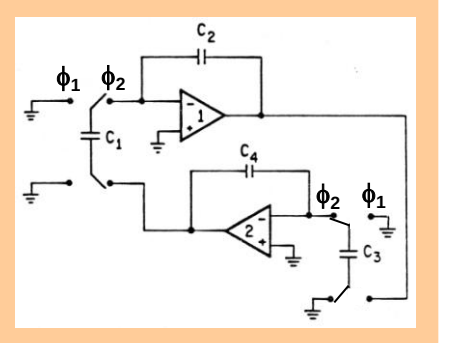
- Opamp Noise
  - Thermal noise
  - 1/f (flicker) noise
- Thermal noise associated with the switching process (kT/C)
  - Same as continuous-time filters
- Precaution regarding aliasing of noise required

Extending the Maximum Achievable Critical Frequency of Switched-Capacitor Filters

Consider a switched-capacitor resonator:

Regular sampling:
Each opamp is busy settling only during one of the two clock phases

→ Idle during the other clock phase

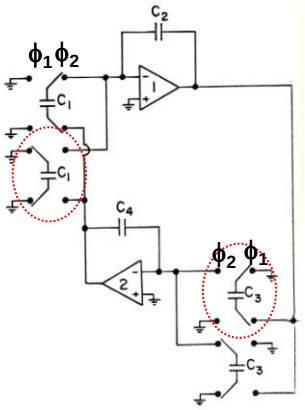


Note: During ϕ_1 both opamps are idle

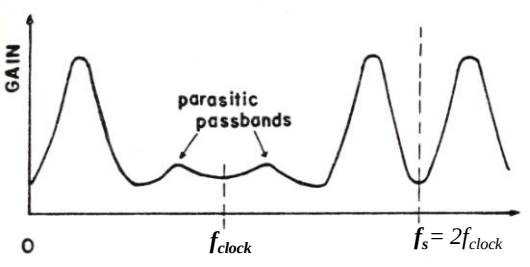
Switched-Capacitor Resonator Using Double-Sampling

Double-sampling:

- 2nd set of switches & sampling caps added to all integrators
- While one set of switches/caps sampling the other set transfers charge into the intg. cap
- Opamps busy during both clock phases
- **Effective sampling freq. twice the clock freq. while opamp bandwidth requirement remains the same**



Double-Sampling Issues

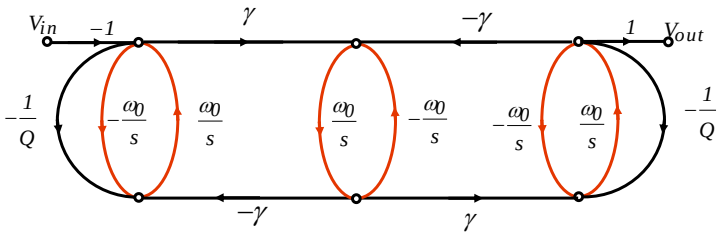


Issues to be aware of:
- Jitter in the clock
- Unequal clock phases
-Mismatch in sampling caps.

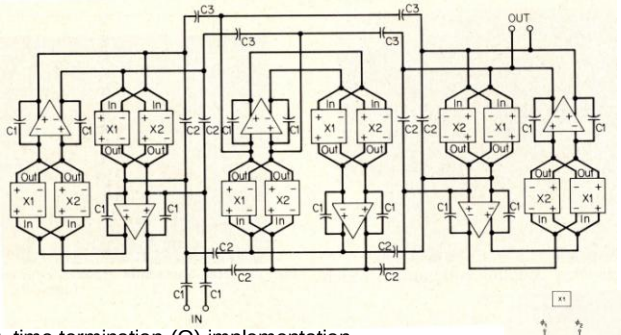
→ Results in parasitic passbands

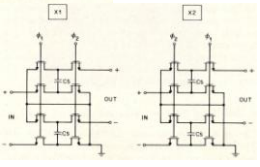
Ref: Tat C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31).

Sixth Order Bandpass Filter Signal Flowgraph



Double-Sampled Fully Differential 6th Order S.C. All-Pole Bandpass Filter

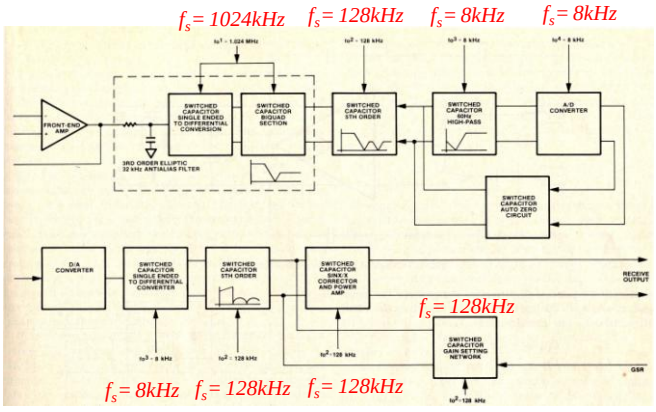




- Cont. time termination (Q) implementation
- Folded-Cascode opamp with f_u = *100MHz* used
- Center freq. *3.1MHz* (Measured error *>1%*), filter *Q=55*
- Clock freq. *12.83MHz* → effective oversampling ratio *8.27*
- Measured dynamic range *46dB* (*IM3=1%)*

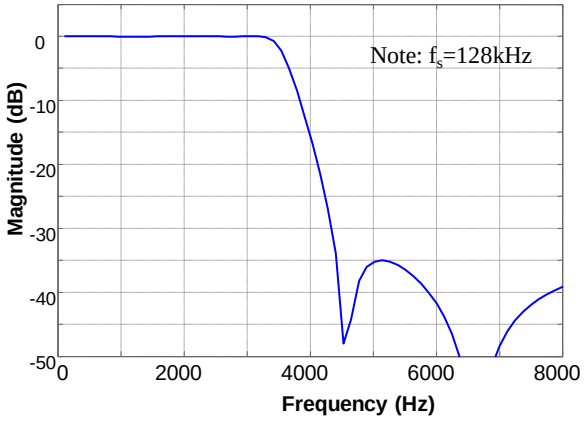
Ref: B.S. Song, P.R. Gray "Switched-Capacitor High-Q Bandpass Filters for IF Applications," *IEEE Journal of Solid State Circuits*, Vol. 21, No. 6, pp. 924-933, Dec. 1986.

Switched-Capacitor Filter Application
Example: Voice-Band CODEC (Coder-Decoder) Chip

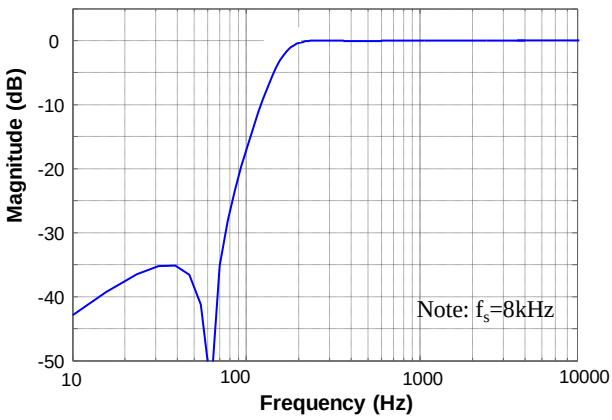


Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits*, Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

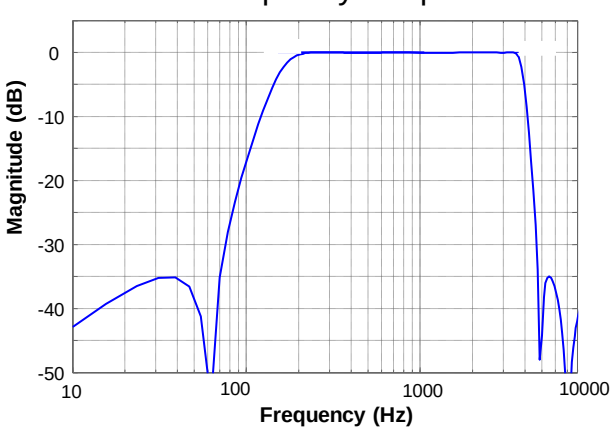
CODEC Transmit Path
Lowpass Filter Frequency Response



CODEC Transmit Path
Highpass Filter



CODEC Transmit Path Filter
Overall Frequency Response



Low Q bandpass (Q<1) filter shape→ Implemented with lowpass followed by highpass

CODEC Transmit Path Clocking Scheme

First filter (1st order RC type) performs anti-aliasing for the next S.C. biquad

The first 2 stage filters form 3rd order elliptic with corner frequency @ 32kHz → Anti-aliasing for the next S.C. lowpass filter with 3.4kHz corner freq.

The stages prior to the high-pass perform anti-aliasing for high-pass

Notice gradual lowering of clock frequency → Ease of anti-aliasing

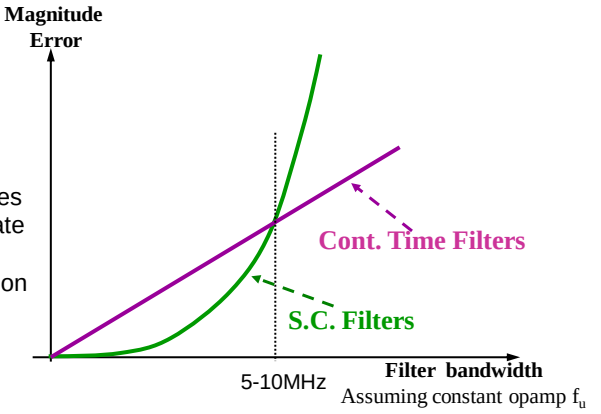
SC Filter Summary

- ✓ Pole and zero frequencies proportional to
  - Sampling frequency f_s
  - Capacitor ratios
  - ➢ High accuracy and stability in response
  - ➢ Long time constants realizable without large R, C
- ✓ Compatible with transconductance amplifiers
  - Reduced circuit complexity, power dissipation
- ✓ Amplifier bandwidth requirements less stringent compared to CT filters (low frequencies only)
- ☹ Issue: Sampled-data filters → require anti-aliasing prefiltering

Switched-Capacitor Filters versus Continuous-Time Filter Limitations

Considering overall effects:

- Opamp finite unity-gain-bandwidth
- Opamp settling issues
- Opamp finite slew rate
- Clock feedthru & switch charge injection
- Switch+ sampling cap. finite time-constant



→ Limited switched-capacitor filter performance frequency range

Summary
Filter Performance versus Filter Topology

	Max. Usable Bandwidth	SNDR	Freq. Tolerance w/o Tuning	Freq. Tolerance + Tuning
Opamp-RC	~10MHz	60-90dB	+-30-50%	1-5%
Opamp-MOSFET-C	~ 5MHz	40-60dB	+-30-50%	1-5%
Opamp-MOSFET-RC	~ 5MHz	50-90dB	+-30-50%	1-5%
Gm-C	~ 100MHz	40-70dB	+-40-60%	1-5%
Switched Capacitor	~ 10MHz	40-90dB	<1%	_

Frequency Warping

- Frequency response
  - Continuous time (s-plane): imaginary axis
  - Sampled time (z-plane): unit circle
- Continuous to sampled time transformation
  - Should map imaginary axis onto unit circle
  - How do S.C. integrators map frequencies?

$$H_{\text{S.C.}}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}$$

$$= -\frac{C_s}{C_{int}} \quad \frac{1}{2j \sin \pi f T}$$

CT – SC Integrator Comparison

CT Integrator

$$H_{\text{RC}}(s) = -\frac{1}{s\tau}$$

$$= -\frac{1}{2\pi j f_{RC} \tau}$$

SC Integrator

$$H_{\text{SC}}(z) = \frac{C_s}{C_{int}} \frac{z^{-1/2}}{1 - z^{-1}}$$

$$= -\frac{C_s}{C_{int}} \frac{1}{2j \sin \pi f_{SC} T_s}$$

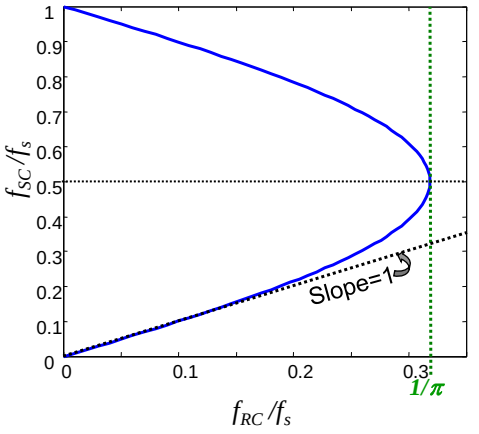
Identical time constants:

$$\tau = RC = \frac{C_{int}}{f_s C_s}$$

Set: $H_{RC}(f_{RC}) = H_{SC}(f_{SC})$ →

$$f_{RC} = \frac{f_s}{\pi} \sin\left(\pi \frac{f_{SC}}{f_s}\right)$$

LDI Integration



$$f_{RC} = \frac{f_s}{\pi}\sin\left(\pi\frac{f_{SC}}{f_s}\right)$$

- "RC" frequencies up to f_s/π map to physical (real) "SC" frequencies
- Frequencies above f_s/π do not map to physical frequencies
- Mapping is symmetric about $f_s/2$ (aliasing)
- "Accurate" only for $f_{RC} << f_s$

Material Covered in EE247
Where are We?

- ✓ Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Pipeline ADCs,….
    - Oversampled converters
    - Self-calibration techniques
- Systems utilizing analog/digital interfaces