

# EE247

## Lecture 15

- D/A converters
  - Practical aspects of current-switched DACs (continued)
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations
  - Self calibration techniques
    - Current copiers
    - Dynamic element matching
  - DAC reconstruction filter
- A/D converter introduction

## Summary Last Lecture

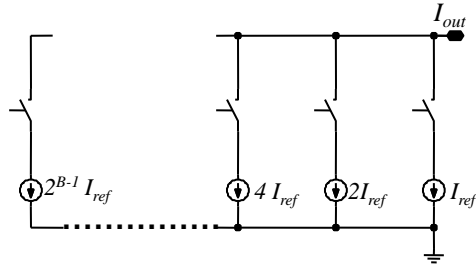
- D/A converter architectures:
- Resistor string DAC
  - Serial charge redistribution DAC
  - Parallel charge scaling DAC
  - Combination of resistor string (MSB) & binary weighted charge scaling (LSB)
  - Current source DAC
    - Unit element
    - Binary weighted
- Static performance
- Component matching-systematic & random errors
    - Component random variations → Gaussian pdf
    - INL for both unit-element & binary weight DAC:  $\sigma_{INL} = \sigma_e \times 2^{B/2-1}$
    - DNL for unit-element:  $\sigma_{DNL} = \sigma_e$
    - DNL for binary-weighted  $\sigma_{DNL} = \sigma_e \times 2^{B/2}$

## INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:

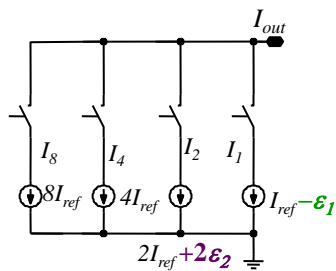
$$0 \text{ to } 1 \rightarrow \sigma_{DNL}^2 = \sigma_{(dI/I)}^2$$

$$1 \text{ to } 2 \rightarrow \sigma_{DNL}^2 = 3\sigma_{(dI/I)}^2$$

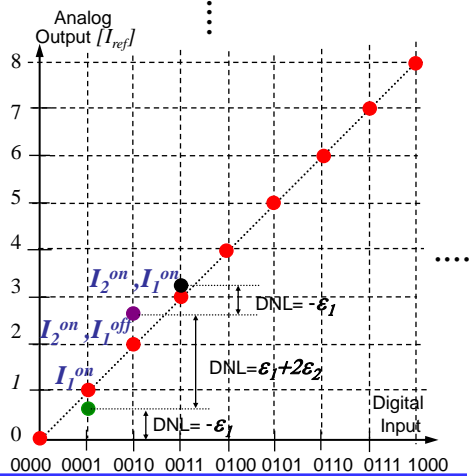


- Consider MSB transition:  
0111 ...  $\rightarrow$  1000 ...

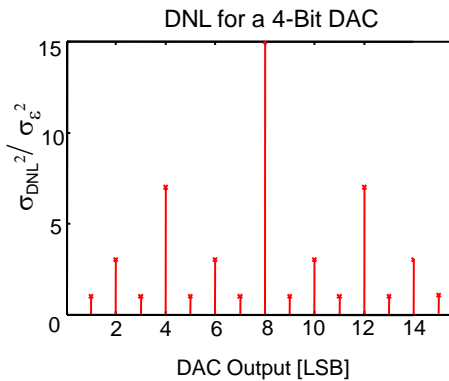
## DAC DNL Example: 4bit DAC



- DNL depends on transition
    - Example:
- $$0 \text{ to } 1 \rightarrow \sigma_{DNL}^2 = \sigma_{(dI_{ref}/I_{ref})}^2$$
- $$1 \text{ to } 2 \rightarrow \sigma_{DNL}^2 = 3\sigma_{(dI_{ref}/I_{ref})}^2$$



# Binary Weighted DAC DNL



- Worst-case transition occurs at mid-scale:

$$\sigma_{DNL}^2 = \underbrace{(2^{B-1}-1)\sigma_{\epsilon}^2}_{0111\dots} + \underbrace{(2^{B-1})\sigma_{\epsilon}^2}_{1000\dots}$$

$$\cong 2^B \sigma_{\epsilon}^2$$

$$\sigma_{DNL_{max}} = 2^{B/2} \sigma_{\epsilon}$$

$$\sigma_{INL_{max}} \cong \frac{1}{2} \sqrt{2^B - 1} \sigma_{\epsilon} \cong \frac{1}{2} \sigma_{DNL_{max}}$$

- Example:

$$B = 12, \sigma_{\epsilon} = 1\%$$

$$\rightarrow \sigma_{DNL} = 0.64 \text{ LSB}$$

$$\rightarrow \sigma_{INL} = 0.32 \text{ LSB}$$

## Unit Element versus Binary Weighted DAC Example: B=10

### Unit Element DAC

$$\sigma_{DNL} = \sigma_{\epsilon}$$

$$\sigma_{INL} \cong 2^{B/2-1} \sigma_{\epsilon} = 16 \sigma_{\epsilon}$$

Number of switched elements:

$$S = 2^B = 1024$$

*Requires B to (2<sup>B</sup>-1) decoder to address switches*

### Binary Weighted DAC

$$\sigma_{DNL} \cong 2^{B/2} \sigma_{\epsilon} = 32 \sigma_{\epsilon}$$

$$\sigma_{INL} \cong 2^{B/2-1} \sigma_{\epsilon} = 16 \sigma_{\epsilon}$$

$$S = B = 10$$

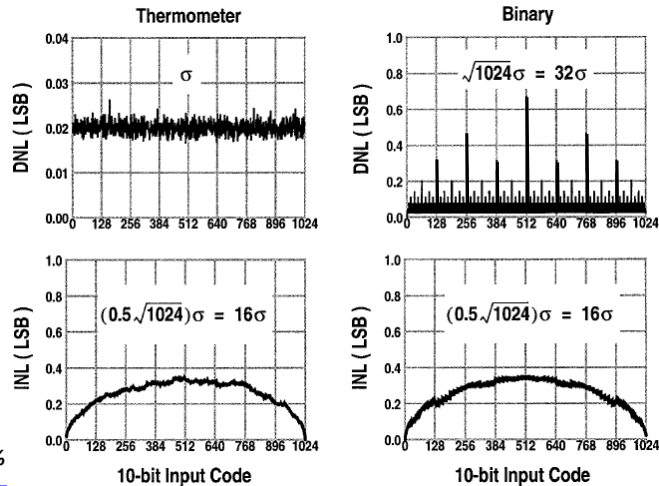
*B-bit digital input can be used directly*

*Significant difference in performance and complexity!*

## 10Bit DAC DNL/INL Comparison Plots: RMS for 100 Simulation Runs

Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm<sup>2</sup>," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948 - 1958, December 1998.

Note:  $\sigma_{\epsilon} = 2\%$



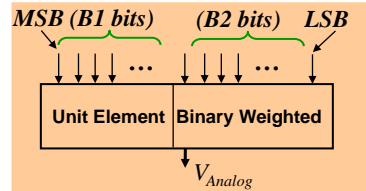
## DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. *IEEE Transactions on Circuits and Systems*, vol.CAS-29, (no.6), June 1982. p.383-9.

## Segmented DAC Combination of Unit-Element & Binary-Weighted

- Objective:  
Compromise between unit-element and binary-weighted DAC



- Approach:  
 $B_1$  MSB bits  $\rightarrow$  unit elements  
 $B_2$  LSB bits  $\rightarrow$  binary weighted
- INL: unaffected same as either architecture
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on  $\rightarrow$  Same as binary weighted DAC with  $(B_2+1)$  # of bits
- Number of switched elements:  $(2^{B_1-1}) + B_2$

## Comparison

Example:

$$B = 12, \quad B_1 = 5, \quad B_2 = 7$$

$$\underbrace{B_1 = 6}_{\text{MSB}}, \quad \underbrace{B_2 = 6}_{\text{LSB}}$$

$$\sigma_{DNL} \cong 2^{(B_2+1)/2} \sigma_\epsilon = 2\sigma_{INL}$$

$$\sigma_{INL} \cong 2^{B_2/2-1} \sigma_\epsilon$$

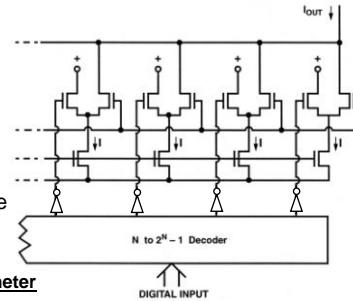
$$S = 2^{B_1} - 1 + B_2$$

Assuming:  $\sigma_\epsilon = 1\%$

DAC Architecture ( $B_1+B_2$ )	$\sigma_{INL[LSB]}$	$\sigma_{DNL[LSB]}$	# of switched elements
Unit element (12+0)	0.32	0.01	4095
Segmented (6+6)	0.32	0.113	63+6=69
Segmented (5+7)	0.32	0.16	31+7=38
Binary weighted(0+12)	0.32	0.64	12

## Practical Aspects Current-Switched DACs

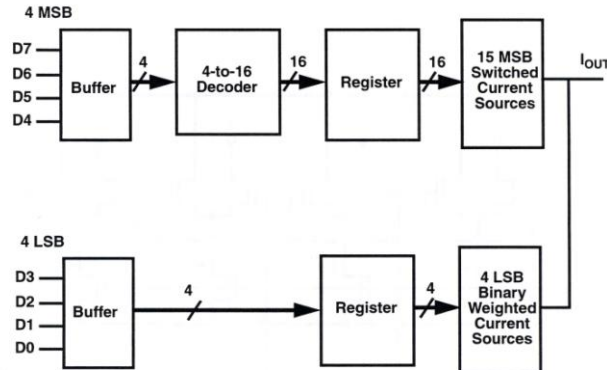
- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on → switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder



	<u>Binary</u>	<u>Thermometer</u>
	000	0000000
	001	0000001
→ B to (2 <sup>B</sup> -1) decoder	010	0000011
	011	0000111
	100	0001111
	101	0011111
	110	0111111
	111	1111111

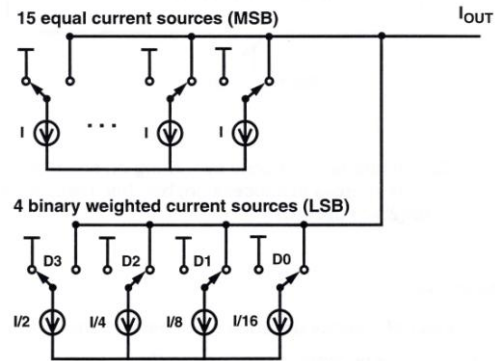
## Segmented Current-Switched DAC Example: 8bit → 4MSB+4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register



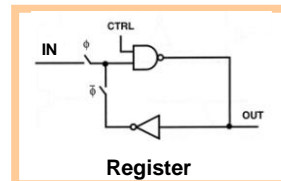
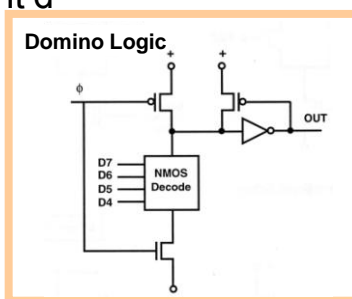
## Segmented Current-Switched DAC Cont'd

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register



## Segmented Current-Switched DAC Cont'd

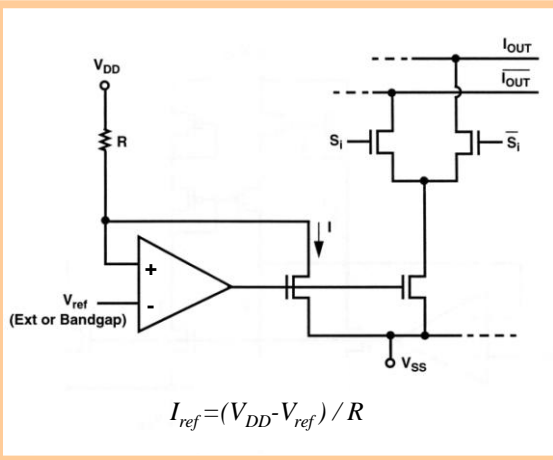
- MSB Decoder
  - Domino logic
  - Example:  $D_4, D_5, D_6, D_7 = 1$   $OUT = 1$
- Register
  - Latched NAND gate:
  - $CTRL = 1$   $OUT = INB$



## Segmented Current-Switched DAC Reference Current Considerations

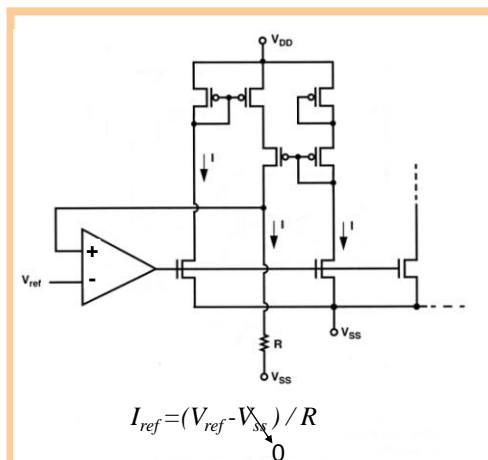
- $I_{ref}$  is referenced to  $V_{DD}$

→ Problem:  
Reference current varies with supply voltage



## Segmented Current-Switched DAC Reference Current Considerations

- $I_{ref}$  is referenced to  $V_{SS} \rightarrow GND$



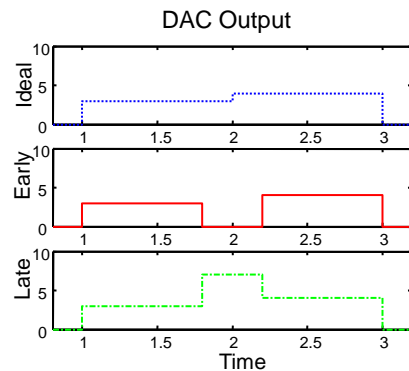


## DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling
- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches & switch charge injection
- Timing error related glitches
  - Control signal timing skew

## Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011  $\rightarrow$  100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early



## Glitch Energy

- Glitch energy (worst case) proportional to:  $dt \times 2^{B-1}$
- $dt \rightarrow$  error in timing &  $2^{B-1}$  associated with half of the switches changing state
- LSB energy proportional to:  $T=1/f_s$
- Need  $dt \times 2^{B-1} \ll T$  or  $dt \ll 2^{-B+1} T$
- Examples:

$f_s$ [MHz]	B	$dt$ [ps]
1	12	$\ll 488$
20	16	$\ll 1.5$
1000	12	$\ll 0.5$

**$\rightarrow$  Timing accuracy for logic circuitry associated with data converters much more critical compared to digital circuitry e.g. DSP**

## DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry

# DAC Implementation Examples

- Untrimmed segmented
  - T. Miki et al, "An 80-MHz 8-bit CMOS D/A Converter," JSSC December 1986, pp. 983
  - A. Van den Bosch et al, "A 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," JSSC March 2001, pp. 315
- Current copiers:
  - D. W. J. Groeneveld et al, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," JSSC December 1989, pp. 1517
- Dynamic element matching:
  - R. J. van de Plassche, "Dynamic Element Matching for High-Accuracy Monolithic D/A Converters," JSSC December 1976, pp. 795

## An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI,  
YOICHI AKASAKA, AND YASUTAKA HORIBA

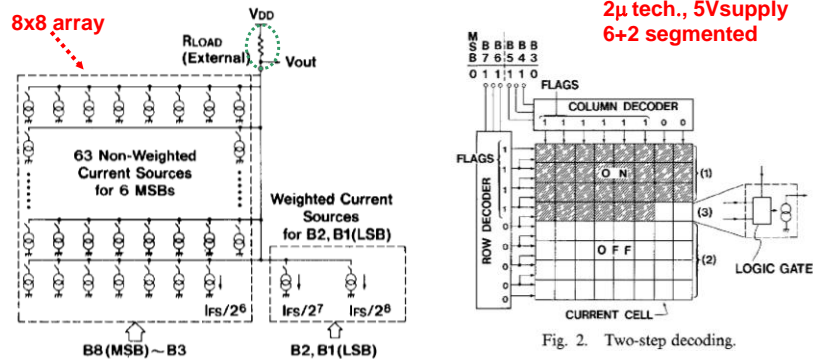


Fig. 1. Basic architecture of the DAC.

Fig. 2. Two-step decoding.

- Two sources of systematic error:
- Finite current source output resistance
  - Voltage drop due to finite ground bus resistance

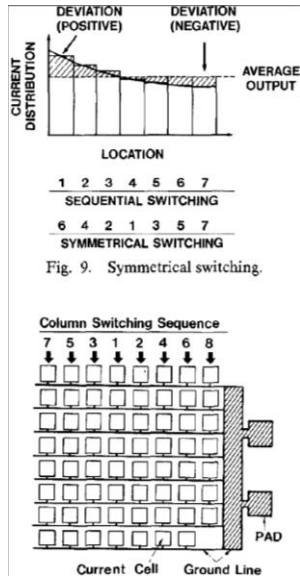
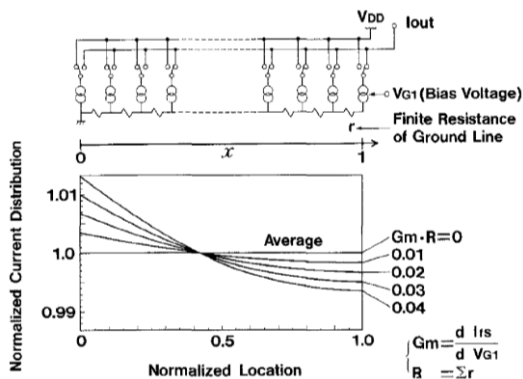


Fig. 9. Symmetrical switching.

## Current-Switched DACs in CMOS

Assumptions:

$RxI$  small compared to transistor gate-overdrive

To simplify analysis: Initially, all device currents assumed to be equal to  $I$

$$V_{GS_{M2}} = V_{GS_{M1}} - 4RI$$

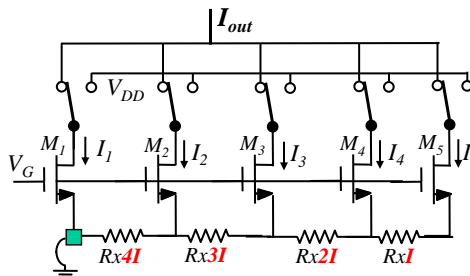
$$V_{GS_{M3}} = V_{GS_{M1}} - 7RI$$

$$V_{GS_{M4}} = V_{GS_{M1}} - 9RI$$

$$V_{GS_{M5}} = V_{GS_{M1}} - 10RI$$

$$I_2 = k(V_{GS_{M2}} - V_{th})^2$$

$$I_2 = I_1 \left( 1 - \frac{4RI}{V_{GS_{M1}} - V_{th}} \right)^2$$



Example: 5 unit element current sources

## Current-Switched DACs in CMOS

$$I_2 = k(V_{GS_{M_2}} - V_{th})^2 = I_1 \left( 1 - \frac{4RI}{V_{GS_{M_1}} - V_{th}} \right)^2$$

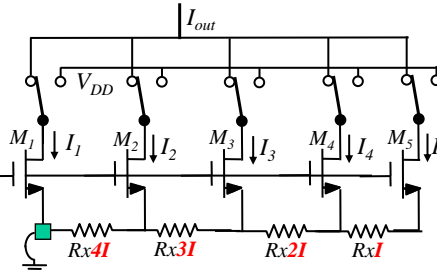
$$g_{m_{M_1}} = \frac{2I_1}{V_{GS_{M_1}} - V_{th}}$$

$$\rightarrow I_2 = I_1 \left( 1 - \frac{4Rg_{m_{M_1}}}{2} \right)^2 \approx I_1 (1 - 4Rg_{m_{M_1}})$$

$$\rightarrow I_3 = I_1 \left( 1 - \frac{7Rg_{m_{M_1}}}{2} \right)^2 \approx I_1 (1 - 7Rg_{m_{M_1}})$$

$$\rightarrow I_4 = I_1 \left( 1 - \frac{9Rg_{m_{M_1}}}{2} \right)^2 \approx I_1 (1 - 9Rg_{m_{M_1}})$$

$$\rightarrow I_5 = I_1 \left( 1 - \frac{10Rg_{m_{M_1}}}{2} \right)^2 \approx I_1 (1 - 10Rg_{m_{M_1}})$$

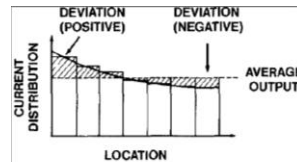
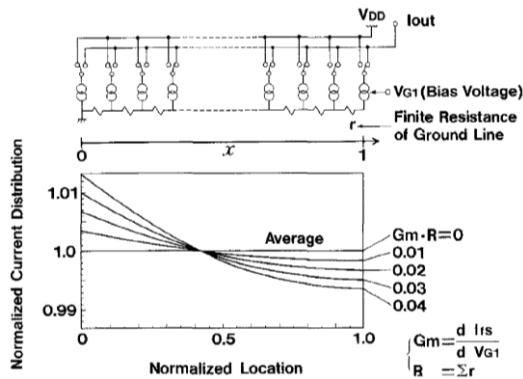


Example: 5 unit element current sources

→ Desirable to have  $g_m$  small

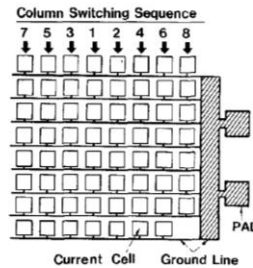
### Two sources of systematic error:

- Finite current source output resistance
- Voltage drop due to finite ground bus resistance

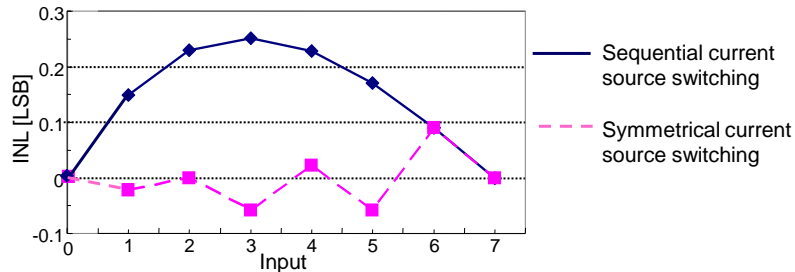


SEQUENTIAL SWITCHING  
6 4 2 1 3 5 7

Fig. 9. Symmetrical switching.



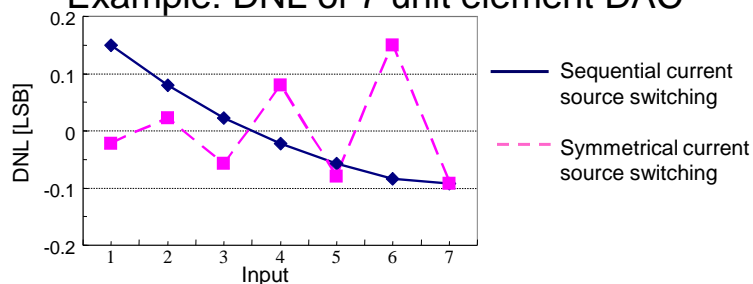
## Current-Switched DACs in CMOS Example: INL of 3-Bit unit element DAC



- Example: 7 unit element current source DAC- assume  $g_m R = 1/100$
- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)  
 $\rightarrow INL = +0.25LSB$
  - If switching of current sources symmetrical (4-3-5-2-6-1-7)  
 $\rightarrow INL = +0.09, -0.058LSB \rightarrow INL$  reduced by a factor of 2.6

This technique is also effective in compensating for systematic errors associated with process gradients.

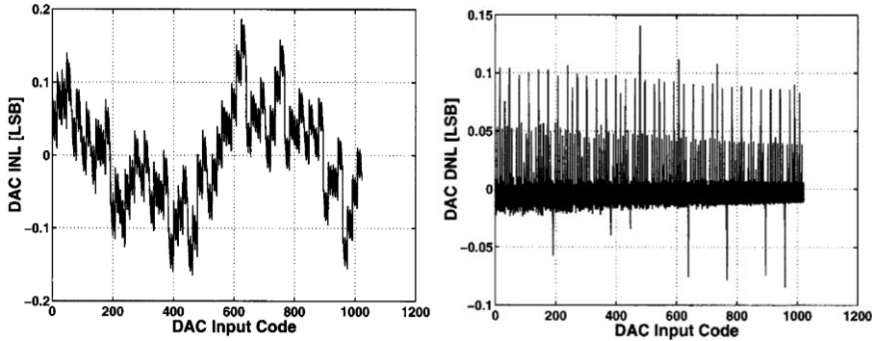
## Current-Switched DACs in CMOS Example: DNL of 7 unit element DAC



- Example: 7 unit element current source DAC- assume  $g_m R = 1/100$
- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)  
 $\rightarrow DNL_{max} = +0.15LSB$
  - If switching of current sources symmetrical (4-3-5-2-6-1-7)  
 $\rightarrow DNL_{max} = +0.15LSB \rightarrow DNL_{max}$  unchanged

# A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*,  
 Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

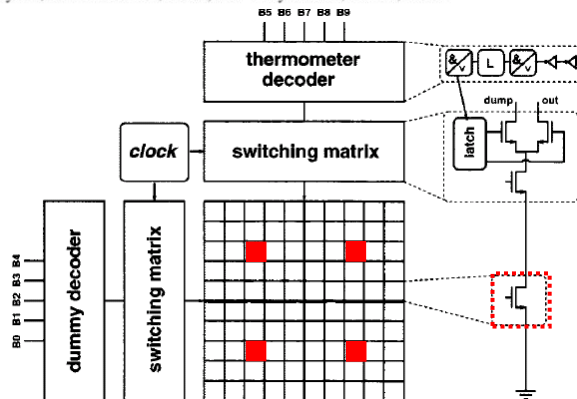


**More recent published DAC using symmetrical switching built in 0.35μ/3V analog/1.9V digital, area x10 smaller compared to previous example**

# A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

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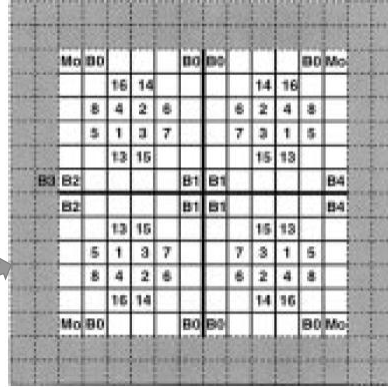
- Layout of Current sources -each current source made of 4 devices in parallel each located in one of the 4 quadrants
- Thermometer decoder used to convert incoming binary digital control for the 5 MSB bits
- Dummy decoder used on the LSB side to match the latency due to the MSB decoder



# A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

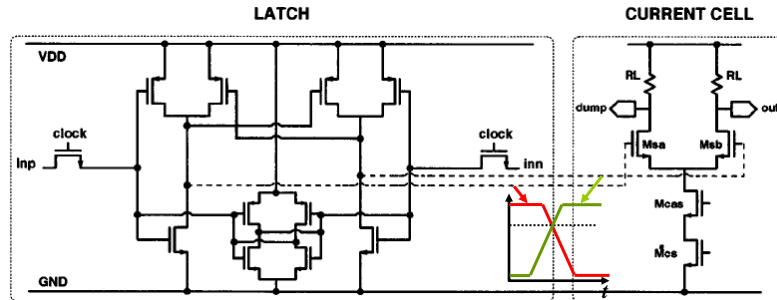
Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

- Current source layout
  - MSB current sources layout in the mid sections of the four quad
  - LSB current sources mostly in the periphery
  - Two rows of dummy current sources added @ the periphery to create identical environment for devices in the center versus the ones on the outer sections



# A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*

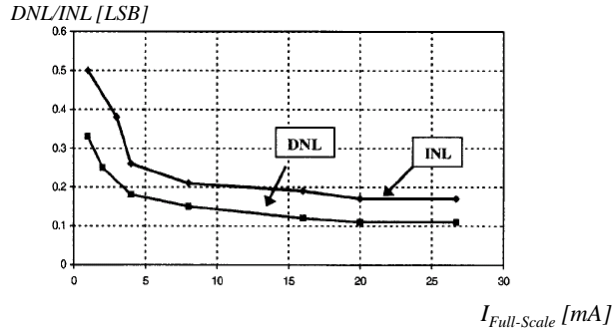


- Note that each current cell has its clocked latch and clock signal laid out to be close to its switch to ensure simultaneous switching of current sources
- Special attention paid to the final latch to have the cross point of the complementary switch control signal such that the two switches are not both turned off during transition



# A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*



- Measured DNL/INL with current associated with the current cells as variable

# A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

Called:  
Current Copier

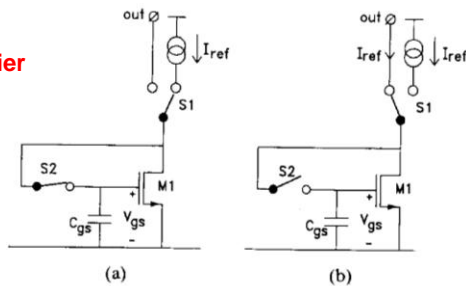
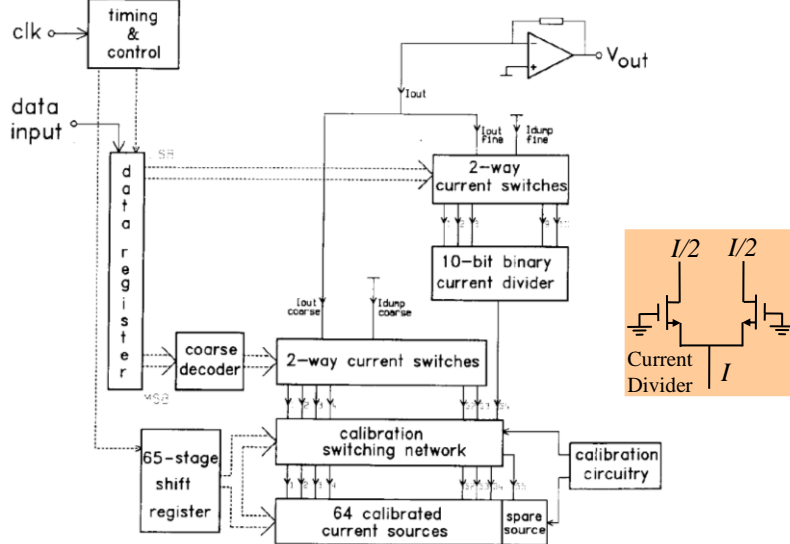


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.

**16bit DAC (6+10) - MSB DAC uses current copier technique**



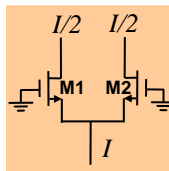
**Current Divider Inaccuracy due to Device Mismatch**

M1 & M2 mismatch results in the two output currents not being exactly equal:

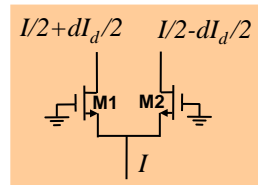
$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

$$\frac{dI_d}{I_d} = \frac{2}{V_{GS} - V_{th}} \times \left[ \left( \frac{dW/L}{W/L} \right) + dV_{th} \right]$$



Ideal Current Divider



Real Current Divider  
M1 & M2 mismatched

→ Problem: Device mismatch could severely limit DAC accuracy  
→ Use of dynamic element matching (next few pages)

## Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

- Idea is:
  - Even though the two outputs of the diff pair divider may not be exactly equal (due to device mismatch)
  - The sum of the two currents stays constant
    - By using switching tie both outputs to sum of the two

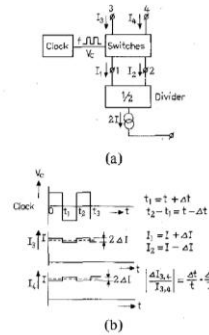
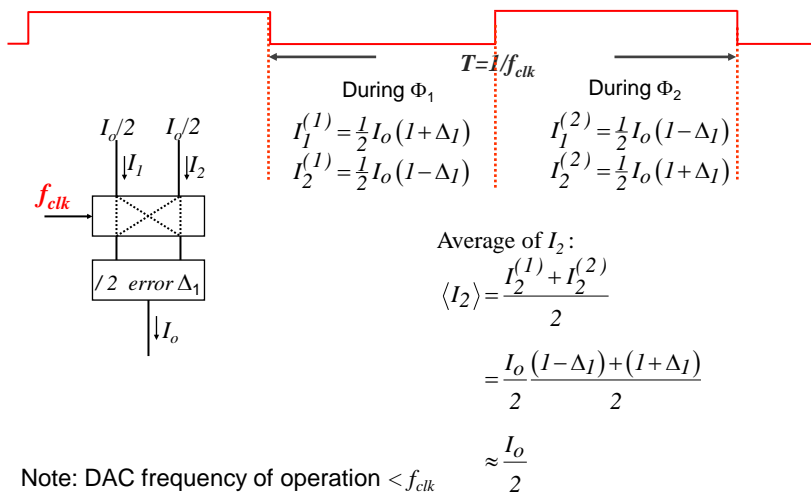
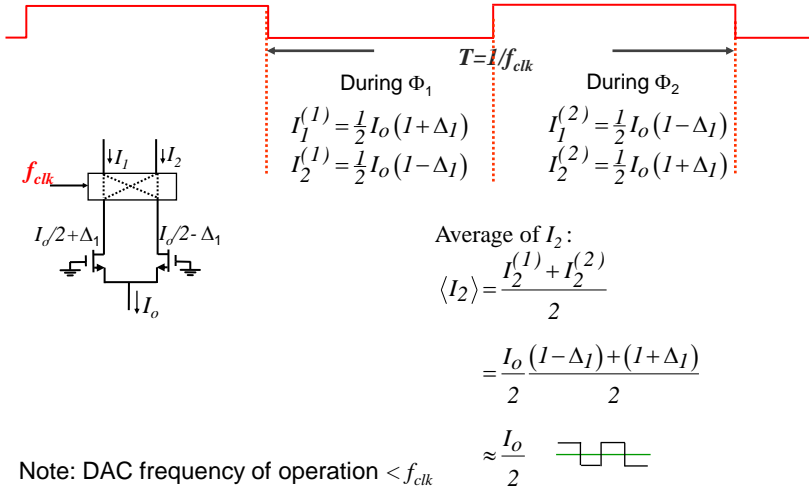


Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

## Dynamic Element Matching

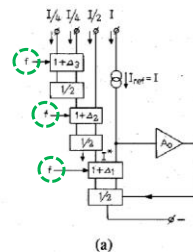
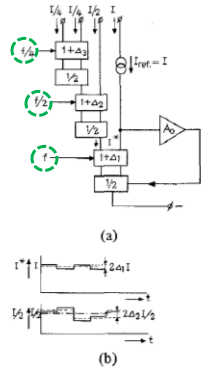


# Dynamic Element Matching



Note: DAC frequency of operation  $< f_{clk}$

Note:  
 For optimum current division accuracy  $\rightarrow$  clock frequency is divided by two for each finer division  
 Problem: DAC frequency of operation drastically reduced



$$I_o = I_{ref} \left[ \frac{1}{4} (1 + \Delta_1) + \frac{1}{2} (1 + \Delta_2) + (1 + \Delta_3) \right]$$

$$I_o = \frac{I_{ref}}{4} \left[ (1 + \Delta_1 + \Delta_2 + \Delta_3) + \Delta_1 + \Delta_2 + \Delta_3 \right]$$

$$I_o = \frac{I_{ref}}{4} \left[ (1 + \Delta_1 + \Delta_2 + \Delta_3) + \Delta_1 + \Delta_2 + \Delta_3 \right]$$

(b)

(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.

Note: What if the same clock frequency is used?

## Dynamic Element Matching

During  $\Phi_1$

$$I_1^{(1)} = \frac{1}{2} I_o (1 + \Delta_1)$$

$$I_2^{(1)} = \frac{1}{2} I_o (1 - \Delta_1)$$

$$I_3^{(1)} = \frac{1}{2} I_1^{(1)} (1 + \Delta_2)$$

$$= \frac{1}{4} I_o (1 + \Delta_1) (1 + \Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$

$$= \frac{I_o}{4} \frac{(1 + \Delta_1)(1 + \Delta_2) + (1 - \Delta_1)(1 - \Delta_2)}{2}$$

$$= \frac{I_o}{4} (1 + \Delta_1 \Delta_2)$$

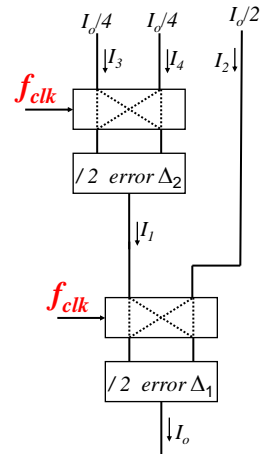
During  $\Phi_2$

$$I_1^{(2)} = \frac{1}{2} I_o (1 - \Delta_1)$$

$$I_2^{(2)} = \frac{1}{2} I_o (1 + \Delta_1)$$

$$I_3^{(2)} = \frac{1}{2} I_1^{(2)} (1 - \Delta_2)$$

$$= \frac{1}{4} I_o (1 - \Delta_1) (1 - \Delta_2)$$



E.g.  $\Delta_1 = \Delta_2 = 1\% \rightarrow$  matching error is  $(1\%)^2 = 0.01\%$

## Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

- Bipolar 12-bit DAC using dynamic element matching built in 1976
- Element matching clock frequency 100kHz
- INL < 0.25LSB!

### 12-BIT D/A TEST CHIP

D/A NETWORK DATA	
Resolution :	12 bit
Accuracy :	$\leq 1/4$ L.S.B. or $5 \cdot 10^{-5}$ (linearity)
Output current :	2 mA
Temp. Coeff. of output current :	5 ppm/ $^{\circ}$ C
Voltage Coeff. of output current :	1 ppm/V
Chip size :	2.5 x 2.5 mm
Max. clock freq. for dynamic matching :	100 kHz
Power supply :	-15V

## ISSCC 2004 / SESSION 20 / DIGITAL-TO-ANALOG CONVERTERS / 20.1

### 20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

Bernd Schaffner and Richard Adams

Example: State-of-the-Art current steering DAC

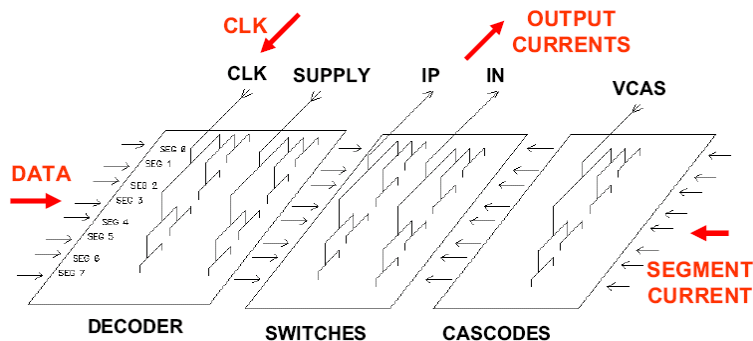
Segmented:  
6bit unit-element  
8bit binary

Max Sample Frequency	1.4	GSPS
Resolution	14	Bit
DNL	+/- 0.8	LSB
INL	+/- 2.1	LSB
SFDR @ 1.0 GSPS	> 60	dB
IMD @ 1.0 GSPS	> 64	dBc
NSD @ $f_{out} = 400\text{MHz}$	-155	dBm/Hz
Power ( Core ) @ 1.4GSPS	200	mW
Power( Total ) @ 1.4GSPS	400	mW
Area ( Core )	0.8	mm <sup>2</sup>
Area ( Chip )	6.25	mm <sup>2</sup>

## ISSCC 2004 / SESSION 20 / DIGITAL-TO-ANALOG CONVERTERS / 20.1

### 20.1 A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications

#### Layout Tree Structures

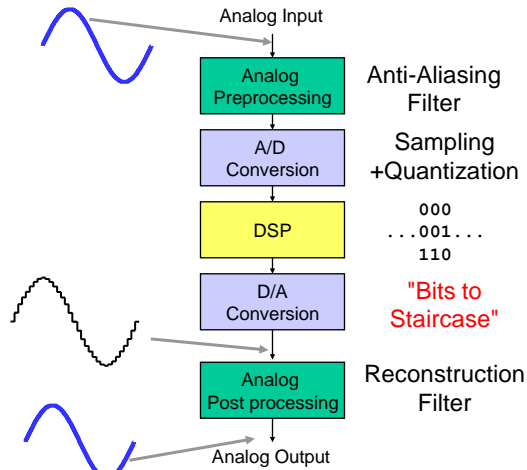


# DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog

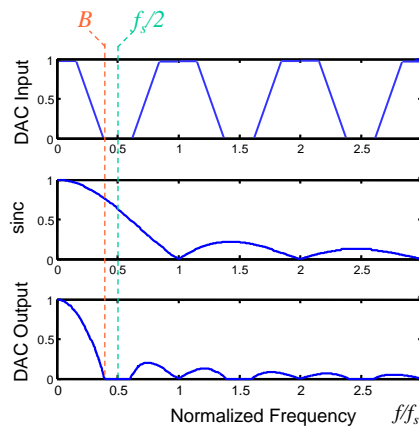
- DAC output → staircase form

- Some applications require filtering (smoothing) of DAC output
  - Reconstruction filter

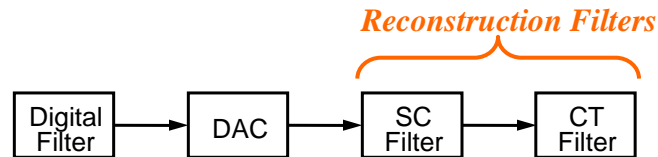


# DAC Reconstruction Filter

- Output of DAC:
  - Frequency domain: DAC input spectrum shaped by S/H sinc function
  - Time domain: Staircase shaped waveform
- Tasks:
  - Correct for sinc droop if needed
  - Remove “aliases” (stair-case approximation)
    - Reconstruction filter: Need and requirements depend on application

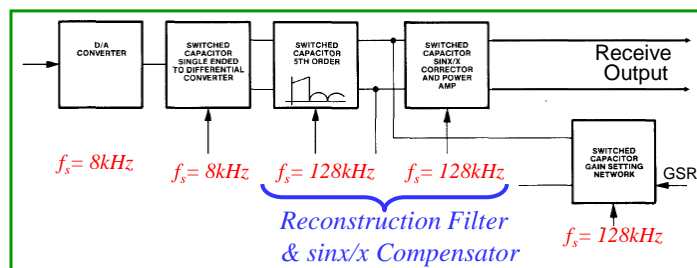


## Reconstruction Filter Options



- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth  $B \ll f_s/2$ )
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band  $\text{sinc}/x$  amplitude droop associated with the inherent DAC S/H function

## DAC Reconstruction Filter Example: Voice-Band CODEC Receive Path



Note:  $f_{sig}^{max} = 3.4kHz$

$f_s^{DAC} = 8kHz$

$$\rightarrow \sin(\pi f_{sig}^{max} x T_s) / (\pi f_{sig}^{max} x T_s)$$

$$= -2.75 \text{ dB droop due to DAC } \text{sinc}/x \text{ shape}$$

Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip,"  
*IEEE Journal of Solid-State Circuits*, Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.



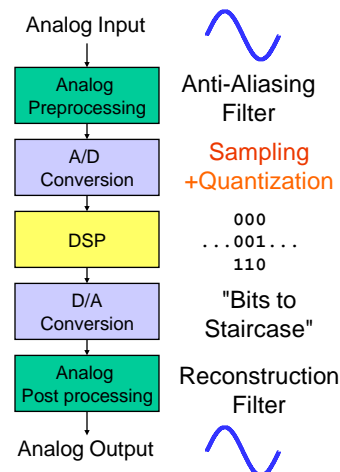
## Summary D/A Converter

- D/A architecture
  - Unit element – complexity proportional to  $2^B$ - excellent DNL
  - Binary weighted- complexity proportional to  $B$ - poor DNL
  - Segmented- unit element MSB( $B_1$ )+ binary weighted LSB( $B_2$ )
    - Complexity proportional  $((2^{B_1}-1) + B_2)$  -DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Time constants, Glitches
- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching
- Depending on the application, reconstruction filter may be needed

## What Next?

### • ADC Converters:

- Need to build circuits that "sample"
- Need to build circuits for amplitude quantization



# Analog-to-Digital Converters

- Two categories:

- Nyquist rate ADCs  $\rightarrow f_{sig}^{max} \sim 0.5x f_{sampling}$ 
  - Maximum achievable signal bandwidth higher compared to oversampled type
  - Resolution limited to max. 14bits
- Oversampled ADCs  $\rightarrow f_{sig}^{max} \ll 0.5x f_{sampling}$ 
  - Maximum achievable signal bandwidth significantly lower compared to nyquist
  - Maximum achievable resolution high (18 to 20bits!)

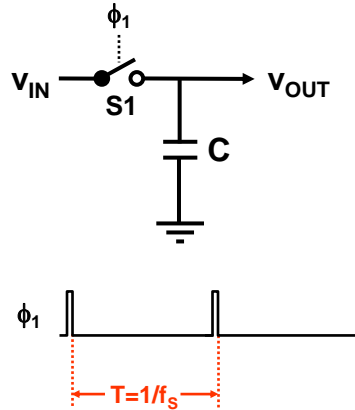
# MOS Sampling Circuits

## Ideal Sampling

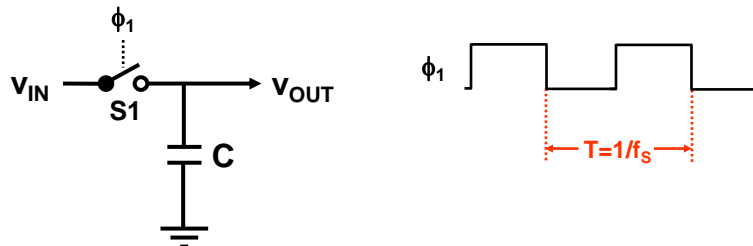
- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage  $v_{IN}$  onto the capacitor  $C$

→ Output Dirac-like pulses with amplitude equal to  $V_{IN}$  at the time of sampling

- In practice not realizable!

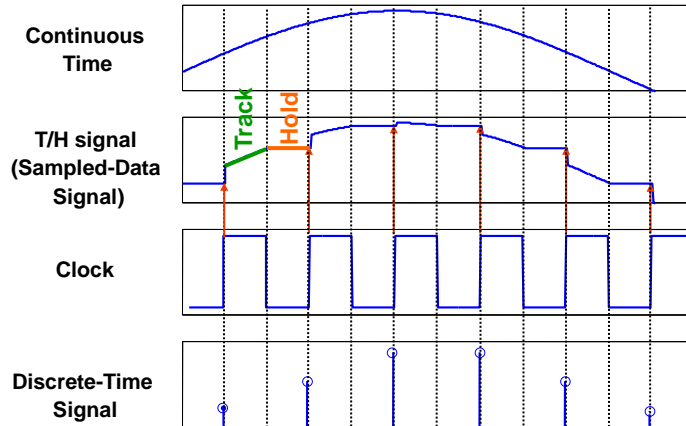


## Ideal Track & Hold Sampling

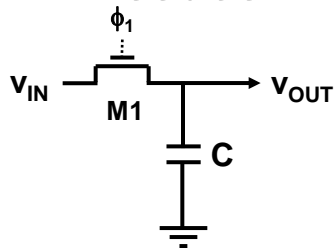


- $V_{out}$  tracks input for  $\frac{1}{2}$  clock cycle when switch is closed
- Ideally acquires *exact* value of  $V_{in}$  at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)

## Ideal T/H Sampling

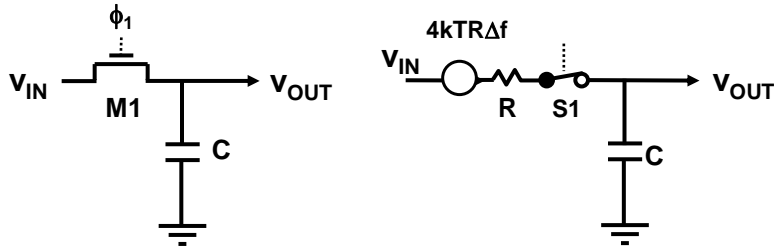


## Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite  $R_{sw}$   $\rightarrow$  limited bandwidth  $\rightarrow$  finite acquisition time
- $R_{sw} = f(V_{in}) \rightarrow$  distortion
- Switch charge injection & clock feedthrough

## Sampling Circuit kT/C Noise



- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in  $\rightarrow$  Total noise variance =  $kT/C$  @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs  $kT/C$  noise at times dominates overall minimum signal handling capability (power dissipation considerations).

## Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times larger compared to quantization noise:

Assumption:  $\rightarrow$  Nyquist rate ADC

For a Nyquist rate ADC : Total quantization noise power  $\approx \frac{\Delta^2}{12}$

Choose C such that thermal noise level is less (or equal) than Q noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$\rightarrow C \geq 12k_B T \left( \frac{2^B - 1}{V_{FS}} \right)^2$$

$$\rightarrow C \geq 12k_B T \times \frac{2^{2B}}{V_{FS}^2}$$

## Sampling Network kT/C Noise

$$C \geq 12k_B T \frac{2^{2B}}{V_{FS}^2}$$

Required $C_{\min}$ as a Function of ADC Resolution		
B	$C_{\min}$ ( $V_{FS} = 1V$ )	$C_{\min}$ ( $V_{FS} = 0.5V$ )
8	0.003 pF	0.012 pF
12	0.8 pF	2.4 pF
14	13 pF	52 pF
16	206 pF	824 pF
20	52,800 pF	211,200 pF

**The large area required for C → limit highest achievable resolution for Nyquist rate ADCs**

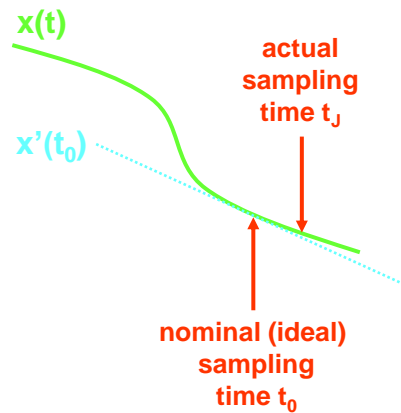
Oversampling results in reduction of required value for C (will be covered in oversampled converter lectures)

## Clock Jitter

- So far : clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Real clock generator → some level of variability
- Variability in T causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"
- What is the effect of clock jitter on ADC performance?

# Clock Jitter

- Sampling jitter adds an error voltage proportional to the product of  $(t_J - t_0)$  and the derivative of the input signal at the sampling instant

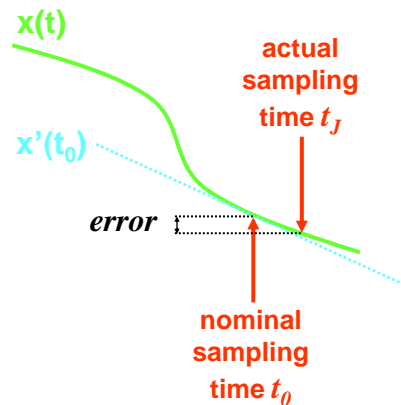


# Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$

- Does jitter matter when sampling dc signals ( $x'(t_0) = 0$ )?



## Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

Amplitude:  $A$   
 Frequency:  $f_x$   
 Jitter:  $dt$

$$x(t) = A \sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x A \cos(2\pi f_x t)$$

$$|x'(t)|_{max} \leq 2\pi f_x A$$

Requirement:

$$|e(t)| \leq |x'(t)|_{max} dt$$

$$|e(t)| \leq 2\pi f_x A dt$$

Worst case

$$A = A_{FS}/2 \quad f_x = f_s/2$$

$$|e(t)| \ll \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt \ll \frac{1}{2^B \pi f_s}$$

# of Bits	$f_s$	$dt \ll$
12	1 MHz	78 ps
16	20 MHz	0.24 ps
12	1000 MHz	0.07 ps

## Statistical Jitter Analysis

- The worst case looks pretty stringent ... what about the “average”?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal
  - $x(t) = A \sin(2\pi f_x t)$ ,
  - then
    - $x'(t) = 2\pi f_x A \cos(2\pi f_x t)$
    - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance  $E\{(t_j - t_0)^2\} = \tau^2$



# Statistical Jitter Analysis

- If  $x'(t)$  and the jitter are independent  

$$- E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\} E\{(t_J - t_0)^2\}$$

- Hence, the jitter error power is

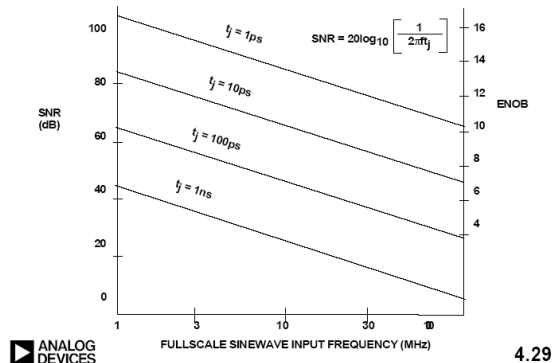
$$E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2$$

- If the jitter is uncorrelated from sample to sample, this “jitter noise” is white

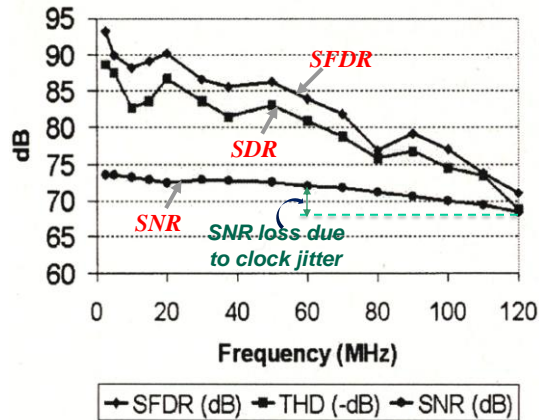
# Statistical Jitter Analysis

$$\begin{aligned} DR_{\text{jitter}} &= \frac{A^2 / 2}{2\pi^2 f_x^2 A^2 \tau^2} \\ &= \frac{1}{2\pi^2 f_x^2 \tau^2} \\ &= -20 \log_{10}(2\pi f_x \tau) \end{aligned}$$

SNR DUE TO APERTURE AND SAMPLING CLOCK JITTER



## Example: ADC Spectral Tests



Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits*, Dec. 2001

## More on Jitter

- In cases where clock signal is provided from off-chip → have to choose a clock signal source with low enough jitter
  - On-chip precautions to keep the clock jitter less than single-digit pico-second :
    - Separate supplies as much as possible
    - Separate analog and digital clocks
    - Short inverter chains between clock source and destination
  - Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
    - RMS noise proportional to input signal frequency
    - RMS noise proportional to input signal amplitude
- In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...