EE247
Lecture 16

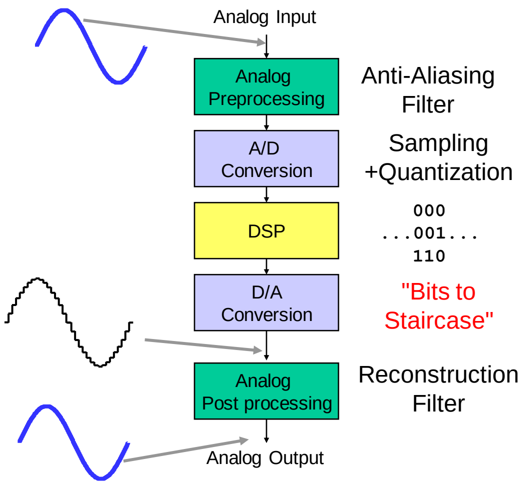
- **D/A Converters (continued)**
  - DAC reconstruction filter
- **ADC Converters**
  - Sampling
    - Sampling switch considerations
      - Thermal noise due to switch resistance
      - Clock jitter related non-idealities
      - Sampling switch bandwidth limitations
      - Switch conductance non-linearity induced distortion
        - Sampling switch conductance dependence on input voltage
        - Clock voltage boosters
      - Sampling switch charge injection & clock feedthrough

Summary Last Lecture

- D/A converters
  - Practical aspects of current-switched DACs (continued)
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations
  - Self calibration techniques
    - Current copiers
    - Dynamic element matching

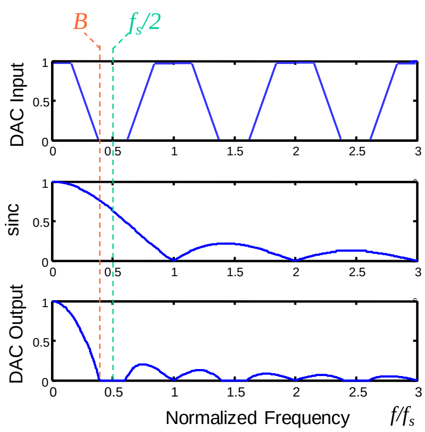
DAC In the Big Picture

- Learned to build DACs
  - Convert the incoming digital signal to analog
- DAC output → staircase form
- Some applications require filtering (smoothing) of DAC output
  → Reconstruction filter

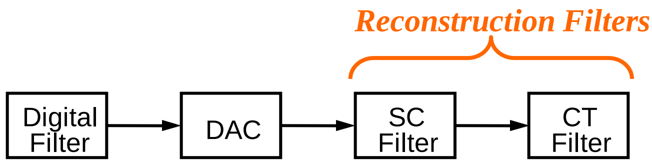


DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc droop
  - Remove "aliases" (stair-case approximation)

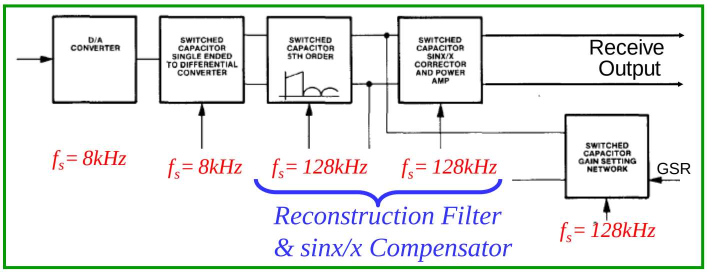


Reconstruction Filter Options



- Reconstruction filter options:
  - Continuous-time filter only
  - CT + SC filter
- SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter
  - Band limits the input signal → prevent aliasing
  - Could also provide high-frequency pre-emphasis to compensate in-band *sinx/x* amplitude droop associated with the inherent DAC S/H function

DAC Reconstruction Filter
Example: Voice-Band CODEC Receive Path



Note: $f_{sig}^{max} = 3.4kHz$

$f_s^{DAC} = 8kHz$

$\rightarrow sin(\pi f_{sig}^{max} x\ T_s)/(\pi f_{sig}^{max} xT_s)$

$= -2.75$ *dB droop due to DAC sinx/x shape*

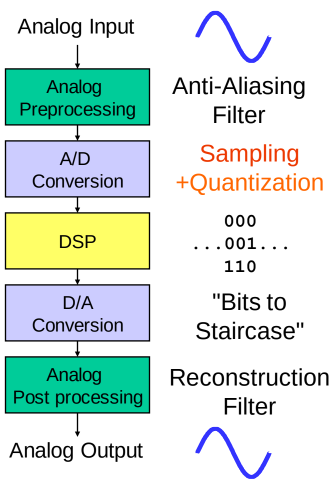
Ref: D. Senderowicz et. al, "A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip," *IEEE Journal of Solid-State Circuits*, Vol.-SC-17, No. 6, pp.1014-1023, Dec. 1982.

Summary
D/A Converter

- D/A architecture
  - Unit element – complexity proportional to 2^B- excellent DNL
  - Binary weighted- complexity proportional to B- poor DNL
  - Segmented- unit element $MSB(B_1)$+ binary weighted $LSB(B_2)$
    - → Complexity proportional $((2^{B1}-1) + B_2)$ -DNL compromise between the two
- Static performance
  - Component matching
- Dynamic performance
  - Time constants, Glitches
- DAC improvement techniques
  - Symmetrical switching rather than sequential switching
  - Current source self calibration
  - Dynamic element matching
- Depending on the application, reconstruction filter may be needed

What Next?

- ADC Converters:
  - Need to build circuits that "sample“
  - Need to build circuits for amplitude quantization



Analog-to-Digital Converters

- Two categories:
  - Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to <14bits
  - Oversampled ADCs → $f_{sig}^{max} << 0.5xf_{sampling}$
    - Maximum achievable signal bandwidth significantly lower compared to nyquist
    - Maximum achievable resolution high (18 to 20bits!)

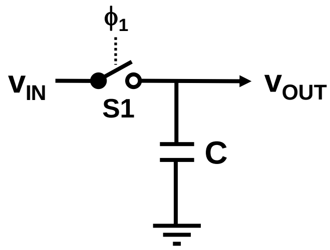
MOS Sampling Circuits

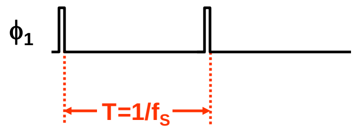
Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage v_{IN} onto the capacitor C

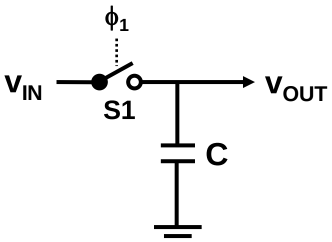
    → Output Dirac-like pulses with amplitude equal to V_{IN} at the time of sampling

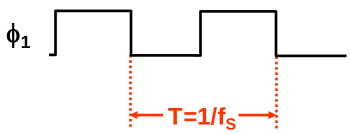
- In practice not realizable!





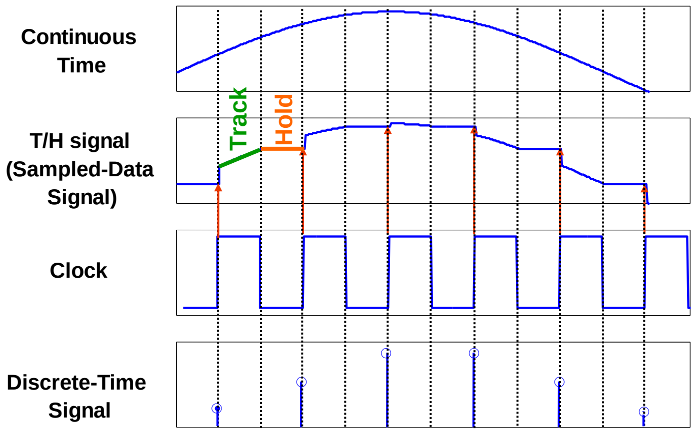
Ideal Track & Hold Sampling



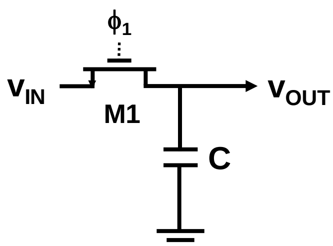


- V_{out} tracks input for ½ clock cycle when switch is closed
- Ideally acquires *exact* value of V_{in} at the instant the switch opens
- "Track and Hold" (T/H) (often called Sample & Hold!)

Ideal T/H Sampling

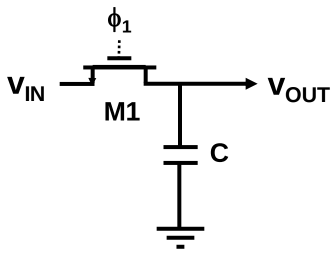


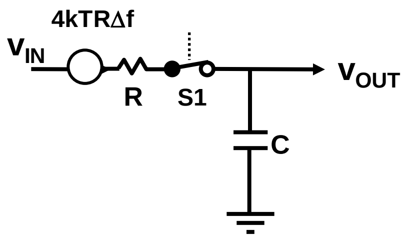
Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of ϕ_1)
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Sampling Circuit kT/C Noise





- Switch resistance & sampling capacitor form a low-pass filter
- Noise associated with the switch resistance results in → Total noise variance= kT/C @ the output (see noise analysis in Lecture 1)
- In high resolution ADCs with such sampling circuit right at the input, kT/C noise at times dominates overall minimum signal handling capability (power dissipation considerations).

Sampling Network kT/C Noise

For ADCs sampling capacitor size is usually chosen based on having thermal noise smaller or equal or at times slightly larger compared to quantization noise:
Assumption: → Nyquist rate ADC

For a Nyquist rate ADC : Total quantization noise power $\approx \frac{\Delta^2}{12}$

Choose C such that thermal noise level is less (or equal) than Q noise

$$\frac{k_B T}{C} \le \frac{\Delta^2}{12}$$

$$\rightarrow \qquad C \ge 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

$$\rightarrow \qquad \boxed{C \ge 12 k_B T \times \frac{2^{2B}}{V_{FS}{}^2}}$$

Sampling Network kT/C Noise

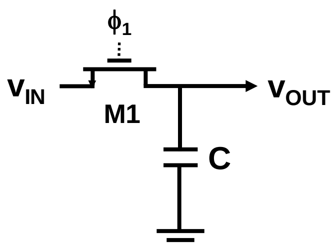
$$C \geq 12 k_B T \frac{2^{2B}}{{V_{FS}}^2}$$

Required C_{min} as a Function of ADC Resolution		
B	C_{min} (V_{FS} = 1V)	C_{min} (V_{FS} = 0.5V)
8	0.003 pF	0.012 pF
12	0.8 pF	2.4 pF
14	13 pF	52 pF
16	206 pF	824 pF
20	52,800 pF	211,200 pF

The large area required for C → limit highest achievable resolution for Nyquist rate ADCs

Oversampling results in reduction of required value for C (will be covered in oversampled converter lectures)

Practical Sampling Issues



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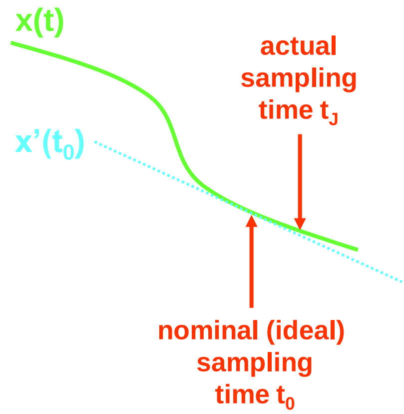
Clock Jitter

- So far : clock signal controls sampling instants – which we assumed to be precisely equi-distant in time (period T)
- Real clock generator → some level of variability
- Variability in T causes errors
  - "Aperture Uncertainty" or "Aperture Jitter"
- What is the effect of clock jitter on ADC performance?

Clock Jitter

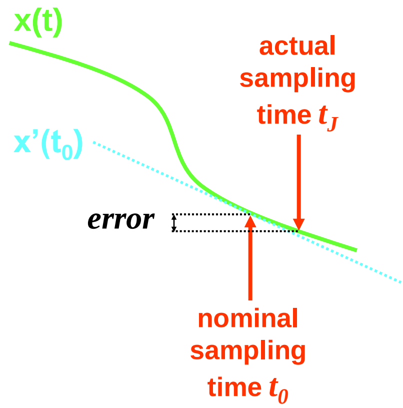
- Sampling jitter adds an error voltage proportional to the product of (t_J-t_0) and the derivative of the input signal at the sampling instant



Clock Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



- Does jitter matter when sampling dc signals ($x'(t_0)=0$)?

Effect of Clock Jitter on Sampling of a Sinusoidal Signal

Sinusoidal input

Amplitude: A
Frequency: f_x
Jitter: dt

$$x(t) = A\sin(2\pi f_x t)$$

$$x'(t) = 2\pi f_x A\cos(2\pi f_x t)$$

$$|x'(t)|_{max} \le 2\pi f_x A$$

Then:

$$|e(t)| \le |x'(t)|_{max}\, dt$$

$$|e(t)| \le 2\pi f_x A dt$$

Worst case

$$A = A_{FS}/2 \qquad f_x = f_s/2$$

$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$

$$dt << \frac{1}{2^B \pi f_s}$$

# of Bits	f_s	dt <<
12	1 MHz	78 ps
16	20 MHz	0.24 ps
12	1000 MHz	0.07 ps

Statistical Jitter Analysis

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal

  $x(t) = A\sin(2\pi f_x t)$,

  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- Assume the jitter has variance $E\{(t_J - t_0)^2\} = \tau^2$

Statistical Jitter Analysis

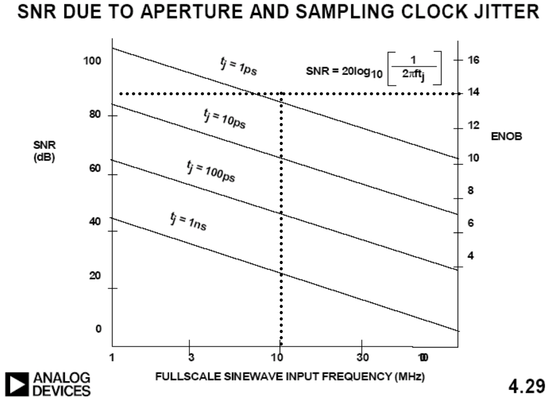
- If x'(t) and the jitter are independent
  - $E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\}\ E\{(t_J - t_0)^2\}$
- Hence, the jitter error power is

$$\mathbf{E\{e^2\} = 2\pi^2 f_x^2 A^2 \tau^2}$$

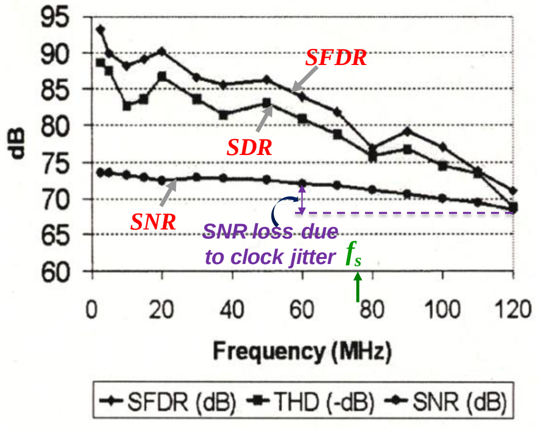
- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

Statistical Jitter Analysis

$$DR_{\text{jitter}} = \frac{A^2/2}{2\pi^2 f_x^2 A^2 \tau^2} = \frac{1}{2\pi^2 f_x^2 \tau^2} = -20\log_{10}(2\pi f_x \tau)$$



Example: ADC Spectral Tests



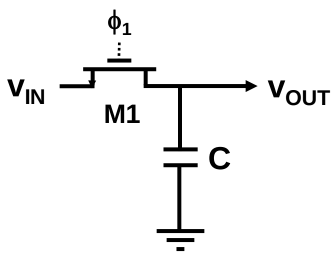
Ref: W. Yang et al., "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. of Solid-State Circuits,* Dec. 2001

Summary
Effect of Clock Jitter on ADC Performance

- In cases where clock signal is provided from off-chip→ have to choose a clock signal source with low enough jitter
- On-chip precautions to keep the clock jitter less than single-digit pico-second :
  - Separate supplies as much as possible
  - Separate analog and digital clocks
  - Short on-chip inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input signal frequency
  - RMS noise proportional to input signal amplitude

  →In cases where clock jitter limits the dynamic range, it's easy to tell, but may be difficult to fix...

Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of ϕ_1)
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

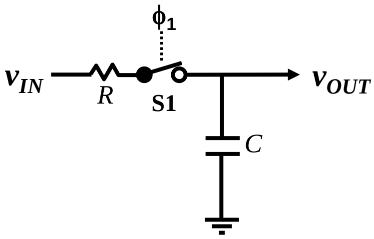
Sampling Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with finite time constant:

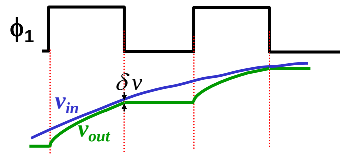
  $\tau = RC$

- Assuming V_{in} is constant or changing slowly during the sampling period and C is initially discharged

- Need to allow enough time for the output to settle to less than 1 ADC LSB → determines minimum duration for ϕ_1 or maximum ADC operating freq.



$$v_{out}(t) = v_{in}\left(1 - e^{-t/\tau}\right)$$



Sampling: Effect of Finite Switch On-Resistance

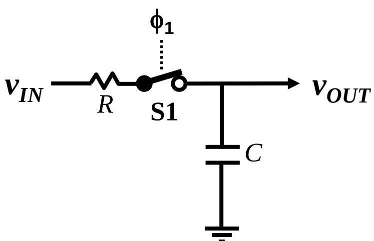
$$V_{in}^{tx} - V_{out}^{tx} << \Delta \quad \text{since } V_{out} = V_{in}\left(1 - e^{-t/\tau}\right)$$

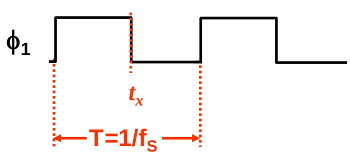
$$\rightarrow V_{in} e^{-T_s/2\tau} << \Delta \;\; or \;\; \tau << \frac{T_s}{2}\frac{1}{\ln\left(V_{in}/\Delta\right)}$$

Worst Case: $V_{in} = V_{FS}$

$$\tau << \frac{T_s}{2}\frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72 \times T_s}{B}$$

$$R << \frac{1}{2 f_s C}\frac{1}{\ln\left(2^B - 1\right)} \approx \frac{0.72}{B f_s C}$$



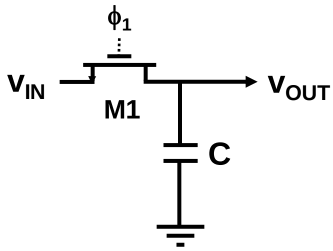


Example:

$B = 14, \quad C_{min} = 13pF, \quad f_s = 100MHz$

$T_s/\tau >> 19.4$, or $10\tau << T_s/2$ → $R << 40\,\Omega$

Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter (edge variation of ϕ_1)
- Finite R_{sw} → limited bandwidth → finite acquisition time
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- Switch charge injection & clock feedthrough

Non-Linear Switch On-Resistance

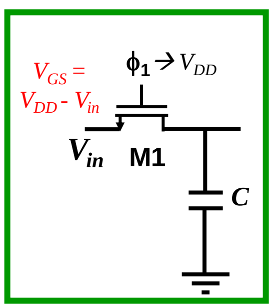
Switch→ MOS operating in triode mode:

$$I_{D(triode)} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}, \qquad \frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_{in})}$$

Let us call R @ V_{in}=0 R_o *then* $R_o = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th})}$

$$R_{ON} = \frac{R_o}{1 - \frac{V_{in}}{V_{DD} - V_{th}}}$$



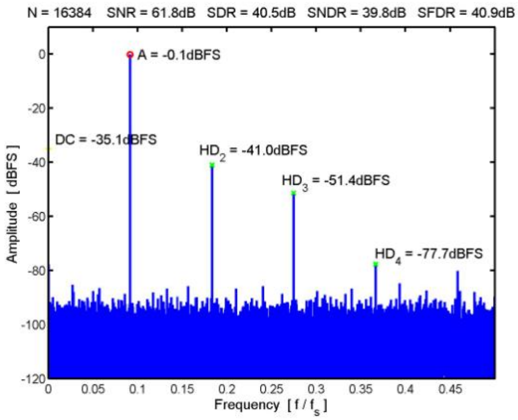
Sampling Distortion

Simulated 10-Bit ADC &
Sampling Switch modeled:

$$v_{out} = v_{in}\left(1-e^{-\frac{T}{2\tau}\left(1-\frac{V_{in}}{V_{DD}-V_{th}}\right)}\right)$$

$T_s/2 = 5\,\tau$
$V_{DD} - V_{th} = 2V$
$V_{FS} = 1V$

→Results in
HD2=-41dBFS &
HD3=-51.4dBFS



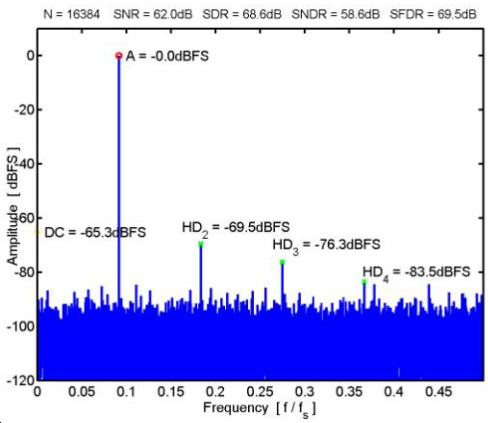
Sampling Distortion

Doubling sampling time (or ½ time constant)
Results in:

HD2 improved from -41dBFS to -70dBFS ~30dB

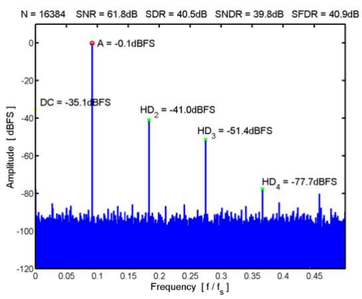
HD3 improved from -51.4dBFS to -76.3dBFS ~25dB

Allowing enough time for the sampling network settling → Reduces distortion due to switch R non-linear behavior to a tolerable level



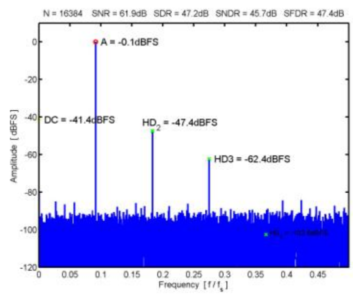
10bit ADC $T_s/2 = 10\,\tau$
$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$

Sampling Distortion
Effect of Supply Voltage



10bit ADC & $T_s/2 = 5\tau$

$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$



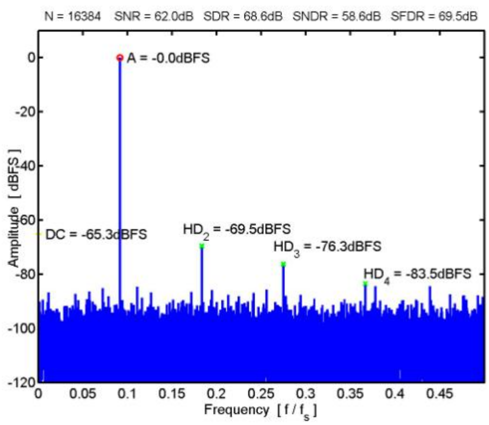
10bit ADC & $T_s/2 = 5\tau$

$V_{DD} - V_{th} = 4V$ $V_{FS} = 1V$

- Effect of higher supply voltage on sampling distortion
  → HD3 decreased by $(V_{DD1}/V_{DD2})^2$
  → HD2 decreased by (V_{DD1}/V_{DD2})

Sampling Distortion

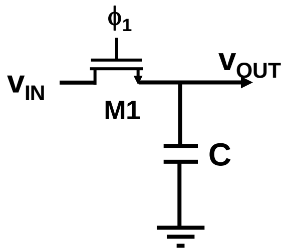
- SFDR → sensitive to sampling distortion - improve linearity by:
  - Larger V_{DD}/V_{FS}
  - Higher sampling bandwidth
- Solutions:
  - Overdesign→ Larger switches
    Issue:
    → Increased switch charge injection
    → Increased nonlinear *S &D* junction cap.
  - Maximize V_{DD}/V_{FS}
    →Decreased dynamic range if V_{DD} const.
  - Complementary switch
  - Constant & max. $V_{GS} \neq f(V_{in})$



10bit ADC T_s/τ = **20**

$V_{DD} - V_{th} = 2V$ $V_{FS} = 1V$

Practical Sampling
Summary So Far!



- *kT/C* noise

$$C \geq 12 k_B T \frac{2^{2B}}{V_{FS}^{\ 2}}$$

- Finite R_{sw} → limited bandwidth

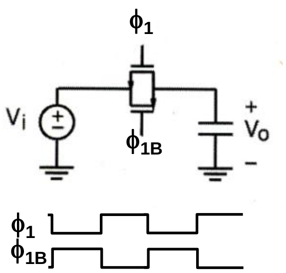
$$R << \frac{0.72}{B\, f_s C}$$

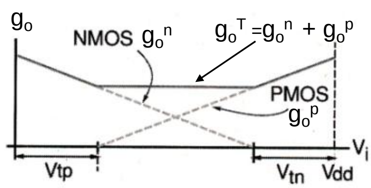
- $g_{sw} = f\,(V_{in})$ → distortion

$$g_{ON} = g_o\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right) \quad \text{for} \quad g_o = \mu C_{ox} \frac{W}{L}\left(V_{DD} - V_{th}\right)$$

- Allowing long enough settling time → reduce distortion due to sw non-linear behavior

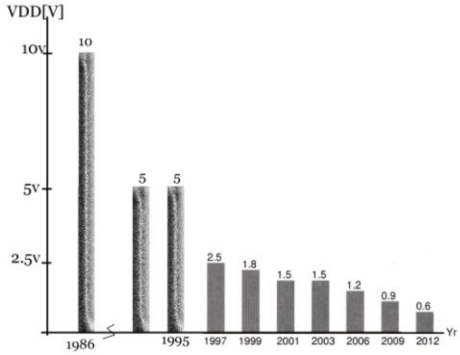
Sampling
Use of Complementary Switches





- Complementary n & p switch advantages:
  - ✓Increase in the overall conductance → lower time constant
  - ✓Linearize the switch conductance for the range $|V_{th}^{p}| <$ Vin < Vdd $-|V_{th}^{n}|$

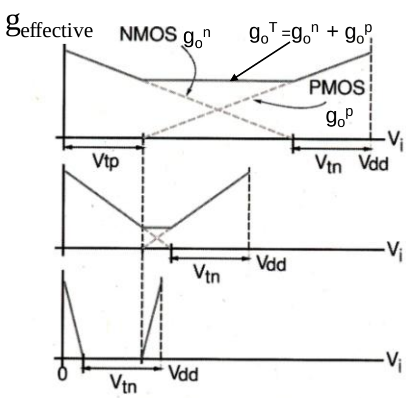
Complementary Switch Issues
Supply Voltage Evolution

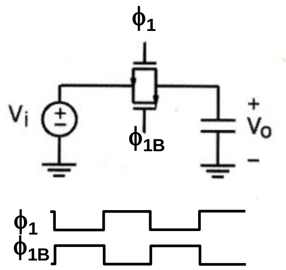


- Supply voltage has scaled down with technology scaling
- Threshold voltages do not scale accordingly

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

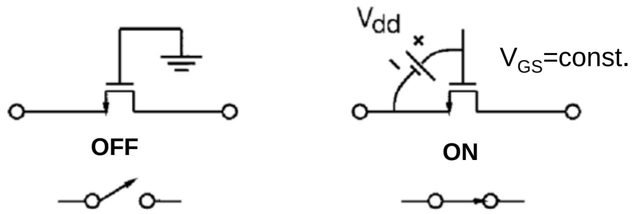
Complementary Switch
Effect of Supply Voltage Scaling





•As supply voltage scales down input voltage range for constant g_o shrinks
→ Complementary switch not effective when V_{DD} becomes comparable to $2xV_{th}$

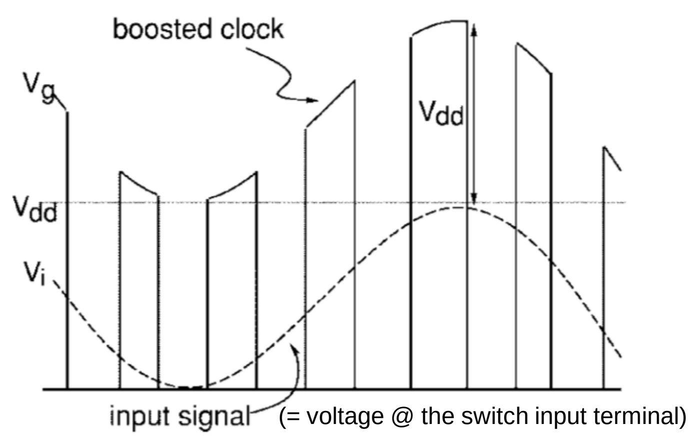
Boosted & Constant V_{GS} Sampling



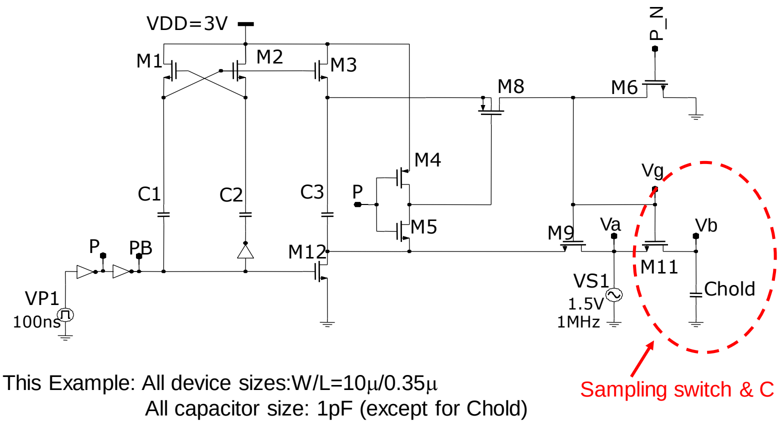
- Gate voltage V_{GS} =low
  - ➢ Device off
  - ➢ Beware of signal feedthrough due to parasitic capacitors

- Increase gate overdrive voltage as much as possible + keep V_{GS} constant
  - ➢ Switch overdrive voltage independent of signal level
  - ➢ Error due to finite R_{ON} linear (to 1st order)
  - ➢ Lower R_{on} → lower time constant

Constant V_{GS} Sampling



Constant V_{GS} Sampling Circuit



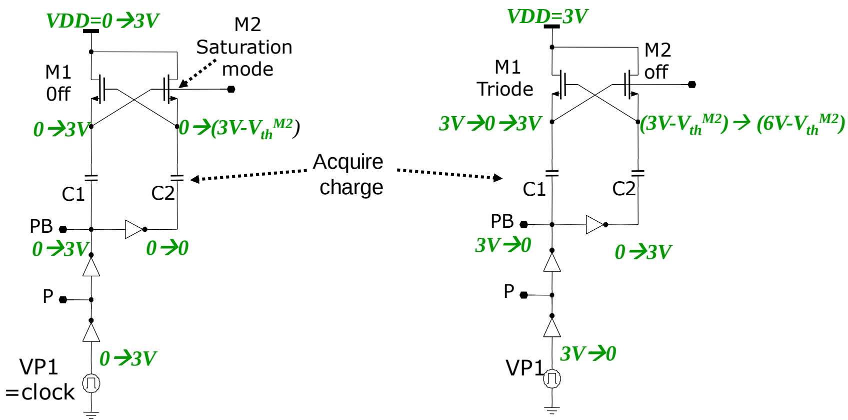
This Example: All device sizes:W/L=10μ/0.35μ

All capacitor size: 1pF (except for Chold)

Note: Each critical switch requires a separate clock booster

Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

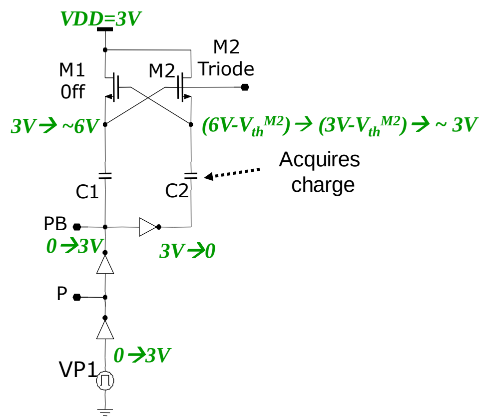
Clock Voltage Doubler



a) Start–up

b) Next clock phase

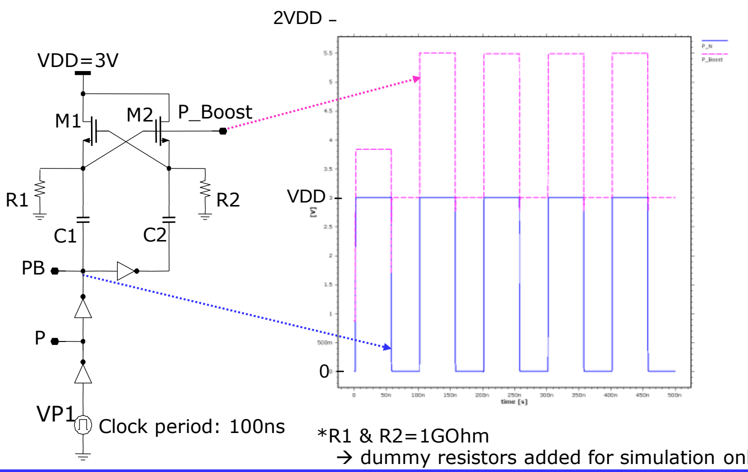
Clock Voltage Doubler



c) Next clock phase

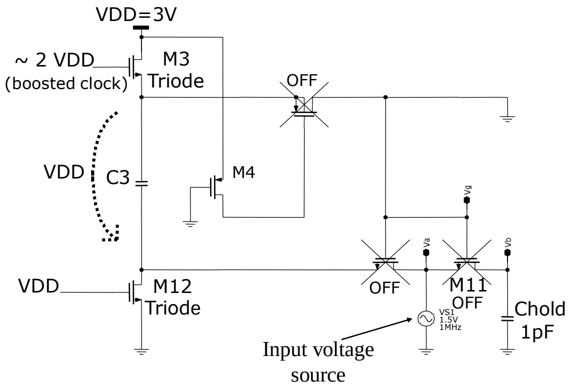
- Both C1 & C2 → charged to VDD after 1.5 clock cycle
- Note that bottom plate of C1 & C2 is either 0 or VDD while top plates are at VDD or 2VDD

Clock Voltage Doubler

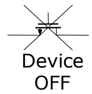


*R1 & R2=1GOhm
→ dummy resistors added for simulation only

Constant V_{GS} Sampler: Φ Low

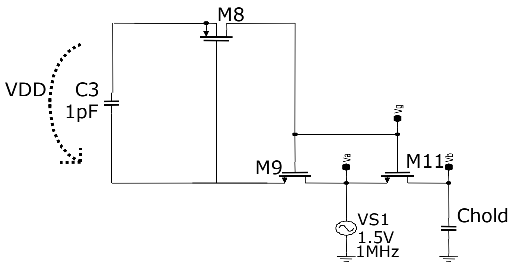


- Sampling switch M11 is OFF



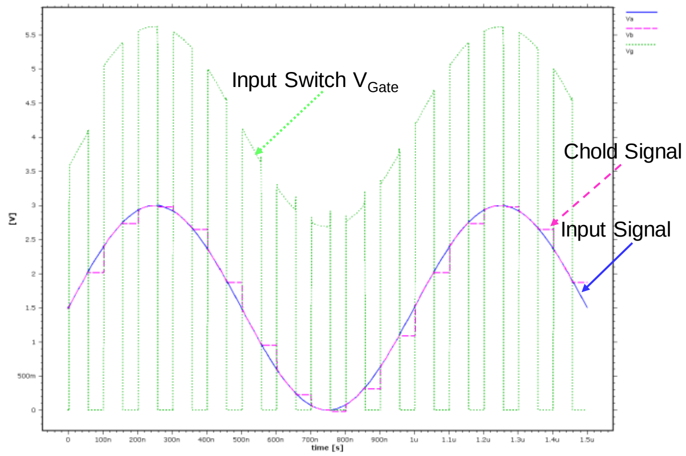
- C3 charged to ~VDD

Constant V_{GS} Sampler: Φ High

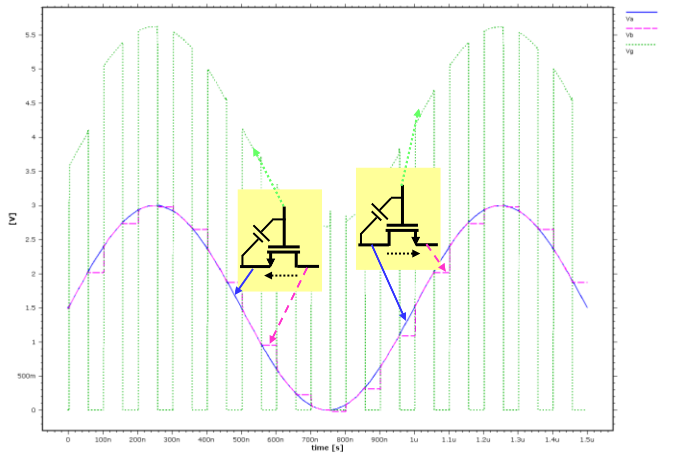


- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD
- Mission accomplished!?

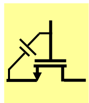
Constant V_{GS} Sampling



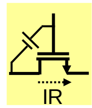
Constant V_{GS} Sampling?



Constant V_{GS} Sampling?



- During the time period: $V_{in}< V_{out}$
  → V_{GS}=constant=V_{DD}
  - Larger V_{GS}-V_{th} compared to no boost
  - V_{GS}=cte and not a function of input voltage
    → Significant linearity improvement



- During the time period: $V_{in}>V_{out}$:
  → V_{GS}= V_{DD} - IR
- Larger V_{GS}-V_{th} compared to no boost
- V_{GS} is a function of IR and hence input voltage
  → Linearity improvement not as pronounced as for $V_{in}< V_{out}$

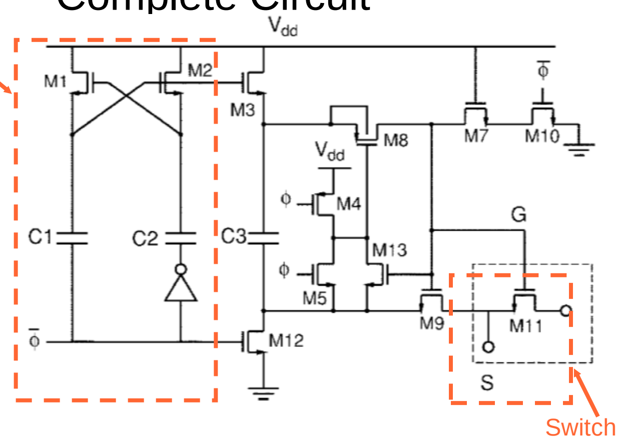
Boosted Clock Sampling Complete Circuit

M7 & M13 for reliability

<u>Remaining issues:</u>

-V_{GS} constant only for V_{in} <V_{out}

-Nonlinearity due to Vth dependence of M11on body-source voltage

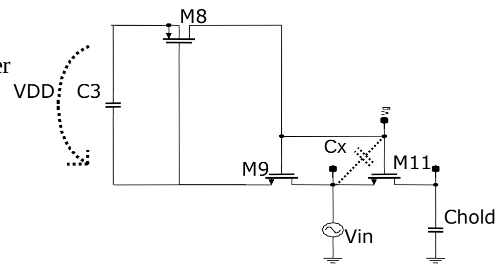


Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Boosted Clock Sampling Design Consideration

Choice of value for C3:

- C3 too large → large charging current → large dynamic power dissipation
- C3 too small→
  Vgate-Vs=
  VDD.C3/(C3+Cx)
  →Loss of VGS due to low ratio of Cx/C3
  Cx includes C_{GS} of M11 plus all other parasitics caps….



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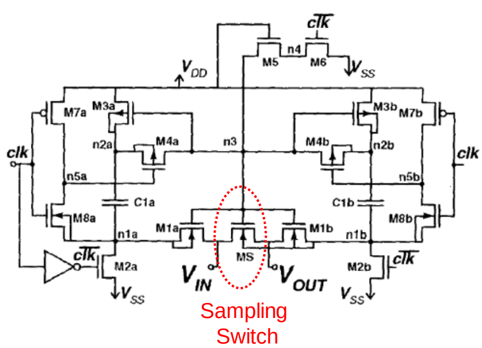
Advanced Clock Boosting Technique

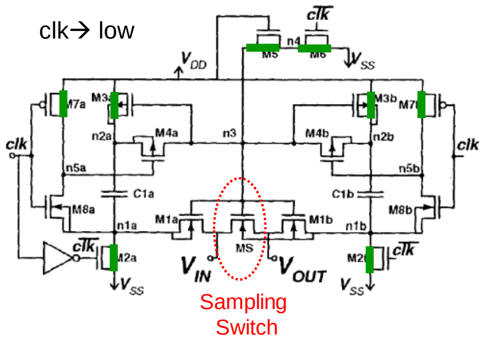


Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314

Two floating voltages sources generated and connected to Gate and S & D

Advanced Clock Boosting Technique

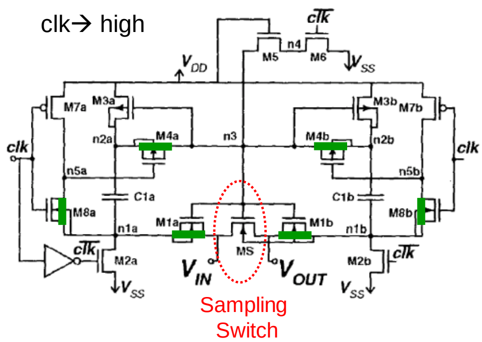
clk→ low



- clk→ low
  - Capacitors C1a & C1b → charged to VDD
  - MS → off
  - Hold mode

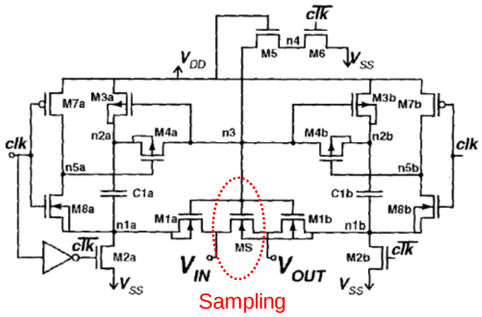
Advanced Clock Boosting Technique

clk→ high



- clk→ high
  - Top plate of C1a & C1b connected to gate of sampling switch
  - Bottom plate of C1a connected to V_{IN}
  - Bottom plate of C1b connected to V_{OUT}
  - VGS & VGD of MS both @ VDD & ac signal on G of MS → average of V_{IN} & V_{OUT}

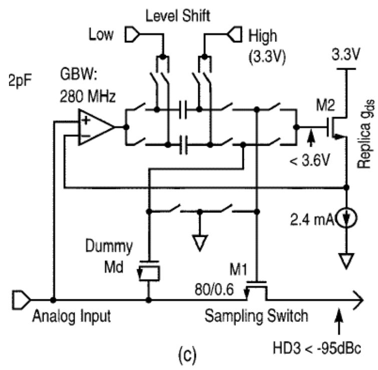
Advanced Clock Boosting Technique



Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314

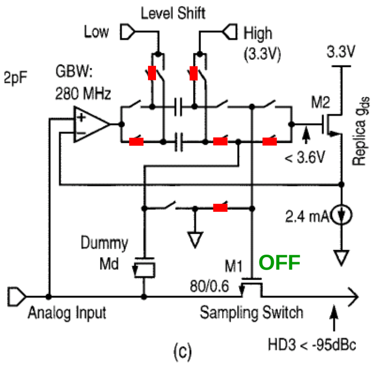
- Gate tracks *average* of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at f_{in}=200MHz

Constant Conductance Switch



Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Constant Conductance Switch



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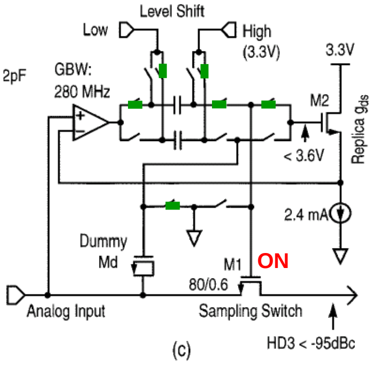
Constant Conductance Switch



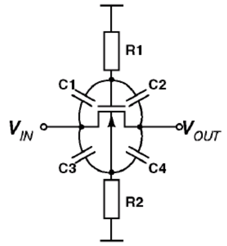
M2→ Constant current
→ constant g_{ds}

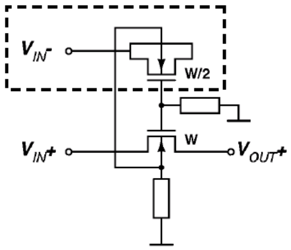
M1→ replica of M2
& same VGS
as M2
→ M1 also
constant g_{ds}

- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range required

Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Switch Off-Mode Feedthrough Cancellation



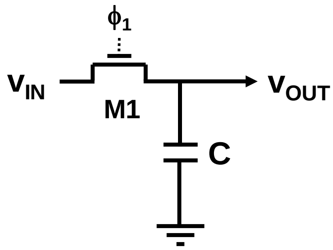


High-pass feedthrough paths past an open switch

Feedthrough cancellation with a dummy switch

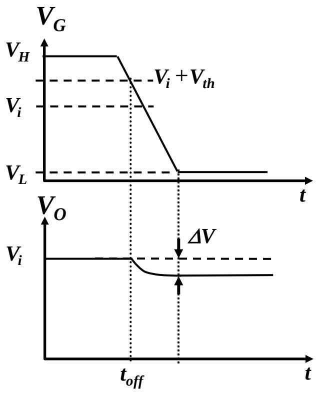
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314

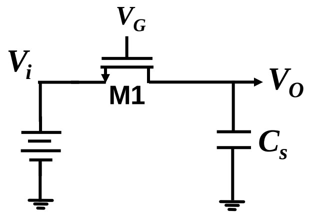
Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Sampling Switch Charge Injection & Clock Feedthrough
Switching from Track to Hold

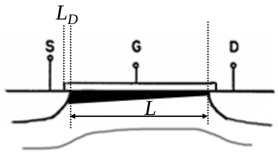




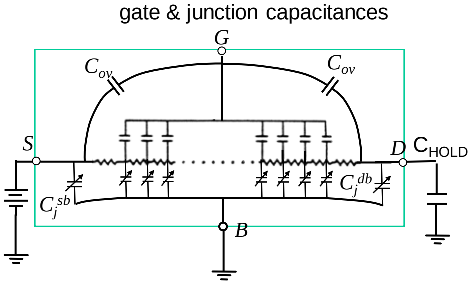
- First assume V_i is a DC voltage
- When switch turns off → offset voltage induced on C_s
- Why ?

Sampling
Switch Charge Injection

MOS xtor operating in triode region
Cross section view

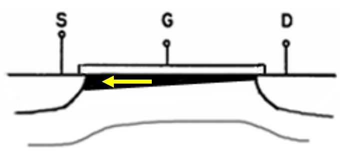


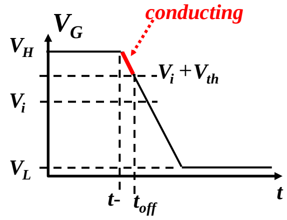
Distributed channel resistance &
gate & junction capacitances



- Channel → distributed RC network formed between G,S, and D
- Channel to substrate junction capacitance → distributed & voltage dependant
- Drain/Source junction capacitors to substrate → voltage dependant
- Over-lap capacitance $C_{ov} = L_D x W x C_{ox}'$ associated with G-S & G-D overlap

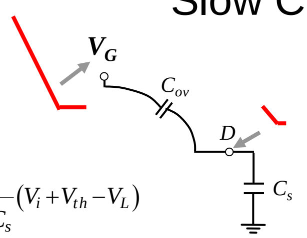
Switch Charge Injection
Slow Clock

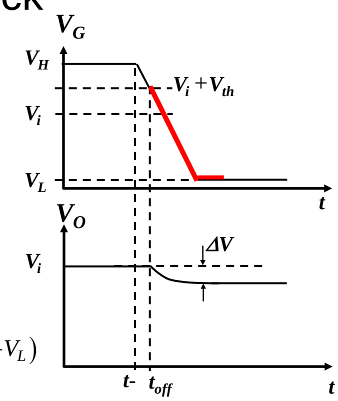




- Slow clock→ clock fall time >> device speed
  → During the period (t- to t_{off}) current in channel discharges channel charge into low impedance signal source
- Only source of error → Clock feedthrough from C_{ov} to C_s

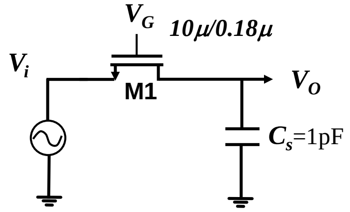
Switch Clock Feedthrough
Slow Clock

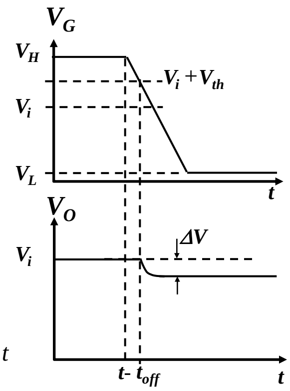




$$\Delta V = -\frac{C_{ov}}{C_{ov}+C_s}(V_i+V_{th}-V_L)$$
$$\approx -\frac{C_{ov}}{C_s}(V_i+V_{th}-V_L)$$
$$V_o = V_i + \Delta V$$
$$V_o = V_i - \frac{C_{ov}}{C_s}(V_i+V_{th}-V_L) = V_i\left(1-\frac{C_{ov}}{C_s}\right) - \frac{C_{ov}}{C_s}(V_{th}-V_L)$$
$$V_o = V_i(1+\varepsilon)+V_{os}$$
$$where\ \varepsilon = -\frac{C_{ov}}{C_s}\ ;\ V_{os} = -\frac{C_{ov}}{C_s}(V_{th}-V_L)$$

Switch Charge Injection & Clock Feedthrough
Slow Clock- Example





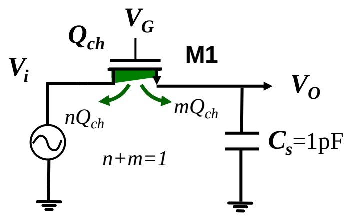
$C'_{ov}=0.1fF/\mu \quad C_{ox}=9fF/\mu^2 \quad V_{th}=0.4V \quad V_L=0$

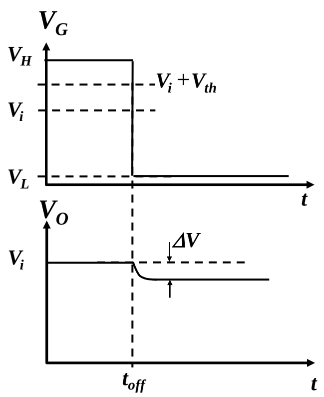
$$\varepsilon=-\frac{C_{ov}}{C_s}=-\frac{10\mu x0.1fF/\mu}{1pF}=-.1\%$$

Allowing $\varepsilon=1/2LSB \rightarrow$ ADC resolution $<\sim 9bit$

$$V_{os}=-\frac{C_{ov}}{C_s}(V_{th}-V_L)=-0.4mV$$

Switch Charge Injection & Clock Feedthrough
Fast Clock

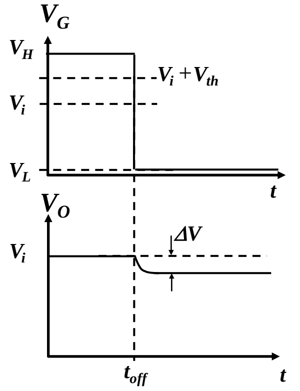




- Sudden gate voltage drop → no gate voltage to establish current in channel → channel charge has no choice but to escape out towards S & D

Switch Charge Injection & Clock Feedthrough Fast Clock

Clock Fall-Time << Device Speed:



$$\Delta V_o = -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2} \times \frac{Q_{ch}}{C_s}$$

$$\approx -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L\left((V_H - V_i - V_{th})\right)}{C_s}$$

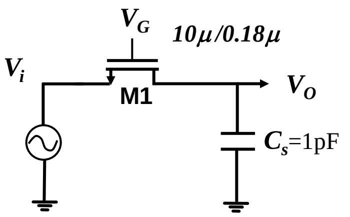
$$V_o = V_i(1+\varepsilon) + V_{os}$$

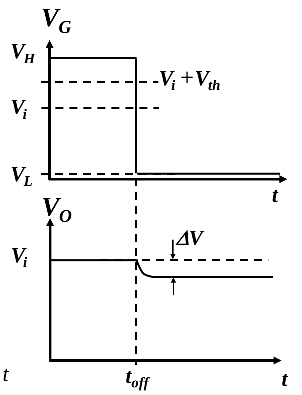
$$where\ \varepsilon = \frac{1}{2} \times \frac{W C_{ox} L}{C_s}$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{th})}{C_s}$$

- For simplicity it is assumed channel charge divided equally between S & D
- Source of error → channel charge transfer + clock feedthrough via C_{ov} to C_s

Switch Charge Injection & Clock Feedthrough Fast Clock- Example



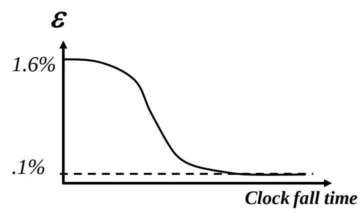


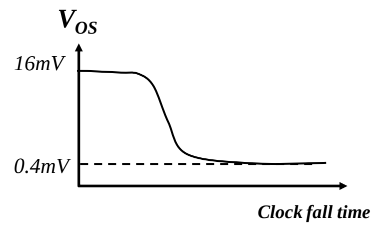
$$C_{ov} = 0.1\frac{fF}{\mu},\ C_{ox} = 9\frac{fF}{\mu^2}, V_{th} = 0.4V, V_{DD} = 1.8V,\ V_L = 0$$

$$\varepsilon = 1/2\frac{WLC_{ox}}{C_s} = \frac{10\mu x 0.18\mu x 9 fF/\mu^2}{1pF} = 1.6\% \rightarrow \sim 5-bit$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2} \times \frac{W C_{ox} L (V_H - V_{th})}{C_s} = -1.8mV - 14.6mV = -16.4mV$$

Switch Charge Injection & Clock Feedthrough Example-Summary





Error function of:

- → Clock fall time
- → Input voltage level
- → Source impedance
- → Sampling capacitance size
- → Switch size
  - Clock fall/rise should be controlled not to be faster (sharper) than necessary

Switch Charge Injection Error Reduction

- How do we reduce the error?
  → Reduce switch size to reduce channel charge?

$$\Delta V_o = -\frac{1}{2}\frac{Q_{ch}}{C_s} \downarrow$$

$$\tau = R_{ON} C_s = \frac{C_s}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \uparrow \qquad \left(note: \frac{T_s}{2} = k\tau\right)$$

Consider the figure of merit (FOM):

$$FOM = \frac{1}{\tau \times \Delta V_o} \approx \frac{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})}{C_s} \times 2 \times \frac{C_s}{W C_{ox} L\left((V_H - V_i - V_{th})\right)}$$

$$\rightarrow FOM \propto \mu / L^2$$

- Reducing switch size increases τ → increased distortion→ not a viable solution
- Small τ and small ΔV → use minimum chanel length (mandated by technology)
- For a given technology τ x ΔV ~ constant

Sampling Switch Charge Injection & Clock Feedthrough Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Channel charge injection
  - Clock feedthrough to C_s via C_{ov}
- Issues due to charge injection & clock feedthrough:
  - DC offset induced on hold C
  - Input dependant error voltage → distortion
- Solutions:
  - Slowing down clock edges as much as possible
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?