EE247
Lecture 17

- Administrative issues
  - Midterm exam postponed to **Thurs. Oct. 28th**
    - o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    - o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    - o Midterm includes material covered to **end of lecture 14**

EE247
Lecture 17

ADC Converters
- Sampling (continued)
  - Sampling switch considerations
    - Clock voltage boosters
    - Sampling switch charge injection & clock feedthrough
      - Complementary switch
      - Use of dummy device
      - Bottom-plate switching
- Track & hold
  - T/H circuits
  - T/H combined with summing/difference function
  - T/H circuit incorporating gain & offset cancellation
  - T/H aperture uncertainty

Practical Sampling Summary So Far!

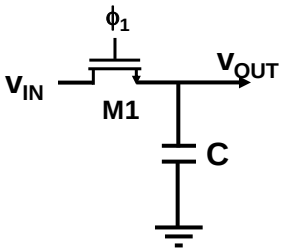
- *kT/C* noise

$$C \geq 12 k_B T \frac{2^{2B}}{V_{FS}{}^2}$$

- Finite R_{sw} → limited bandwidth

$$R << \frac{0.72}{B f_s C}$$

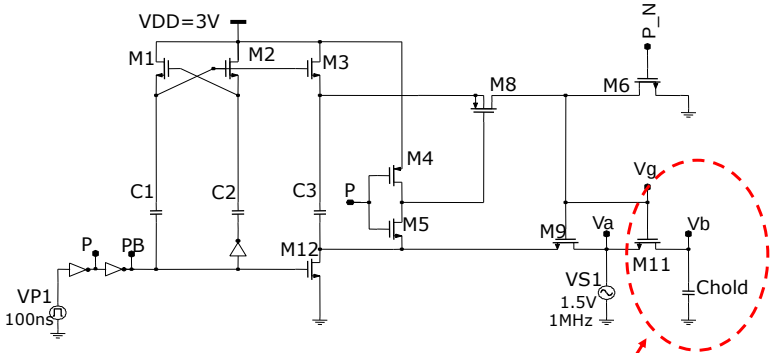
- $g_{sw} = f(V_{in})$ → distortion



$$g_{ON} = g_o\left(1 - \frac{V_{in}}{V_{DD} - V_{th}}\right) \quad \text{for} \quad g_o = \mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{th}\right)$$

- Allowing long enough settling time → reduce distortion due to switch non-linear behavior

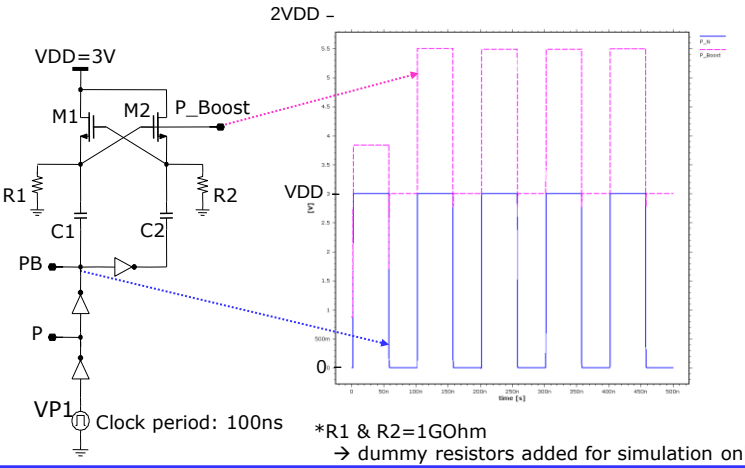
Constant V_{GS} Sampling Circuit



This Example: All device sizes:W/L=10μ/0.35μ
All capacitor size: 1pF (except for Chold)
Note: Each critical switch requires a separate clock booster

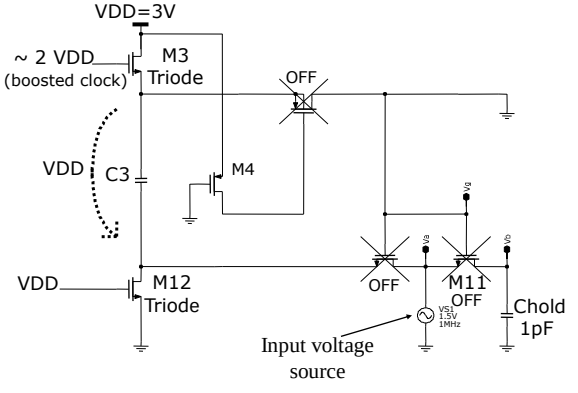
Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Clock Voltage Doubler



*R1 & R2=1GOhm
→ dummy resistors added for simulation only

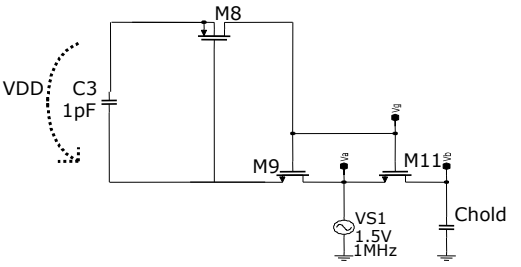
Constant V_{GS} Sampler: Φ Low



- Sampling switch M11 is OFF

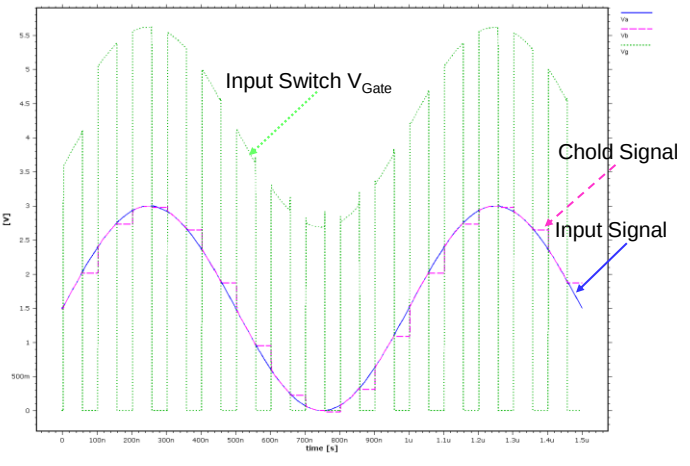
- C3 charged to ~VDD

Constant V_{GS} Sampler: Φ High

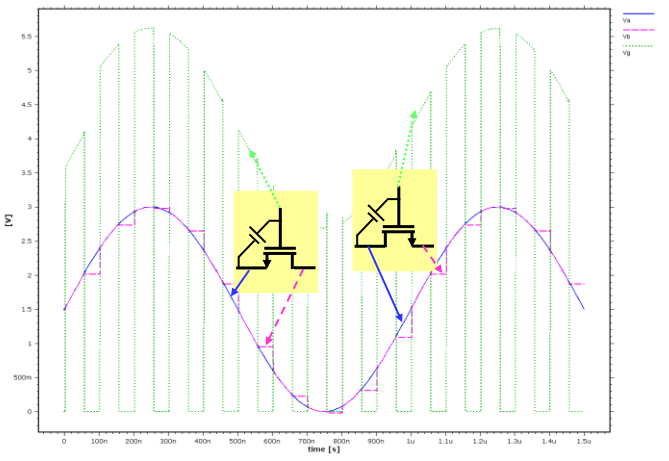


- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD
- Mission accomplished!?

Constant V_{GS} Sampling



Constant V_{GS} Sampling?



Constant V_{GS} Sampling?

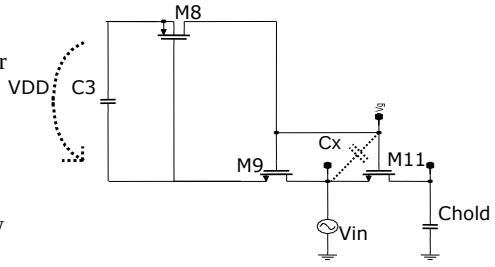
- During the time period: $V_{in} < V_{out}$
  - → V_{GS}=constant=V_{DD}
  - – Larger V_{GS}-V_{th} compared to no boost
  - – V_{GS}=cte and not a function of input voltage
    - → Significant linearity improvement

- During the time period: $V_{in} > V_{out}$:
  - → V_{GS}= V_{DD} - IR
- Larger V_{GS}-V_{th} compared to no boost
- V_{GS} is a function of IR and hence input voltage
  - → Linearity improvement not as pronounced as for $V_{in} < V_{out}$

Boosted Clock Sampling Design Considerations

Choice of value for C3:

- C3 too large → large charging current → large dynamic power dissipation
- C3 too small→ $(Vgate\text{-}Vs)_{M11}$= VDD.C3/(C3+Cx) →Loss of VGS_{M11} due to low ratio of C3/Cx Cx includes C_{GS} of M11 plus all other parasitics caps….



Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

Boosted Clock Sampling Design Considerations

- Reliability issues:
  - Avoid having any of the G-S and G-D, and D-S terminal voltages for ALL circuit devices exceed the maximum V_{DD} prescribed by the SI processing firm.
  - In particular, the thin MOS device gate oxide could gradually sustain damage through getting exposed to higher than prescribed voltage.

Boosted Clock Sampling Complete Circuit

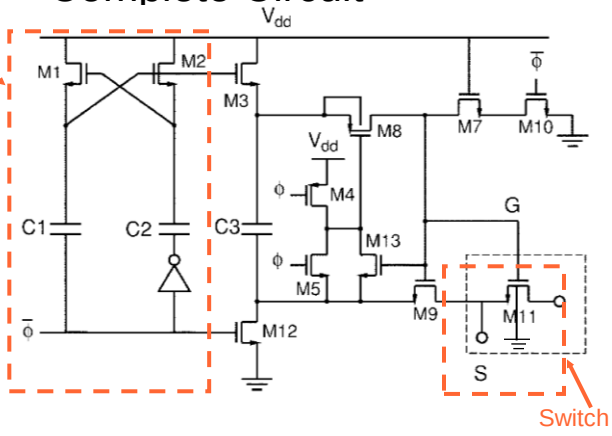
Clock Multiplier

M7 & M13 for reliability

Remaining issues:

-V_{GS} constant only for V_{in} <V_{out}

-Nonlinearity due to Vth dependence of M11on body-source voltage



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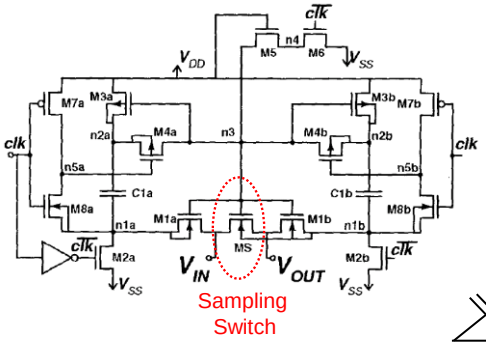
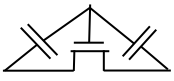
Advanced Clock Boosting Technique



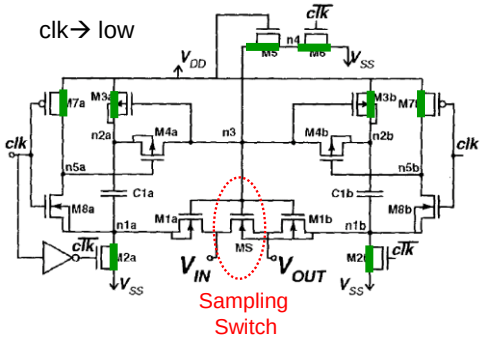
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Tech. Papers, pp. 314



Two floating voltages sources generated and connected to Gate and S & D

Advanced Clock Boosting Technique

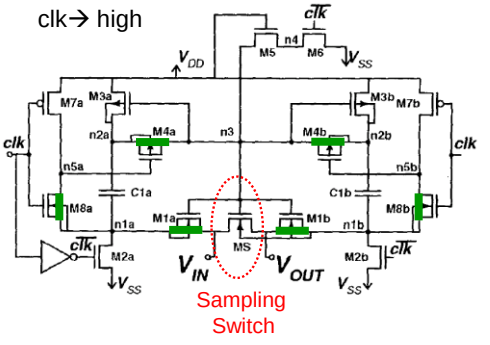
clk→ low



- clk→ low
  - Capacitors C1a & C1b → charged to VDD
  - MS → off
  - Hold mode

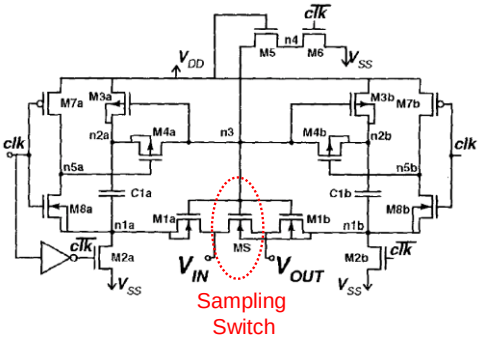
Advanced Clock Boosting Technique

clk→ high



- clk→ high
  - Top plate of C1a & C1b connected to gate of sampling switch
  - Bottom plate of C1a connected to V_{IN}
  - Bottom plate of C1b connected to V_{OUT}
  - VGS & VGD of sampling switch (MS) both @ VDD & ac signal on G of MS → average of V_{IN} & V_{OUT}

Advanced Clock Boosting Technique



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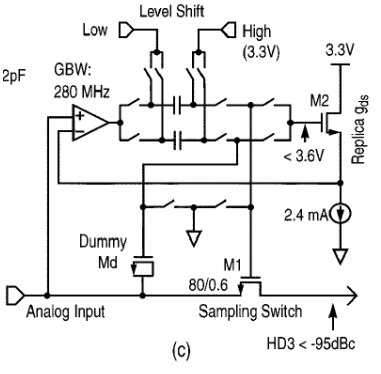
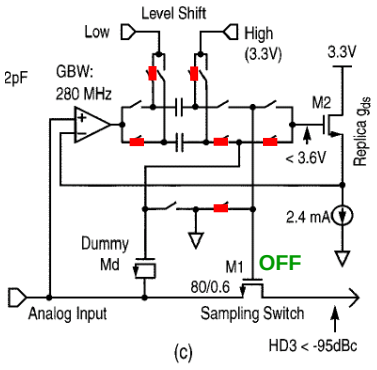
- Gate tracks *average* of input and output, reduces effect of I·R drop at high frequencies
- Bulk also tracks signal ⇒ reduced body effect (technology used allows connecting bulk to S)
- Reported measured SFDR = 76.5dB at f_{in}=200MHz

Constant Conductance Switch



Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Constant Conductance Switch



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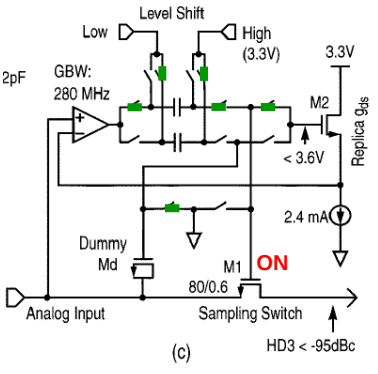
Constant Conductance Switch



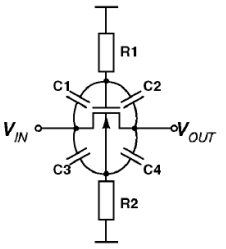
M2→ Constant current

M1→ replica of M2 & same VGS as M2
→ M1 also constant current

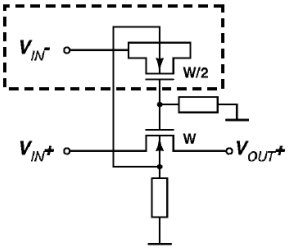
- Note: Authors report requirement of 280MHz GBW for the opamp for 12bit 50Ms/s ADC
- Also, opamp common-mode compliance for full input range required

Ref: H. Pan et al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, pp. 1769-1780, Dec. 2000

Switch Off-Mode Feedthrough Cancellation



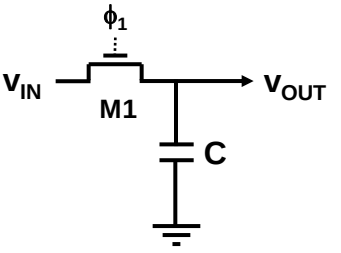
High-pass feedthrough paths past an open switch



Feedthrough cancellation with a dummy switch

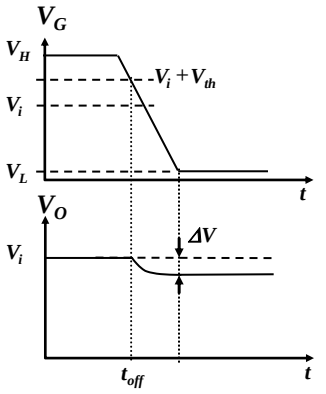
Ref: M. Waltari et al., "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend," ISSCC 2002, Dig. Techn. Papers, pp. 314

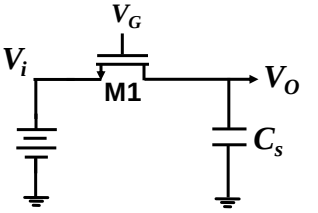
Practical Sampling Issues



- Switch induced noise due to M1 finite channel resistance
- Clock jitter
- Finite R_{sw} → limited bandwidth → finite acquisition time
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection & clock feedthrough

Sampling Switch Charge Injection & Clock Feedthrough Switching from Track to Hold

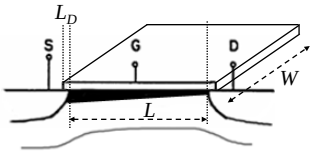




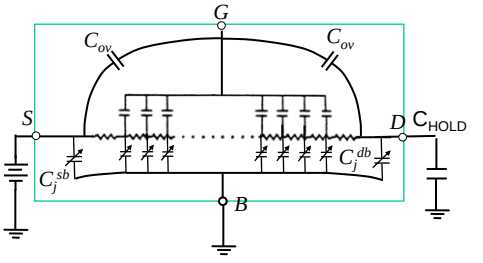
- First assume V_i is a DC voltage
- When switch turns off → unwanted offset voltage induced on C_s
- Why ?

Sampling Switch Charge Injection

MOS xtor operating in triode region
Cross section view

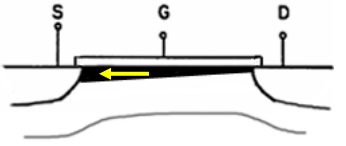


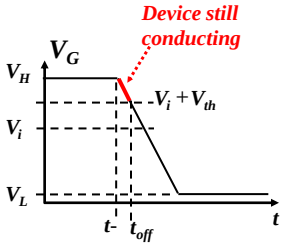
Distributed channel resistance & gate & junction capacitances



- Channel → distributed RC network formed between G,S, and D
- Channel to substrate junction capacitance → distributed & voltage dependant
- Drain/Source junction capacitors to substrate → voltage dependant
- Over-lap capacitance $C_{ov} = L_D.W.C_{ox}'$ associated with G-S & G-D overlap

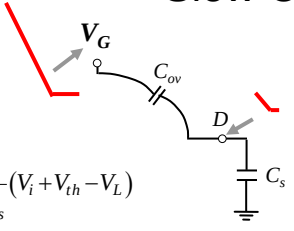
Switch Charge Injection
Slow Clock

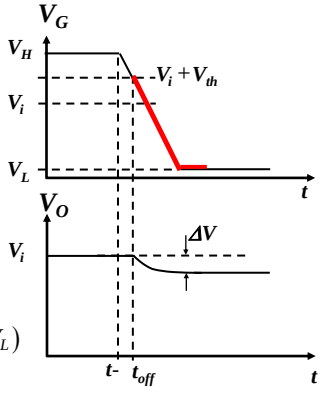




- Slow clock→ clock fall time >> device speed
  → During the period (t- to t_{off}) current in channel discharges channel charge into low impedance signal source
- Only source of error → Clock feedthrough from C_{ov} to C_s

Switch Clock Feedthrough
Slow Clock





$$\Delta V = -\frac{C_{ov}}{C_{ov}+C_s}(V_i + V_{th} - V_L)$$

$$\approx -\frac{C_{ov}}{C_s}(V_i + V_{th} - V_L)$$

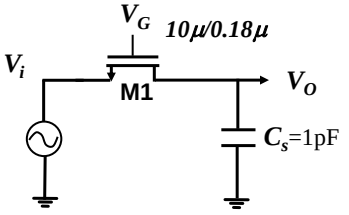
$$V_o = V_i + \Delta V$$

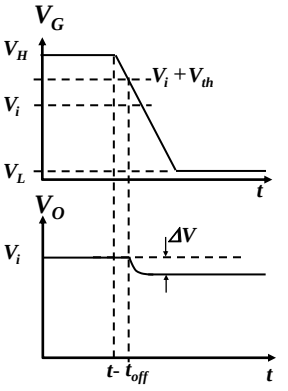
$$V_o = V_i - \frac{C_{ov}}{C_s}(V_i + V_{th} - V_L) = V_i\left(1 - \frac{C_{ov}}{C_s}\right) - \frac{C_{ov}}{C_s}(V_{th} - V_L)$$

$$V_o = V_i(1+\varepsilon) + V_{os}$$

$$where\ \varepsilon = -\frac{C_{ov}}{C_s};\ V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L)$$

Switch Charge Injection & Clock Feedthrough Slow Clock- Example





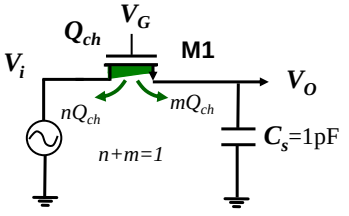
$C'_{ov} = 0.1fF/\mu \quad C_{ox} = 9fF/\mu^2 \quad V_{th} = 0.4V \quad V_L = 0$

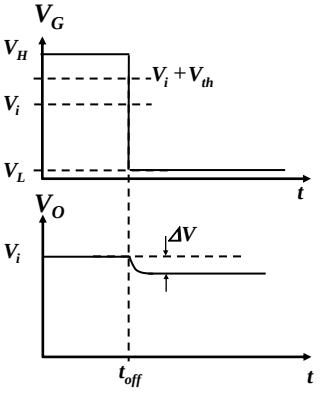
$$\varepsilon = -\frac{C_{ov}}{C_s} = -\frac{10\mu x 0.1fF/\mu}{1pF} = -.1\%$$

$Allowing\ \varepsilon = 1/2LSB \rightarrow ADC\ resolution <\sim 9bit$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_{th} - V_L) = -0.4mV$$

Switch Charge Injection & Clock Feedthrough Fast Clock





- Sudden gate voltage drop → no gate voltage to establish current in channel → channel charge has no choice but to escape out towards S & D

Switch Charge Injection & Clock Feedthrough Fast Clock

Clock Fall-Time << Device Speed:

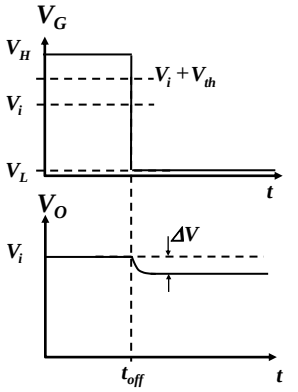
$$\Delta V_o = -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{Q_{ch}}{C_s}$$

$$\approx -\frac{C_{ov}}{C_{ov}+C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L\left((V_H - V_i - V_{th})\right)}{C_s}$$

$$V_o = V_i(1+\varepsilon) + V_{os}$$

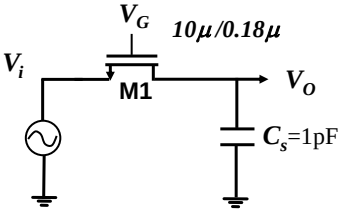
$$where\ \varepsilon = \frac{1}{2}\times\frac{WC_{ox}L}{C_s}$$

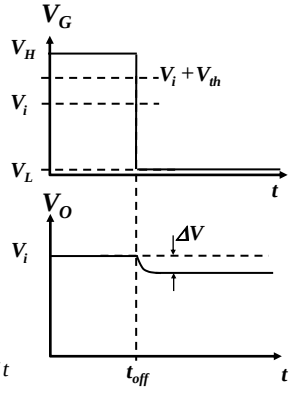
$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L(V_H - V_{th})}{C_s}$$



- For simplicity it is assumed channel charge divided equally between S & D
- Source of error → channel charge transfer + clock feedthrough via C_{ov} to C_s

Switch Charge Injection & Clock Feedthrough Fast Clock- Example



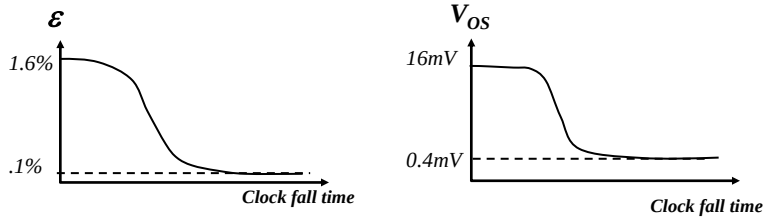


$$C_{ov} = 0.1\frac{fF}{\mu},\ C_{ox} = 9\frac{fF}{\mu^2},\ V_{th} = 0.4V, V_{DD} = 1.8V,\ V_L = 0$$

$$\varepsilon = 1/2\frac{WLC_{ox}}{C_s} = \frac{10\mu x 0.18\mu x 9fF/\mu^2}{1pF} = 1.6\% \rightarrow \sim 5-bit$$

$$V_{os} = -\frac{C_{ov}}{C_s}(V_H - V_L) - \frac{1}{2}\times\frac{WC_{ox}L(V_H - V_{th})}{C_s} = -1.8mV - 14.6mV = -16.4mV$$

Switch Charge Injection & Clock Feedthrough Example-Summary



Error function of:

- → Clock fall time
- → Input voltage level
- → Source impedance
- → Sampling capacitance size
- → Switch size
  - Clock fall/rise should be controlled not to be faster (sharper) than necessary

Switch Charge Injection Error Reduction

- How do we reduce the error?
  - → Reduce switch size to reduce channel charge?

$$\Delta V_o = -\frac{1}{2}\frac{Q_{ch}}{C_s} \downarrow$$

$$\tau = R_{ON}C_s = \frac{C_s}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})} \uparrow \qquad (note: \frac{T_s}{2} = k\tau)$$

Consider the figure of merit (FOM):

$$FOM = \frac{1}{\tau \times \Delta V_o} \approx \frac{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})}{C_s} \times 2 \times \frac{C_s}{WC_{ox}L\left((V_H - V_i - V_{th})\right)}$$

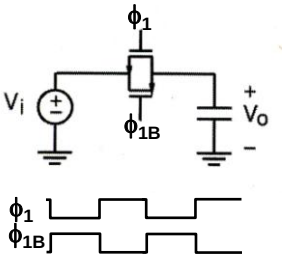
$$\rightarrow FOM \propto \mu / L^2$$

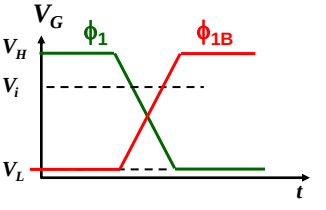
- Reducing switch size increases τ → increased distortion→ not a viable solution
- Small τ and small ΔV → use minimum chanel length (mandated by technology)
- For a given technology τ x ΔV ~ constant

Sampling Switch Charge Injection & Clock Feedthrough Summary

- Extra charge injected onto sampling capacitor @ switch device turn-off
  - Channel charge injection
  - Clock feedthrough to C_s via C_{ov}
- Issues due to charge injection & clock feedthrough:
  - DC offset induced on hold C
  - Input dependant error voltage → distortion
- Solutions:
  - Slowing down clock edges as much as possible
  - Complementary switch?
  - Addition of dummy switches?
  - Bottom-plate sampling?

Switch Charge Injection & Clock Feedthrough Complementary Switch





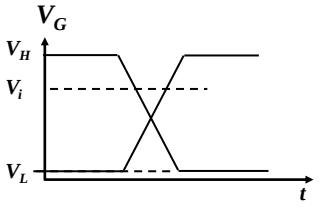
- In slow clock case if area of n & p devices & widths are equal (W_n=W_p)→ effect of overlap capacitor for n & p devices to first order cancel (cancellation accuracy depends on matching of n & p width and overlap length L_D)
- Since in CMOS technologies μ_n~2.5μ_p choice of W_n=W_p not optimal from linearity perspective (W_p>W_n preferable)

Switch Charge Injection
Complementary Switch
Fast Clock

$$|Q_{ch-n}| = W_n C_{ox} L_n \left(V_H - V_i - |V_{th-n}|\right)$$

$$|Q_{ch-p}| = W_p C_{ox} L_p \left(V_i - V_L - |V_{th-p}|\right)$$

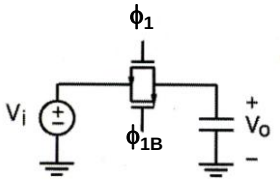
$$\Delta V_o \approx -\frac{1}{2}\left(\frac{|Q_{ch-n}|}{C_s} - \frac{|Q_{ch-p}|}{C_s}\right)$$



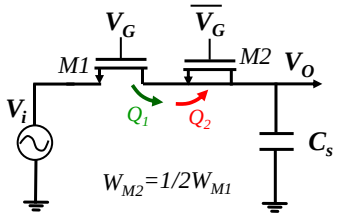
$$V_o = V_i(1+\varepsilon) + V_{os}$$

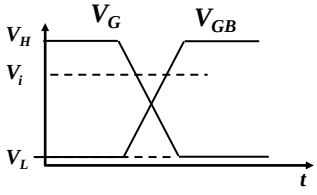
$$\varepsilon \approx \frac{1}{2} \times \frac{W_n C_{ox} L_n + W_p C_{ox} L_p}{C_s}$$

- In fast clock case
  - To 1st order, offset due to overlap caps cancelled for equal device width
  - Input voltage dependant error worse!



Switch Charge Injection
Dummy Switch



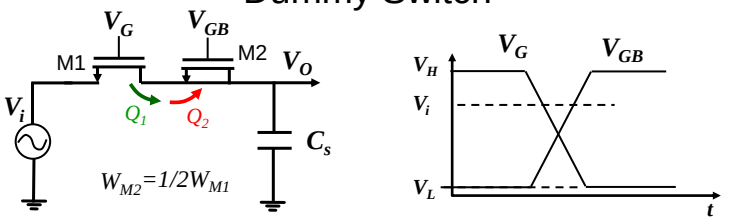


$$Q_1 \approx \frac{1}{2} Q_{ch}^{M1} + Q_{ov}^{M1}$$

$$Q_2 \approx Q_{ch}^{M2} + 2Q_{ov}^{M2}$$

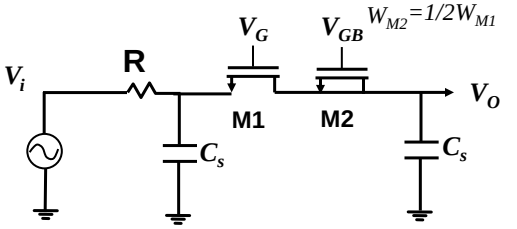
$$For\ W_{M2} = \frac{1}{2} W_{M1} \rightarrow Q_2 = -Q_1 \quad \& \quad Q_{ov}^{M1} = 2Q_{ov}^{M2}$$

Switch Charge Injection
Dummy Switch



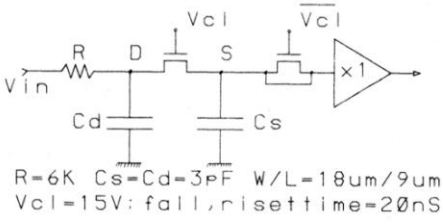
- Dummy switch same L as main switch but half W
- Main device clock goes low, dummy device gate goes high → dummy switch acquires same amount of channel charge main switch needs to lose
- Effective only if exactly half of the charge stored in M1 is transferred to M2 (depends on input/output node impedance) and requires good matching between clock fall/rise

Switch Charge Injection
Dummy Switch



- To guarantee half of charge goes to each side→ create the same environment on both sides
  - ❖ Add capacitor equal to sampling capacitor to the other side of the switch + add fixed resistor to emulate input resistance of following circuit
    → Issues: Degrades sampling bandwidth

Dummy Switch Effectiveness Test

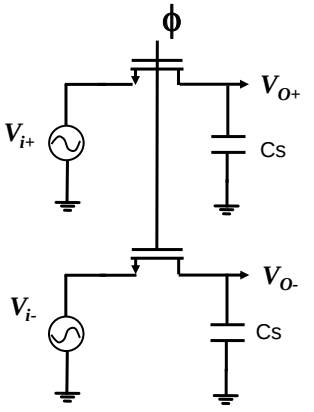


Vin	UNCOMPENSATED SWITCH	COMPENSATED WITH DUMMY	BALANCED SWITCH
0v	-160mV	-45mV	6mV
5v	-105mV	-30mV	1mV
10v	-40mV	-11mV	0.5mV

- Dummy switch → W=1/2W$_{main}$
- As Vin is increased Vc1-Vin is decreased → channel charge decreased→ less charge injection
- Note large Ls →good device area matching

Ref: L. A. Bienstman et al, " An Eight-Channel 8 13it Microprocessor Compatible NMOS D/A Converter with Programmable Scaling", IEEE JSSC, VOL. SC-15, NO. 6, DECEMBER 1980

Switch Charge Injection Differential Sampling



$$V_{o+}-V_{o-}=V_{od} \qquad V_{i+}-V_{i-}=V_{id}$$

$$V_{oc}=\frac{V_{o+}+V_{o-}}{2} \qquad V_{ic}=\frac{V_{i+}+V_{i-}}{2}$$

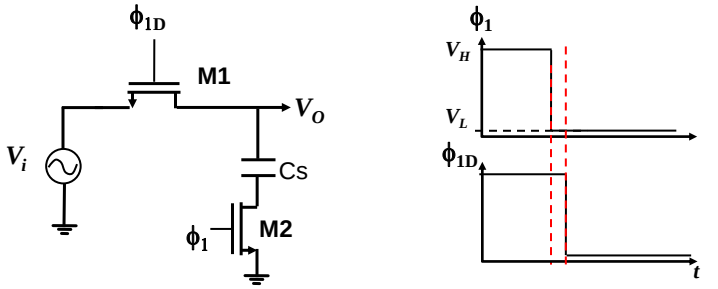
$$V_{o+}=V_{i+}(1+\varepsilon_1)+V_{os1}$$

$$V_{o-}=V_{i-}(1+\varepsilon_2)+V_{os2}$$

$$V_{od}=V_{id}+V_{id}\left(\varepsilon_1+\varepsilon_2\right)/2+(\varepsilon_1-\varepsilon_2)V_{ic}+V_{os1}-V_{os2}$$

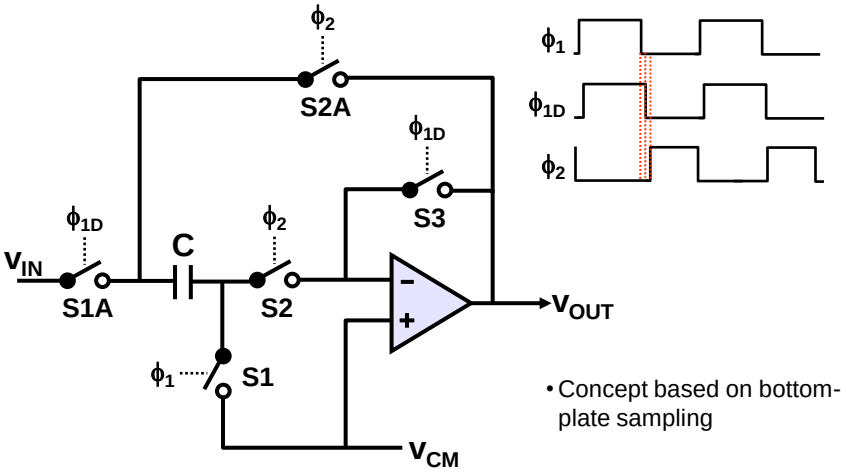
- To 1st order, offset terms cancel
- Note gain error ε still about the same
- Has the advantage of better immunity to noise coupling and cancellation of even order harmonics

Avoiding Switch Charge Injection
Bottom Plate Sampling



- Switches M2 opened slightly earlier compared to M1
  → Injected charge due to turning off M2 is constant since its GS voltage is constant & eliminated when used differentially
- Since C_s bottom plate is already open when M1 is switched off:
  → No signal dependant charge injected on C_s

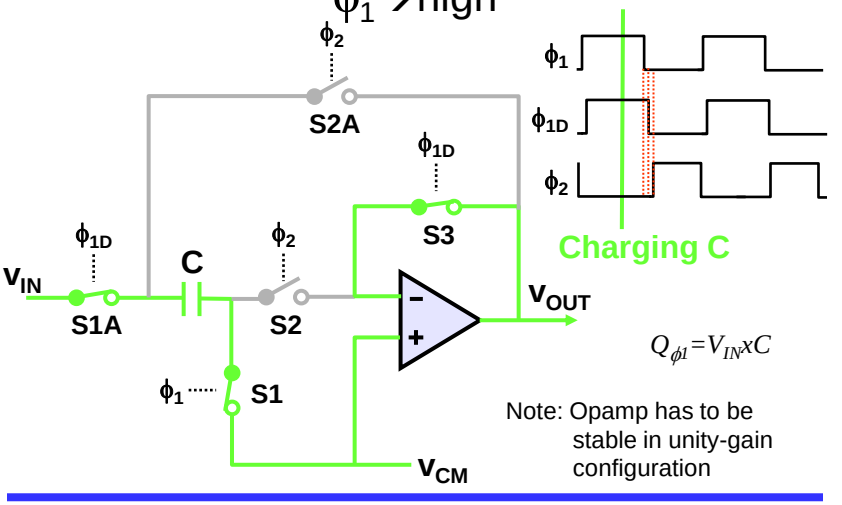
Flip-Around Track & Hold



- Concept based on bottom-plate sampling

Flip-Around T/H-Basic Operation

$\phi_1 \rightarrow$ high

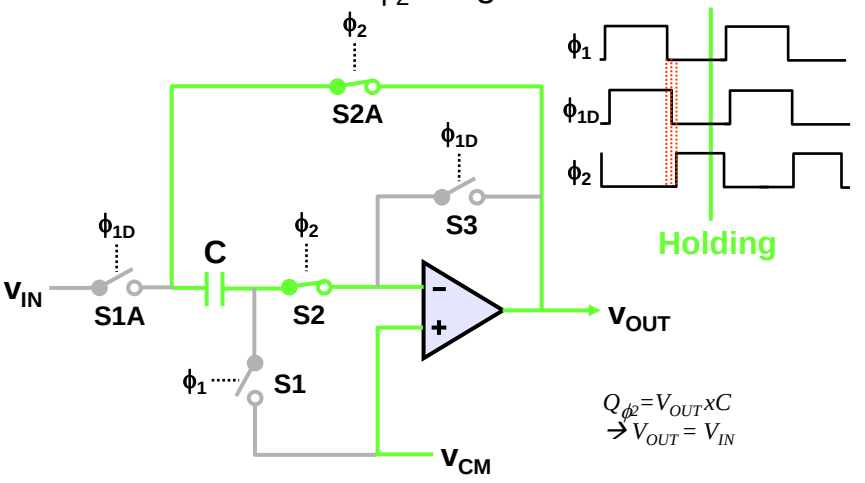


$Q_{\phi 1} = V_{IN} x C$

Note: Opamp has to be stable in unity-gain configuration

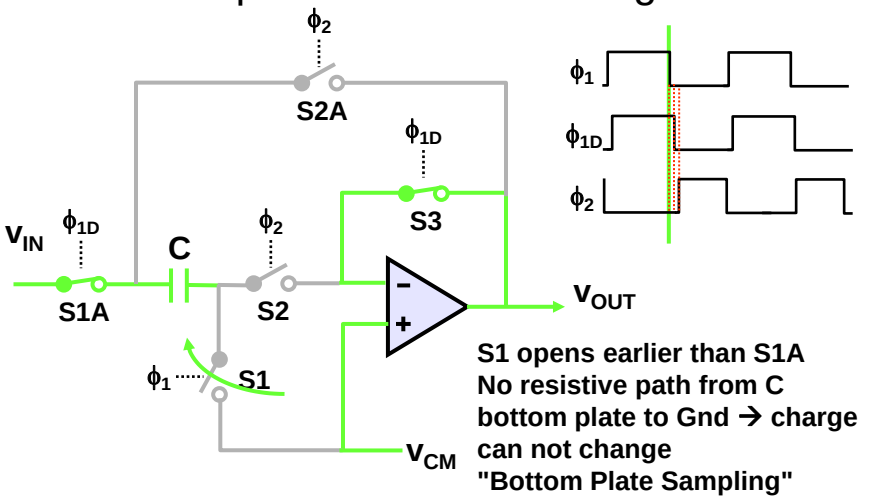
Flip-Around T/H-Basic Operation

$\phi_2 \rightarrow$ high



$Q_{\phi 2} = V_{OUT} x C$
$\rightarrow V_{OUT} = V_{IN}$

Flip-Around T/H - Timing

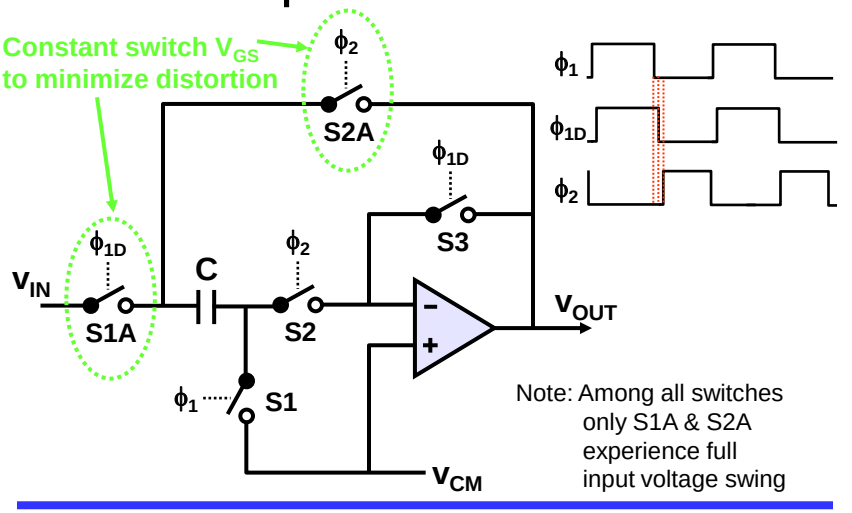


S1 opens earlier than S1A
No resistive path from C bottom plate to Gnd → charge can not change
"Bottom Plate Sampling"

Charge Injection

- At the instant of transitioning from track to hold mode, some of the charge stored in sampling switch S1 is dumped onto C
- With "Bottom Plate Sampling", only charge injection component due to opening of S1 and is to first-order independent of v_{IN}
  - Only a dc offset is added. This dc offset can be removed with a differential architecture

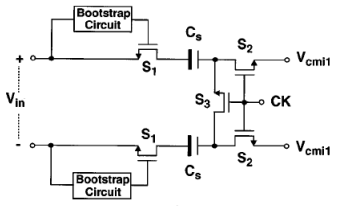
Flip-Around T/H



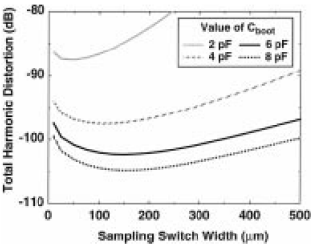
Flip-Around T/H

- S1 is chosen to be an n-channel MOSFET
- Since it always switches the same voltage, it's on-resistance, R_{S1}, is signal-independent (to first order)
- Choosing $R_{S1} >> R_{S1A}$ minimizes the non-linear component of $R = R_{S1A} + R_{S1}$
  - Typically, S1A is a wide (much lower resistance than S1) & constant V_{GS} switch
  - In practice size of S1A is limited by the (nonlinear) S/D capacitance that also adds distortion
  - If S1A's resistance is negligible → delay depends only on S1 resistance
  - S1 resistance is independent of V_{IN} → error due to finite time-constant → independent of V_{IN}

Differential Flip-Around T/H
Choice of Sampling Switch Size



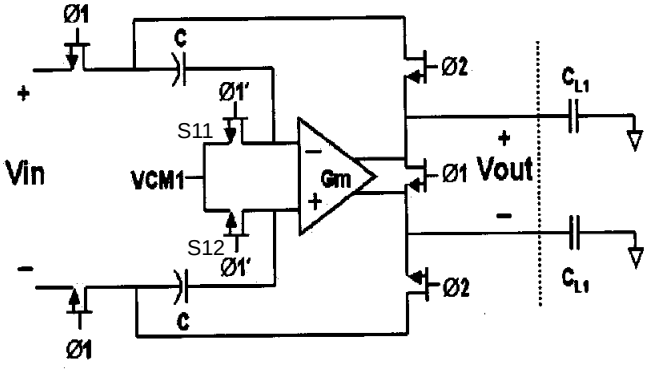
C_S=7pF



- THD simulated w/o sampling switch boosted clock → -45dB
- THD simulated with sampling switch boosted clock (see graph)

Ref: K. Vleugels et al, "A 2.5-V Sigma–Delta Modulator for Broadband Communications Applications " IEEE JSSC, VOL. 36, NO. 12, DECEMBER 2001, pp. 1887

Differential Flip-Around T/H

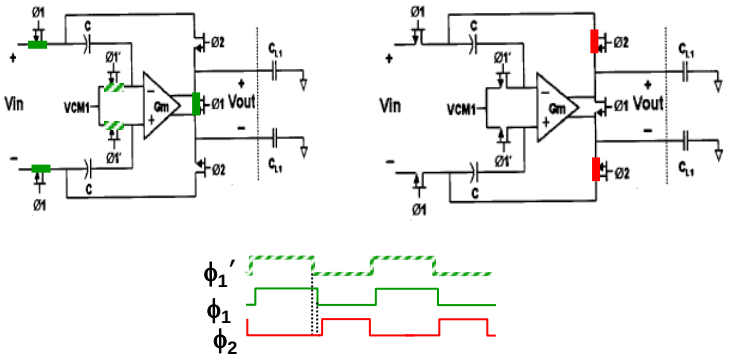


Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit

During input sampling phase→ amp outputs shorted together

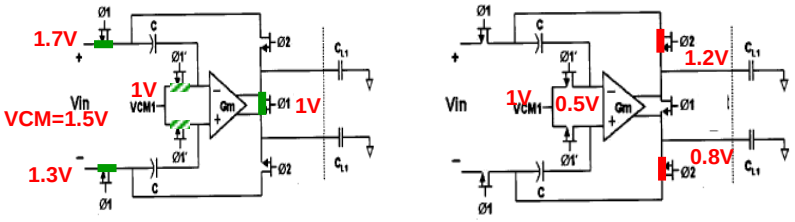
Ref: W. Yang, *et al.* "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001 1931

Differential Flip-Around T/H



- Gain=1
- Feedback factor=1 → high operating speed

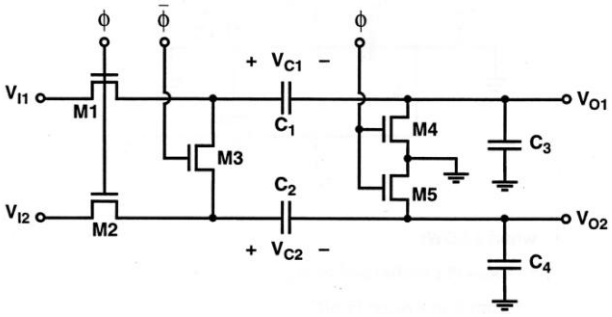
Differential Flip-Around T/H
Issues: Input Common-Mode Range



$\Delta V_{in\text{-}cm}$=1-1.5= - 0.5V

- $\Delta V_{in\text{-}cm}=V_{out\_com}-V_{sig\_com}$
  → Drawback: Amplifier needs to have large input common-mode compliance

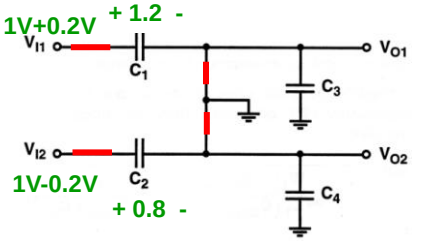
Input Common-Mode Cancellation

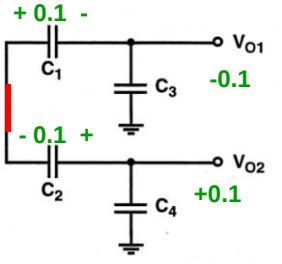


- Note: Shorting switch M3 added

Ref: R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008

Input Common-Mode Cancellation





Track mode (ϕ high)
$V_{C1}=V_{I1}$, $V_{C2}=V_{I2}$
$V_{o1}=V_{o2}=0$

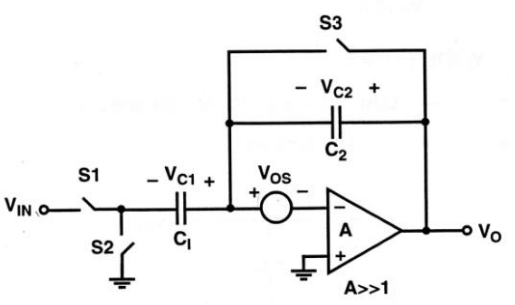
Hold mode (ϕ low)
$V_{o1}+V_{o2}=0$
$V_{o1}-V_{o2}= -(V_{I1}-V_{I2})(C_1/(C_1+C_3))$

→ Input common-mode level removed

Switched-Capacitor Techniques Combining Track & Hold with Other Functions

- T/H + Charge redistribution amplifier
- T/H & Input difference amplifier
- T/H & summing amplifier
- Differential T/H combined with gain stage
- Differential T/H including offset cancellation

T/H + Charge Redistribution Amplifier



Track mode: (S1, S3 → on S2 → off)

$V_{C1}=V_{os}-V_{IN}$, $V_{C2}=0$

$V_o=V_{os}$

T/H + Charge Redistribution Amplifier Hold Mode

S1 & S3 open
S2 closed

$V_{C1} \longrightarrow V_{os}$

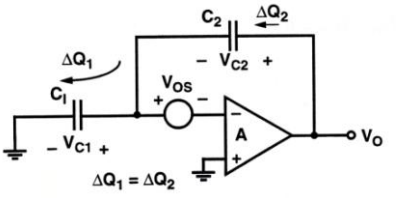
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$

$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$

$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C1} = V_{C2}$$

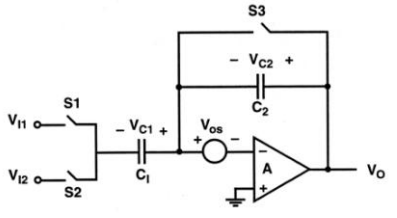
$$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$$

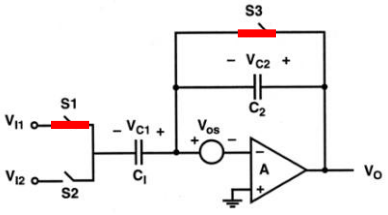


Hold/amplify mode (S1, S3 →off S2→ on)

→ Offset NOT cancelled, but not amplified
→ Input-referred offset =(C_2/C_1) x V_{OS}, & often C_2<C_1

T/H & Input Difference Amplifier

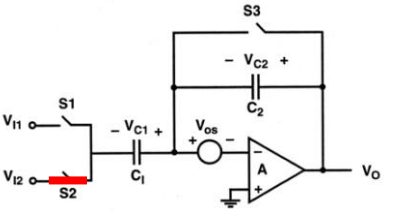




Sample mode:
(S1, S3 →on S2→ off)
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$

Input Difference Amplifier Cont'd

Subtract/Amplify mode (S1, S3 →off S2→ on)
During previous phase:
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$



$$V_{C1} = V_{os} - V_{I2}$$

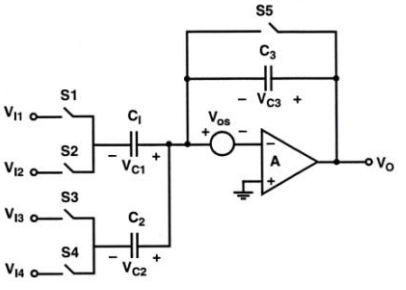
$$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

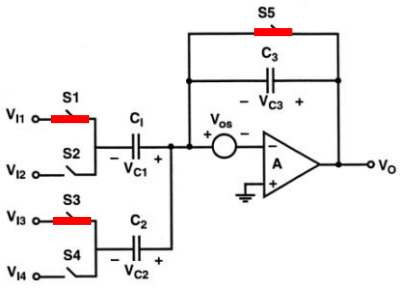
$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

→Offset NOT cancelled, but not amplified
→Input-referred offset =$(C_2/C_1)xV_{OS}$, & $C_2<C_1$

T/H & Summing Amplifier



T/H & Summing Amplifier Cont'd



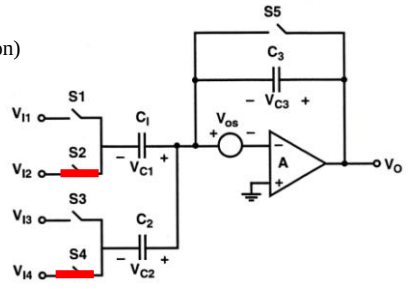
Sample mode (S1, S3, S5→on S2, S4→ off)

$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=V_{os}-V_{I3}$, $V_{C3}=0$

$V_o=V_{os}$

T/H & Summing Amplifier Cont'd

Amplify mode (S1, S3, S5→off, S2, S4→ on)



$$V_{C1}=V_{os}-V_{I2} \Rightarrow \Delta V_{C1}=V_{I1}-V_{I2}$$

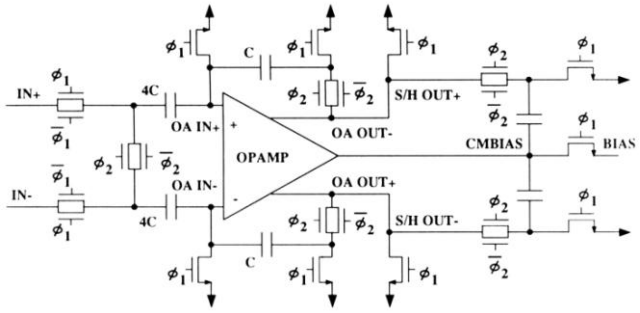
$$V_{C2}=V_{os}-V_{I4} \Rightarrow \Delta V_{C2}=V_{I3}-V_{I4}$$

$$\Delta Q_3=\Delta Q_1+\Delta Q_2=C_1\Delta V_{C1}+C_2\Delta V_{C2}$$

$$\Delta V_{C3}=\frac{\Delta Q_3}{C_3}=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})$$

$$V_O=\left(\frac{C_1}{C_3}\right)(V_{I1}-V_{I2})+\left(\frac{C_2}{C_3}\right)(V_{I3}-V_{I4})+V_{os}$$

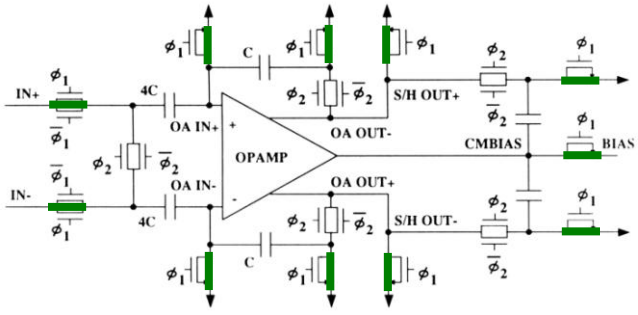
Differential T/H Combined with Gain Stage



Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp

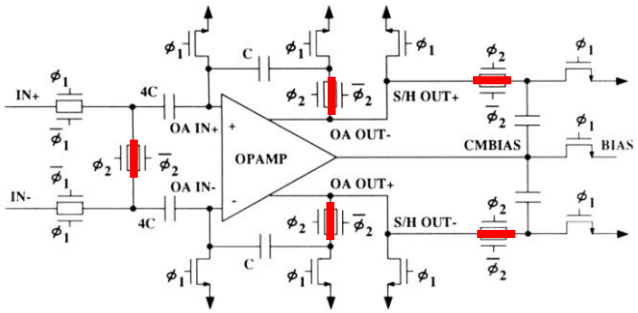
Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Combined with Gain Stage
$\phi 1 \rightarrow$ High



Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Combined with Gain Stage



- *Gain=4C/C=4*
- Input voltage common-mode level removed → opamp can have low input common-mode compliance
- Amplifier offset NOT removed

Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987