EE247
Lecture 18

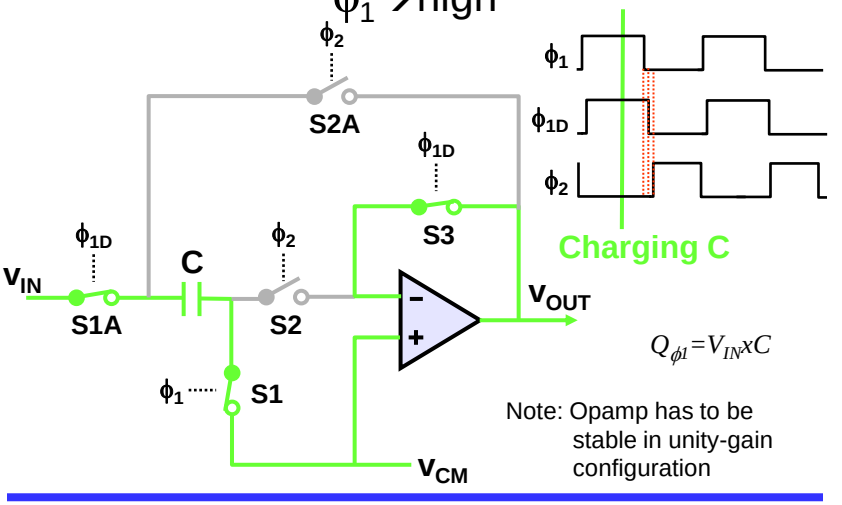
ADC Converters
- Track & hold
  - T/H circuits
  - T/H combined with summing/difference function
  - T/H circuit incorporating gain & offset cancellation
  - T/H aperture uncertainty
- ADC architectures and design
  - Serial- slope type
  - Successive approximation
  - Flash ADC and its sources of error: comparator offset, sparkle code & meta-stability
- Comparator design
  - Single-stage open-loop amplifier
  - Cascade of open-loop amplifiers

Summary of Last Lecture

ADC Converters
- Sampling (continued)
  - Sampling switch considerations
    - Clock voltage boosters
  - Sampling switch charge injection & clock feedthrough
    - Complementary switch
    - Use of dummy device
    - Bottom-plate switching
- Track & hold
  - Flip around T/H

Flip-Around T/H-Basic Operation

$\phi_1 \rightarrow$ high

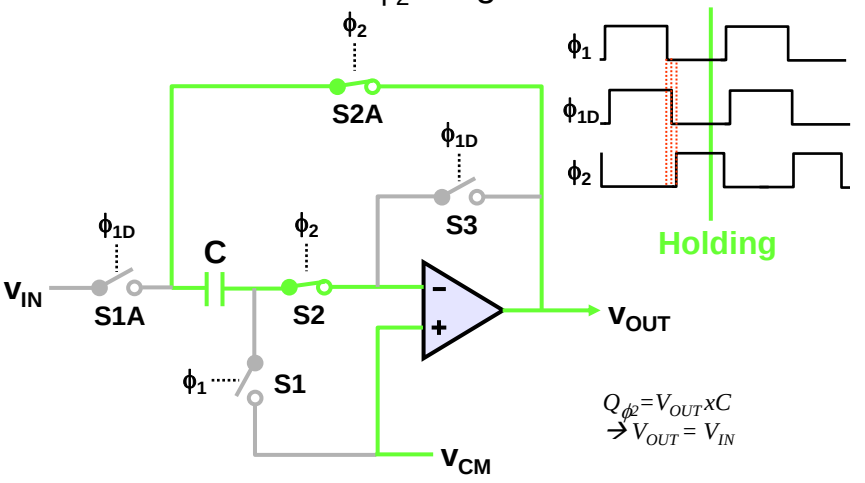


$Q_{\phi 1} = V_{IN} x C$

Note: Opamp has to be stable in unity-gain configuration

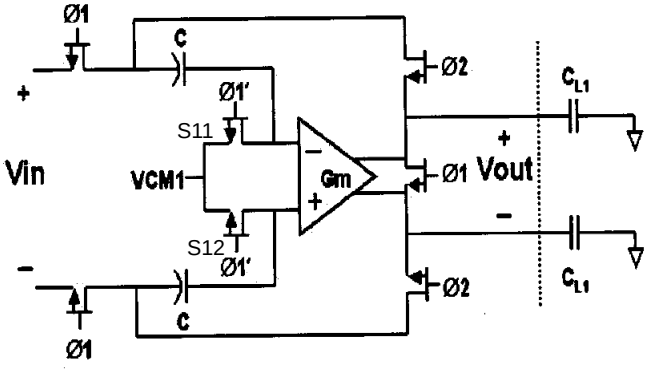
Flip-Around T/H-Basic Operation

$\phi_2 \rightarrow$ high



$Q_{\phi 2} = V_{OUT} x C$
$\rightarrow V_{OUT} = V_{IN}$

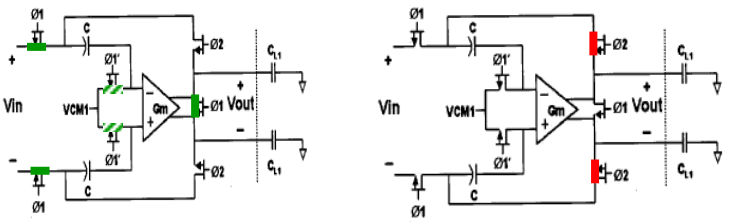
Differential Flip-Around T/H

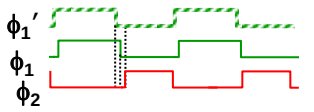


Offset voltage associated with charge injection of S11 & S12 cancelled by differential nature of the circuit

Ref: W. Yang, *et al.* "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001 1931

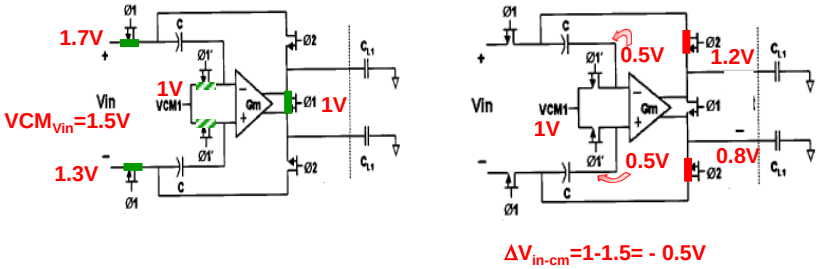
Differential Flip-Around T/H





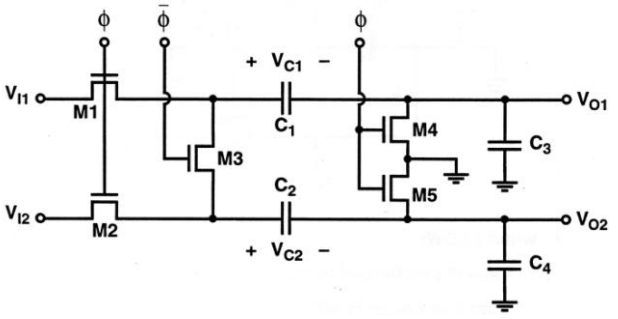
- Gain=1
- Issue: Large input common-mode compliance required

Differential Flip-Around T/H
Issues: Large Input Common-Mode Compliance



- $\Delta V_{in\text{-}cm}=V_{out\_com}-V_{sig\_com}$
  → Drawback: Amplifier needs to have large input common-mode compliance

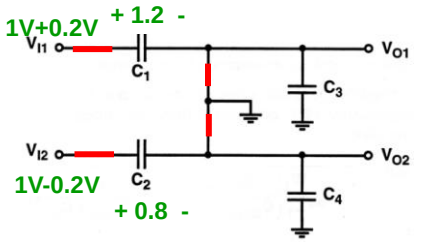
Input Common-Mode Cancellation



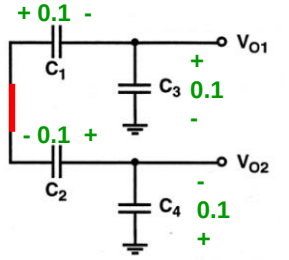
- Note: Shorting switch M3 added

Ref: R. Yen, *et al.* "A MOS Switched-Capacitor Instrumentation Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-17, NO. 6,, DECEMBER 1982 1008

Input Common-Mode Cancellation



Track mode (ϕ high)
$V_{C1}=V_{I1}$, $V_{C2}=V_{I2}$
$V_{o1}=V_{o2}=0$



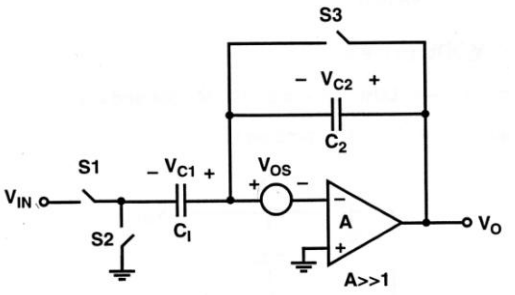
Hold mode (ϕ low)
$V_{o1}+V_{o2}=0$
$V_{o1}-V_{o2}= -(V_{I1}-V_{I2})(C_1/(C_1+C_3))$

→Input common-mode level removed
• Will introduce active version in page 18

Switched-Capacitor Techniques Combining Track & Hold with Various other Functions

- T/H + Charge redistribution amplifier
- T/H & Input difference amplifier
- T/H & summing amplifier
- Differential T/H combined with gain stage
- Differential T/H including offset cancellation

T/H + Charge Redistribution Amplifier



Track mode: (S1, S3 →on S2→ off)

$V_{C1}=V_{os}-V_{IN}$, $V_{C2}=0$

$V_o=V_{os}$

T/H + Charge Redistribution Amplifier Hold Mode

$V_{C1} \longrightarrow V_{os}$

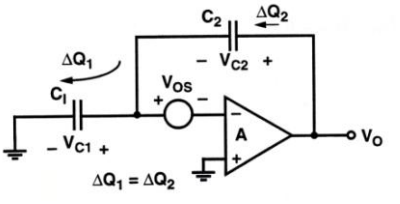
$\Delta V_{C1} = V_{os} - (V_{os} - V_{IN}) = V_{IN}$

$\Delta Q_1 = C_1 \Delta V_{C1} = C_1 V_{IN}$

$\Delta Q_2 = C_2 \Delta V_{C2} = \Delta Q_1$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right) V_{C1} = V_{C2}$$

$$V_O = V_{C2} + V_{os} = \left(\frac{C_1}{C_2}\right) V_{IN} + V_{os}$$



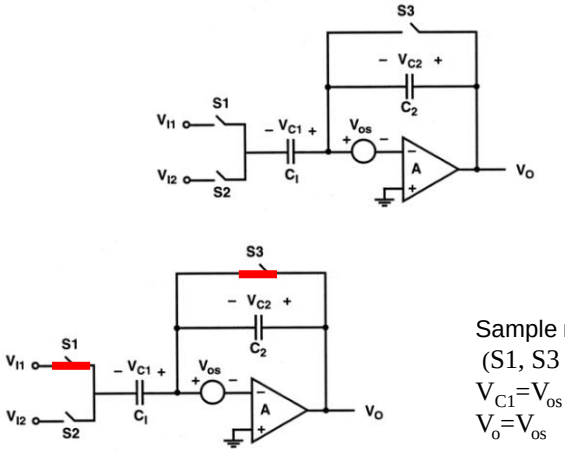
Hold/amplify mode (S1, S3 →off S2→ on)

→ Offset NOT cancelled, but not amplified

→ Input-referred offset =(C_2/C_1) x V_{OS}, & often $C_2<C_1$

→ Can incorporate gain by having $C_1>C_2$

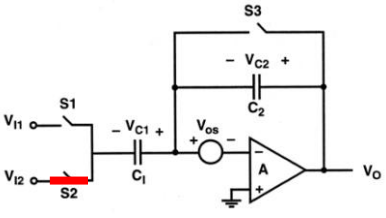
T/H & Input Difference Amplifier



Sample mode:
(S1, S3 →on S2→ off)
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$

Input Difference Amplifier Cont'd

Subtract/Amplify mode (S1, S3 →off S2→ on)
During previous phase:
$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=0$
$V_o=V_{os}$



$$V_{C1} = V_{os} - V_{I2}$$

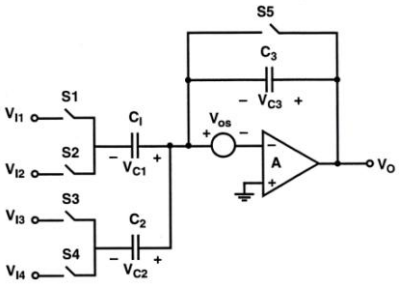
$$\Delta V_{C1} = (V_{os} - V_{I2}) - (V_{os} - V_{I1}) = V_{I1} - V_{I2}$$

$$\Delta V_{C2} = \left(\frac{C_1}{C_2}\right)\Delta V_{C1} = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2})$$

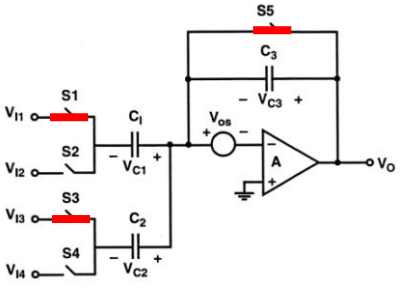
$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$

→Offset NOT cancelled, but not amplified
→Input-referred offset =$(C_2/C_1)xV_{OS}$, & $C_2<C_1$

T/H & Summing Amplifier



T/H & Summing Amplifier Cont'd



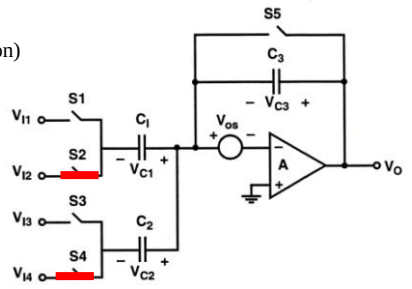
Sample mode (S1, S3, S5→on S2, S4→ off)

$V_{C1}=V_{os}-V_{I1}$, $V_{C2}=V_{os}-V_{I3}$, $V_{C3}=0$

$V_o=V_{os}$

T/H & Summing Amplifier Cont'd

Amplify mode (S1, S3, S5→off, S2, S4→ on)



$$V_{C1} = V_{os} - V_{I2} \Rightarrow \Delta V_{C1} = V_{I1} - V_{I2}$$

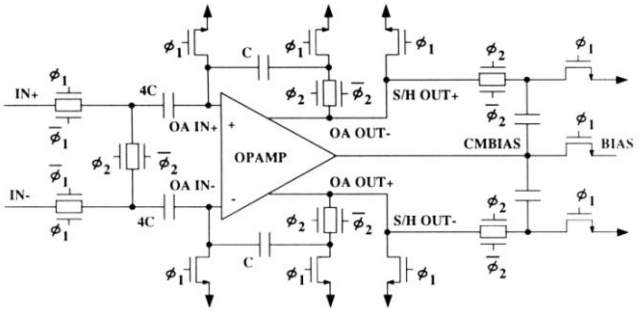
$$V_{C2} = V_{os} - V_{I4} \Rightarrow \Delta V_{C2} = V_{I3} - V_{I4}$$

$$\Delta Q_3 = \Delta Q_1 + \Delta Q_2 = C_1 \Delta V_{C1} + C_2 \Delta V_{C2}$$

$$\Delta V_{C3} = \frac{\Delta Q_3}{C_3} = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4})$$

$$V_O = \left(\frac{C_1}{C_3}\right)(V_{I1} - V_{I2}) + \left(\frac{C_2}{C_3}\right)(V_{I3} - V_{I4}) + V_{os}$$

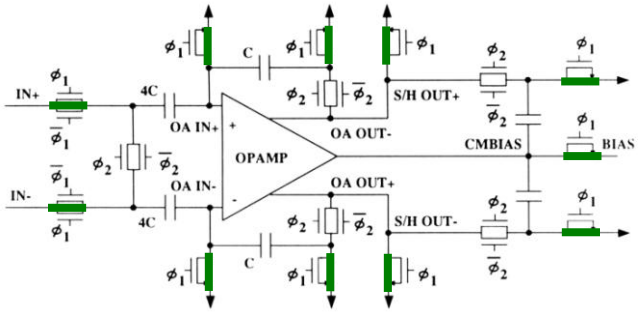
Differential T/H Combined with Gain Stage



Employs the previously discussed technique to eliminate the problem associated with high common-mode voltage excursion at the input of the opamp

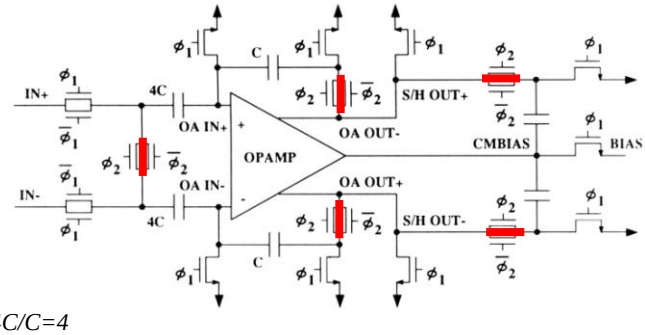
Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Combined with Gain Stage
$\phi 1 \rightarrow$ High



Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

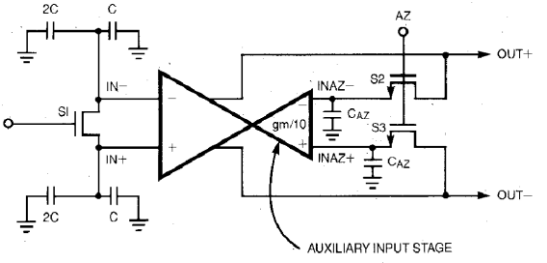
Differential T/H Combined with Gain Stage



- *Gain=4C/C=4*
- Input voltage common-mode level removed → opamp can have low input common-mode compliance
- Amplifier offset NOT removed

Ref: S. H. Lewis, et al., "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter" IEEE JSSC, VOL. SC-22,NO. 6, DECEMBER 1987

Differential T/H Including Offset Cancellation



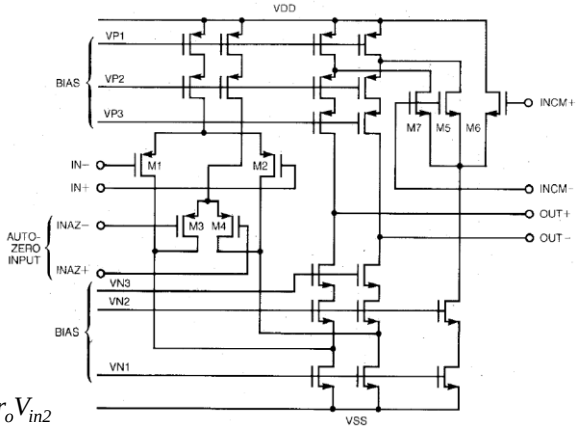
- Operation during offset cancellation phase shown
- Auxiliary inputs added with A_{main}/A_{aux}.=10
- During offset cancellation phase:
  - Aux. amp configured in unity-gain mode: → offset stored on C_{AZ} & canceled during the signal acquisition phase

Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

Differential T/H Including Offset Cancellation Operational Amplifier

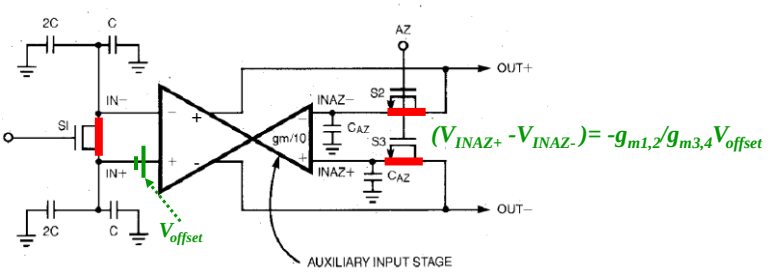
- Operational amplifier → dual input folded-cascode opamp
- M3,4 auxiliary input, M1,2 main input
- To achieve 1/10 gain ratio $W_{M3,4} = 1/10 \times W_{M1,2}$ & current sources are scaled by 1/10
- M5,6,7 → common-mode control
- Output stage → dual cascode → high DC gain

$$V_{out} = g_{m1,2} r_o V_{in1} + g_{m3,4} r_o V_{in2}$$



Ref: H. Ohara, et al., "A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE Journal of Solid-State Circuits,* vol. 22, pp. 930 - 938, December 1987.

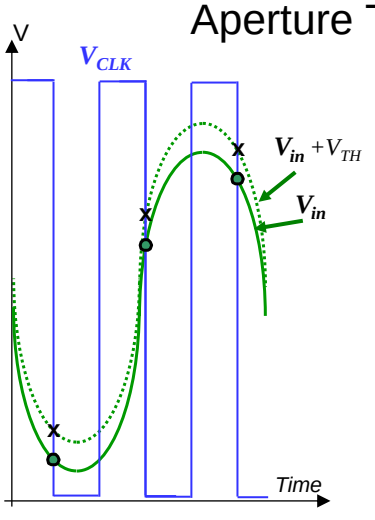
Differential T/H Including Offset Cancellation Phase

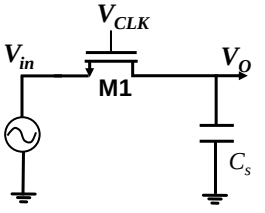


$(V_{INAZ+} - V_{INAZ-}) = -g_{m1,2}/g_{m3,4} V_{offset}$

- During offset cancellation phase AZ and S1 closed → main amplifier offset amplified by g_{m1}/g_{m2} & stored on C_{AZ}
- Auxiliary amp chosen to have lower gain so that:
  - ❑ Aux. amp charge injection associated with opening of switch AZ → reduced by $A_{aux}/A_{main}=1/10$
  - ❑Insignificant increase in power dissipation resulting from addition of aux. inputs
- Requires an extra auto-zero clock phase

Track & Hold Aperture Time Error

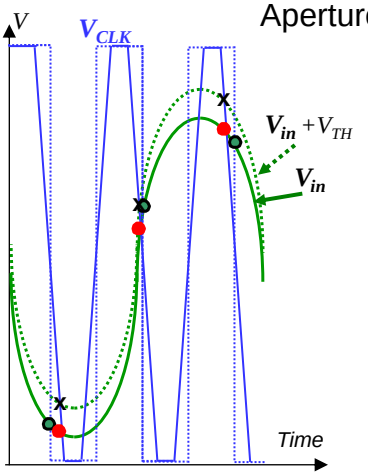




Transition from track to hold:
Occurs when device turns fully off
→ $V_{CLK}=V_{in}+V_{TH}$

Sharp fall-time wrt signal change
→ no aperture error

Track & Hold
Aperture Time Error



Slow falling clock → aperture error

$V_{in}=A\sin(2\pi f_{in}t)$

$\varepsilon = f_{in} x A x \ t_{fall} / V_{CLK}$

$SDR = -20\log\varepsilon - 4$ [dB] (imperical see Ref.)

Example:

Nyquist rate *10-bit ADC* & $A=V_{CLK}/4$

→ *SQNR=62dB*

for distortion due to aperture error < quant noise

→ $t_{fall} < 2x10^{-3}/f_{in}$

→ *Worst case:* $f_{in}=f_s/2$

→ $t_{fall} < 4x10^{-3}/f_s$

→ *e.g.* $f_s=1000MHz$, $t_{fall}<4psec$

Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

Track & Hold
Aperture Time Error

- Aperture error analysis applies to simple sampling network
- Bottom plate sampling → reduced aperture error
- Boosted clock → reduced aperture error

→ Clock edge fall/rise trade-off between switch charge injection versus aperture error

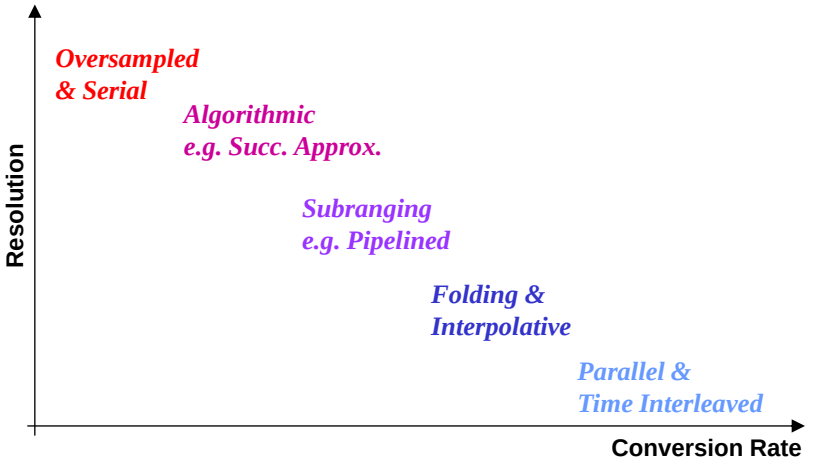
Ref: P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE Journal of Solid-State Circuits,* vol. 26, pp. 643 - 651, April 1991.

ADC
Architecture & Design

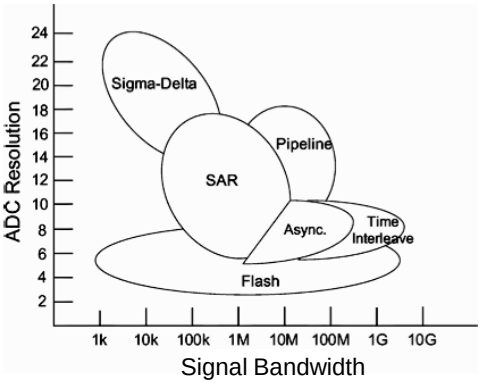
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

Various ADC Architectures
Resolution/Conversion Rate

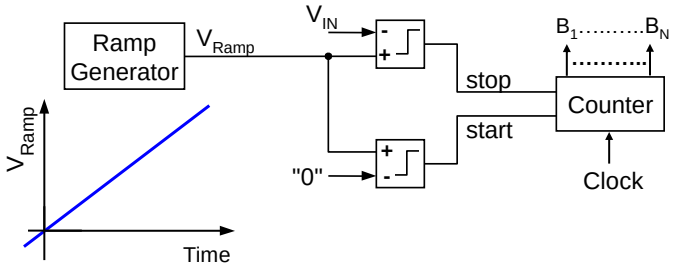


Resolution versus Signal Bandwidth



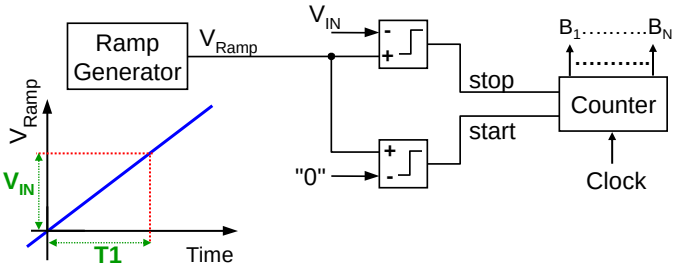
Ref: S. Chen, R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-µm CMOS: *IEEE J. of Solid-State Circuits*, Vol. 41, No. 12, December 2006.

Serial ADC
Single Slope



- Counter starts counting @ V_{Ramp}=0
- Counter stops counting for V_{IN}=V_{Ramp}

Serial ADC
Single Slope

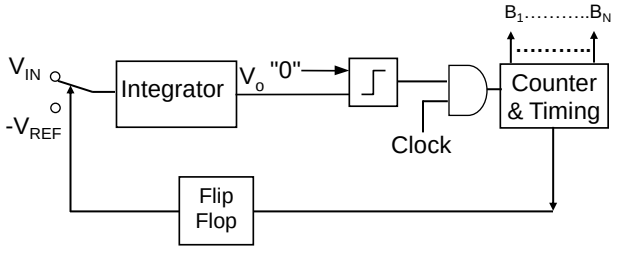


- Note that T1 is proportional to V_{IN}
- Counter output proportional to T1=nT_{clock}
  → Counter output proportional to V_{IN}
  → 2^NxT_{clock}= V_{FS}

Single Slope ADC

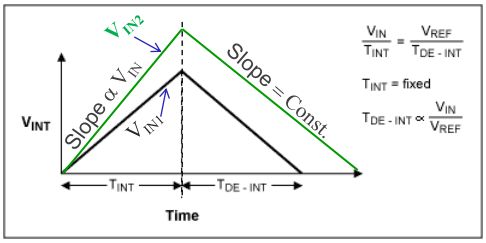
- Advantages:
  - Low complexity & simple
  - INL depends on ramp linearity & not component matching
  - Inherently monotonic
- Disadvantages:
  - Slow (2^N clock pulses for N-bit conversion) (e.g. N=16 f_{clock}=1MHz → needs 65000x1μs=65ms/conversion)
  - Hard to generate precise ramp required for high resolution ADCs
  - Need to calibrate ramp slope versus V_{IN}
- Better: Dual Slope, Multi-Slope

Serial ADC
Dual Slope



- First: V_{IN} is integrated for a fixed time ($2^N x T_{CLK}$)
  → $V_o = 2^N x T_{CLK}\ V_{IN}/\tau_{intg}$
- Next: V_o is de-integrated with V_{REF} until V_o=0
  → Counter output = $2^N\ V_{IN}/V_{REF}$

Dual Slope ADC



http://www.maxim-ic.com/appnotes.cfm/appnote_number/1041

- Integrate V_{in} for fixed time (T_{INT}), de-integrate with V_{REF} applied → $T_{De\text{-}Int} \sim 2^N x T_{CLK} x V_{in}/V_{REF}$
- Most laboratory DVMs use this type of ADC

Dual Slope ADC

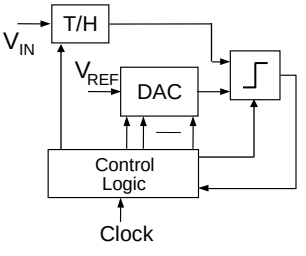
- Advantage:
  - Accuracy to 1st order independent of integrator time-constant and clock period
  - Comparator offset referred to input is attenuated by integrator high DC gain
  - Insensitive to most linear error sources
  - DNL is a function of clock jitter
  - Power line (60Hz) xtalk effect on reading can be canceled by: choosing conversion time multiple of 1/60Hz
  - High accuracy achievable (16+bit)
- Disadvantage:
  - Slow (maximum $2x2^N x T_{clk}$ per conversion)
  - Integrator opamp offset results in ADC offset (can cancel)
  - Finite opamp gain gives rise to INL

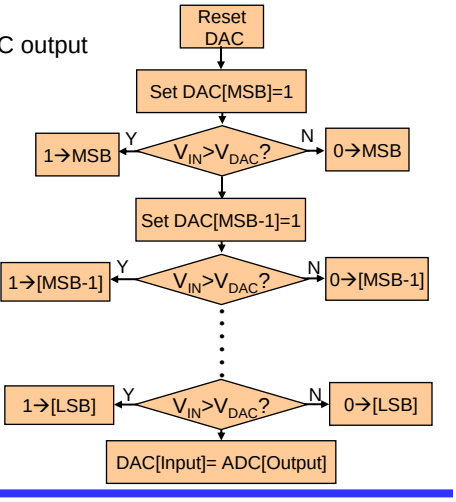
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

Successive Approximation ADC SAR

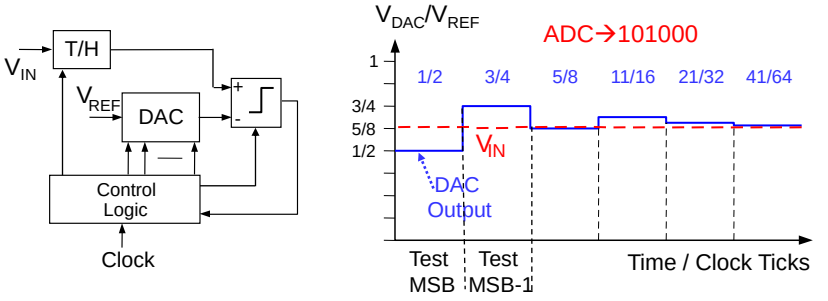
- Algorithmic type ADC
- Based on binary search over DAC output





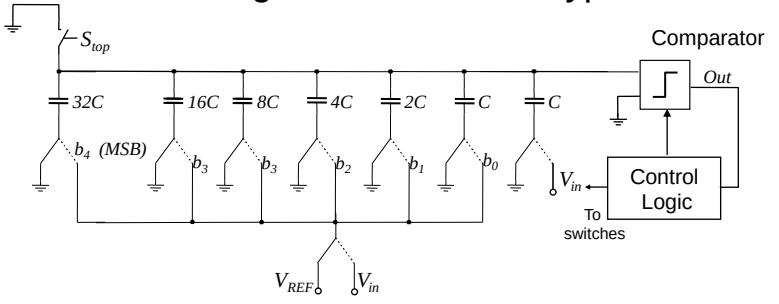
Successive Approximation ADC

Example: 6-bit ADC & $V_{IN}=5/8V_{REF}$



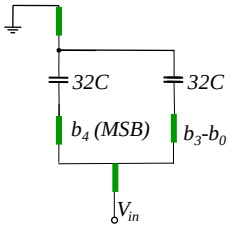
- High accuracy achievable (16+ Bits)
- Need DAC to be accurate enough
- Require N clock cycles for N-bit conversion (much faster than slope type)
- Moderate speed (highest SAR conversion rate 2Ms/sec & 18bits)

Example: SAR ADC
Charge Redistribution Type

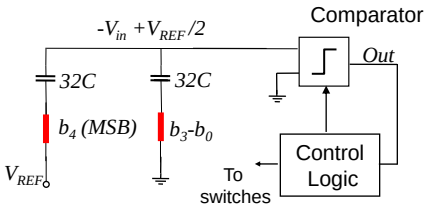


- Built with binary weighted capacitors, switches, comparator & control logic
- T/H inherent in DAC

Charge Redistribution Type SAR DAC Operation: Determining the MSB



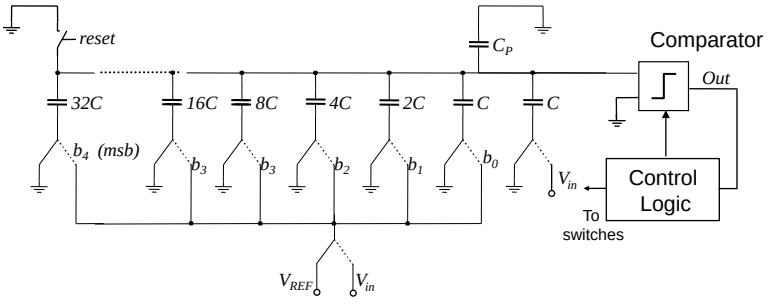
Phase 1



Phase 2

- Operation starts by connecting all top plate to gnd and all bottom plates to V_{in}
- To test the MSB all top plate are opened bottom plate of 32C connected to V_{REF} & rest of bottom plates connected to ground → input to comparator= $-V_{in}+V_{REF}/2$
- Comparator is strobed to determine the polarity of input signal:
  - If negative MSB=1, else MSB=0
- The process continues until all bits are determined

Example: SAR ADC Charge Redistribution Type



- To 1st order parasitic (C_p) insensitive since top plate driven from initial 0 to final 0 by the global negative feedback
- Linearity is a function of accuracy of C ratios
- Possible to add a C ratio calibration cycle (see Ref.)

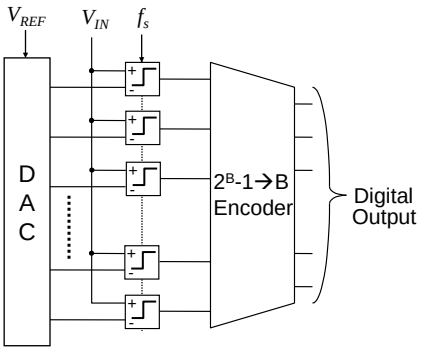
Ref: H. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits,* vol. 19, pp. 813 - 819, December 1984.

ADC Architectures

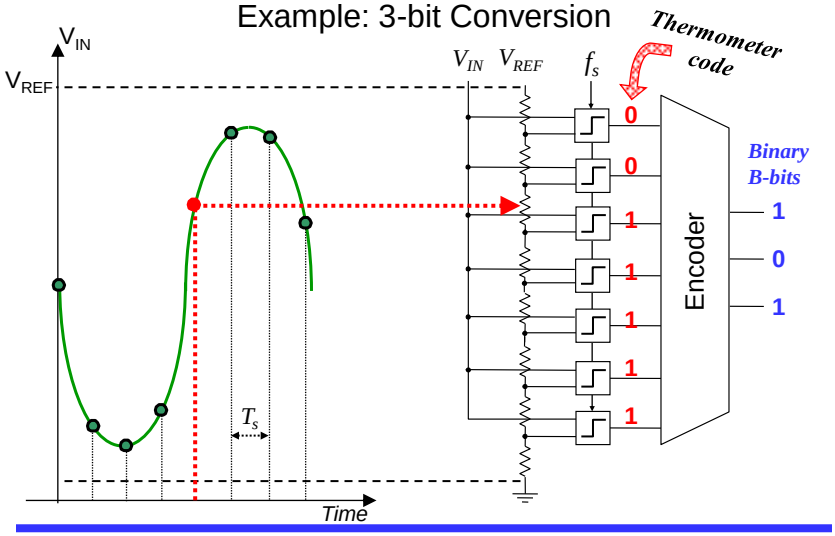
- Slope type converters
- Successive approximation
- Flash
- Time-interleaved / parallel converter
- Folding
- Residue type ADCs
  - Two-step
  - Pipeline
  - …
- Oversampled ADCs

Flash ADC

- B-bit flash ADC:
  - DAC generates all possible $2^B - 1$ levels
  - $2^B - 1$ comparators compare V_{IN} to DAC outputs
  - Comparator output:
    - If $V_{DAC} < V_{IN} \rightarrow 1$
    - If $V_{DAC} > V_{IN} \rightarrow 0$
  - Comparator outputs form thermometer code
  - Encoder converts thermometer to binary code
- Application example: 6-bit Flash ADC in Disk Drives with Gs/s conversion rate

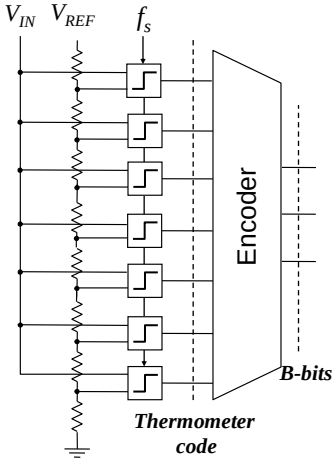


Flash ADC Converter
Example: 3-bit Conversion

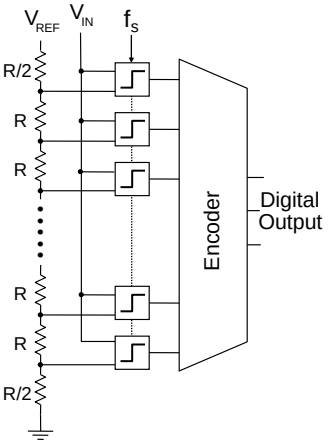


Flash Converter Characteristics

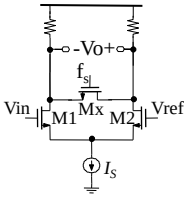
- Very fast: only 1 clock cycle per conversion
  - ½ clock cycle→ V_{IN} & V_{DAC} comparison
  - ½ clock cycle→ 2^B -1 to B encoding
- High complexity: 2^B-1 comparators
- Input capacitance of 2^B-1 comparators connected to the input node:
  - → High capacitance @ input node



Flash ADC Converter Considerations

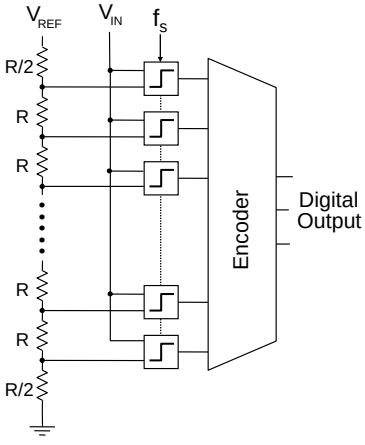


Assume simple comparator design



Depending on Vin level xn lower comparators have M1 on & M2 off xm upper comparators have M1 off & M2 (m+n=2^B-1)
→Total capacitance experienced by input source a function of Vin
→Also note Vin feedthrough to Vref taps via M1 & M2 G-S capacitance & Rs
→When switches Mx open, charge injection and clock feedthru causes perturbation on R taps

Flash Converter Sources of Error

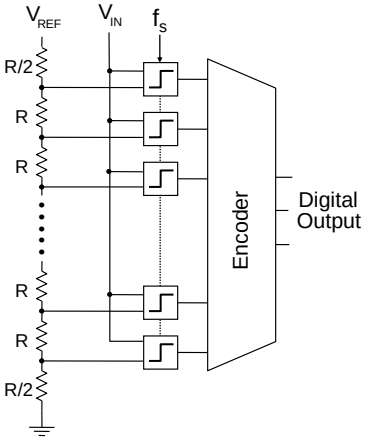


- Comparator input:
  - DC offset
  - Nonlinear input capacitance
  - Feedthrough of input signal to reference ladder
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time (addition of T/H @ the input eliminates this problem)
- Comparator output:
  - Sparkle codes (… 0001011111)
  - Metastability

Flash ADC Converter

Example: 8-bit ADC Comparator Offset Considerations

- 8-bit→ 255 comparators
- V_{REF}=1V → 1LSB=4mV
- DNL<1/2LSB → Comparator input referred offset < 2mV
- Assuming close to 100% yield, 2mV =6σ_{offset}
  → σ_{offset} < 0.33mV



Flash ADC Converter

Example: 8-bits ADC (continued)

→ $1\sigma_{Offset} < 0.33mV$

- Let us assume in the technology used:
  – Voffset-per-unit-sqrt(WxL)=$3\ mVx\ \mu$

$$V_{0\,ffset} = \frac{3mV}{\sqrt{W \times L}} = 0.33mV \quad \rightarrow W \times L = 83\mu^2$$

$$\text{Assuming: } C_{ox} = 9\,fF/\mu^2 \quad \rightarrow C_{GS} = \frac{2}{3} C_{ox} W \times L = 496\,fF$$

$$\rightarrow \text{Total max. input capacitance: } 255 \times 0.496 = 126.5\,pF\,!$$

  – Issues:
    - Si area quite large
    - Large ADC input capacitance
    - Since depending on input voltage level different number of comparator input transistors would be on/off- total input capacitance varies as input varies

    → Nonlinear input capacitance could give rise to signal distortion

Ref: M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.

Flash ADC Converter
Example (continued)

Trade-offs:

- Allowing larger DNL e.g. 1LSB instead of 0.5LSB:
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduces the input capacitance by a factor of 4!
- Reducing the ADC resolution by 1-bit
  - Increases the maximum allowable input-referred offset voltage by a factor of 2
  - Decreases the required device WxL by a factor of 4
  - Reduces the input device area by a factor of 4
  - Reduce the input capacitance by a factor of 4

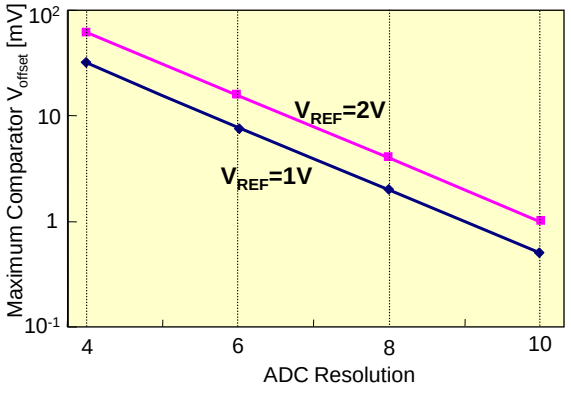
Flash Converter
Maximum Tolerable Comparator Offset versus ADC Resolution

Assumption:

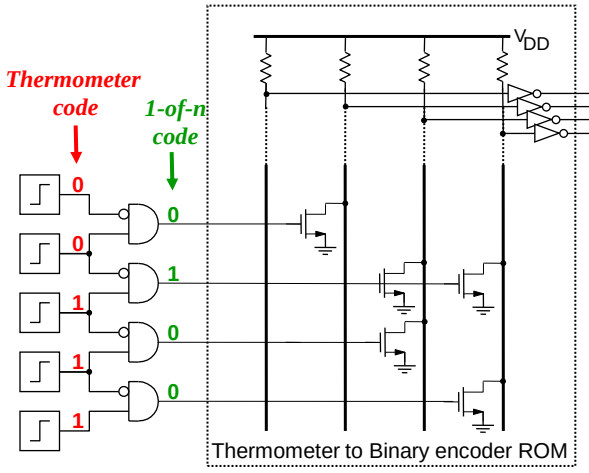
$DNL = 0.5LSB$

Note:

Graph shows max. tolerable offset, note that depending on min acceptable yield, the derived offset numbers are associated with 2σ to 6σ offset voltage



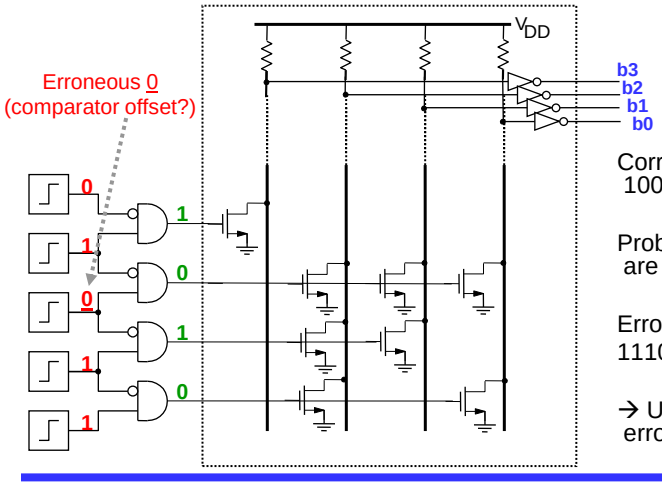
Typical Flash ADC Output Encoder



- Thermometer code → 1-of-n decoding
- Final encoding → NOR ROM
- Ideally, for each code, only one ROM row is on

	b3	b2	b1	b0
Output→	0	0	1	1

Sparkle Codes



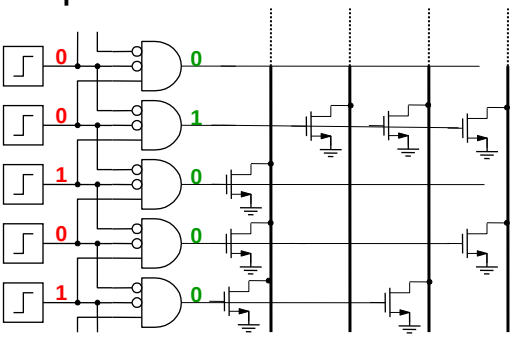
Correct Output: 1000

Problem: Two rows are on

Erroneous Output: 1110

→ Up to ~ ½ FS error!!

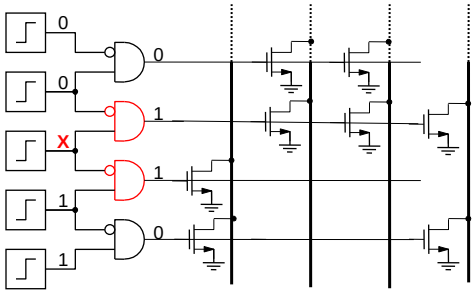
Sparkle Tolerant Encoder



- Protects against a *single* sparkle.
- Possible to improve level of sparkle protection by increasing # of NAND gate inputs

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002

Meta-Stability



Different gates interpret metastable output X differently

Correct output: 1000

Erroneous output: 0000

Solutions:

–Add latches to comparator outputs (high power)

–Gray encoding

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40

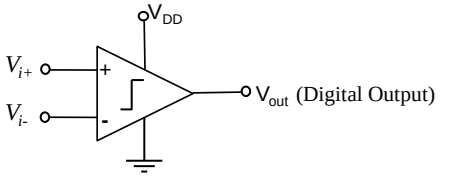
Gray Encoding
Example: 3bit ADC

Thermometer Code							Gray			Binary		
T_7	T_6	T_5	T_4	T_3	T_2	T_1	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	0	0	1	1
0	0	0	1	1	1	1	1	1	0	1	0	0
0	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$
$$G_2 = T_2\overline{T_6}$$
$$G_3 = T_4$$

- Each T_i affects only one G_i
  → Metastability in one T output affects only one of the G bits (unlike binary)
- Protects also against sparkles
- Follow Gray encoder by (latch and) Gray-to-binary encoder

Voltage Comparators



Play an important role in majority of ADCs

Function: Compare the instantaneous value of two analog signals & generate a digital output voltage based on the sign of the difference:

If $V_{i+} - V_{i-} > 0 \rightarrow V_{out} = \text{“1”}$
If $V_{i+} - V_{i-} < 0 \rightarrow V_{out} = \text{“0”}$

Voltage Comparator Architectures

Comparator architecture choices:

- High gain amplifier with differential analog input & single-ended large swing output
  - Output swing has to be compatible with driving digital logic circuits
  - Open-loop amplification→ no frequency compensation required
  - Precise or linear transfer function not required
- Latched comparators; in response to a strobe (clock edge), input stage disabled & digital output stored in a latch till next strobe
  - Two options for implementation :
    - Latch-only comparator
    - Low-gain preamplifier + high-sensitivity latch
- Sampled-data comparators
  - T/H input
  - Offset cancellation

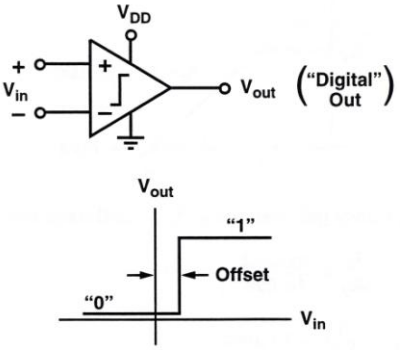
Comparator Built with High-Gain Amplifier

Amplify V_{in}(min) to V_{DD}
→ V_{in}(min) determined by ADC resolution

Example: 12-bit ADC with:
- V_{FS}= 1.5V→ 1LSB=0.36mV
- V_{DD}=1.8V

→ For 1.8V output & 0.5LSB resolution:

$$A_v^{Min} = \frac{1.8V}{0.18mV} \approx 10{,}000$$



Comparator Design
1-Single-Stage Amplification

- Amplifier maximum Gain-Bandwidth product (f_u) for a given technology, typically a function of maximum device f_t

$f_u = unity\text{-}gain\ frequency$, f_o=-3dB frequency $\quad f_o = \frac{f_u}{A_V}$

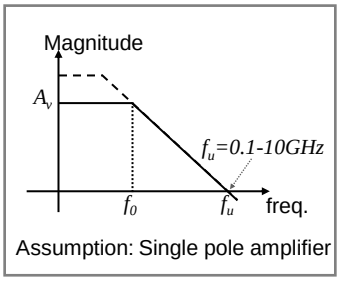
$Example: f_u = 10GHz \ \ \& \ \ A_V = 10{,}000$

$$f_o = \frac{10GHz}{10{,}000} \approx 1MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.16\mu sec$$

$Allowa\ few\ \tau\ for\ output\ to\ settle$

$$f_{Clock}^{Max.} \rightarrow \frac{1}{5\tau_{settling}} \approx 1.26MHz$$

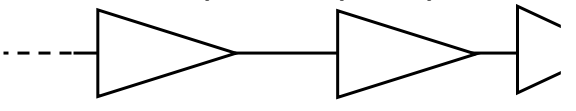


Assumption: Single pole amplifier

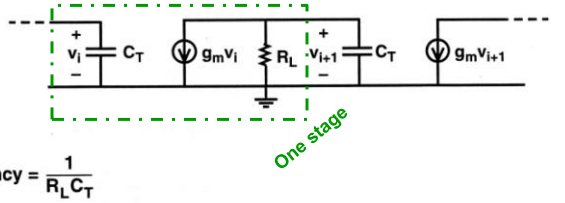
Too slow for majority of applications!

→ Try cascade of lower gain stages to broaden frequency of operation

Comparator Design
2- Cascade of Open Loop Amplifiers



The stages identical → small-signal model for the cascades:



One stage:

$|A_V(0)| = g_m R_L$

ω_o = – 3dB frequency = $\frac{1}{R_L C_T}$

ω_u = – unity gain frequency = G×BW = $\frac{g_m}{C_T}$

$\because \omega_o = \frac{\omega_u}{|A_V(0)|}$

Open Loop Cascade of Amplifiers

For an N-stage cascade:

$$A_T(j\omega) = [A_V(j\omega)]^N = \frac{[A_V(0)]^N}{\left(1+j\frac{\omega}{\omega_0}\right)^N}$$

Define

$\omega_{oN} \equiv$ –3dB frequency of the N-stage cascade

Then

$$|A_T(j\omega_{oN})| = \frac{|A_V(0)|^N}{\sqrt{2}}$$

and

$$\omega_{oN} = \omega_o\sqrt{2^{1/N}-1} = \frac{\omega_u}{|A_V(0)|}\sqrt{2^{1/N}-1}$$

$\therefore$ For a specified $|A_T(0)|$

$$|A_V(0)| = |A_T(0)|^{1/N}$$

$$\Rightarrow \omega_{oN} = \frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}$$

Thus,

$$\frac{\omega_{oN}}{\omega_{o1}} = \left[\frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1}\right] \Big/ \left[\frac{\omega_u}{|A_T(0)|}\right]$$

$$= |A_T(0)|^{\left(\frac{N-1}{N}\right)}\sqrt{2^{1/N}-1}$$

Example: N=4, A_T=10000→ $\omega_{oN}=430\omega_{o1}$

Open Loop Cascade of Amplifiers

For $|A_T(DC)|$=10,000

N	ω_{oN}/ω_{o1}	$\lvert A_V(0)\rvert$
1	1	10,000
2	64	100
3	236	21.5
4	435	10
5	611	6.3
10	1067	2.5
20	1185	1.6

Example:

$N=3,\ f_u=10GHz\ \&\ |A_T(0)|=10000$

$$f_{oN} = \frac{10GHz}{(10{,}000)^{1/3}}\sqrt{2^{1/3-1}} \approx 237MHz$$

$$\tau_{settling} = \frac{1}{2\pi f_o} = 0.7nsec$$

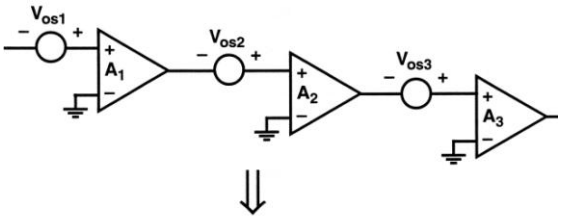
Allow a few τ for output to settle

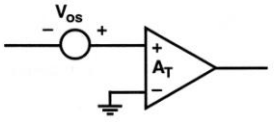
$$f_{Clock}^{Max.} \rightarrow \frac{1}{5\tau_{settling}} \approx 290MHz$$

f_{max} improved from *1.26MHz to 290MHz* → *X236*

Open Loop Cascade of Amplifiers
Offset Voltage

- **From offset point of view: high gain/stage is preferred**
- **Choice of # of stage**
  →bandwidth vs offset tradeoff



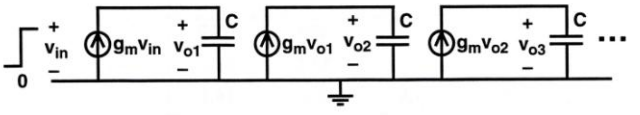


$$A_T = A_1 \cdot A_2 \cdot A_3$$

Input-referred offset $\rightarrow V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$

Open Loop Cascade of Amplifiers
Step Response

- **Assuming linear behavior (not slew limited)**



$$v_{o1} = \frac{1}{C}\int_0^t g_m v_{in} dt = \frac{g_m}{C} v_{in} t$$

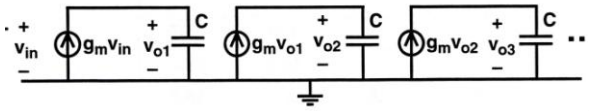
$$v_{o2} = \frac{1}{C}\int_0^t g_m v_{o1} dt = \frac{g_m}{C}\int_0^t \frac{g_m}{C} v_{in} dt = \frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2$$

$$v_{o3} = \frac{1}{C}\int_0^t g_m v_{o2} dt = \frac{g_m}{C}\int_0^t \left[\frac{1}{2}\left(\frac{g_m}{C}\right)^2 v_{in} t^2\right] dt$$

$$= \frac{1}{3}\left(\frac{1}{2}\right)\left(\frac{g_m}{C}\right)^3 v_{in} t^3$$

Open Loop Cascade of Amplifiers Step Response

- **Assuming linear behavior**



N Stages

$$v_{oN} = \left(\frac{g_m}{C}\right)^N \left(\frac{t^N}{N!}\right) v_{in}$$

For the output to reach a specified v_{out} (i.e., $v_{oN} = v_{out}$) the delay is

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{v_{out}}{v_{in}}\right)\right]^{1/N}$$

Open Loop Cascade of Amplifiers Delay/(C/g_m)

$$\tau_D = \left(\frac{C}{g_m}\right)\left[(N!)\left(\frac{V_{out}}{V_{in}}\right)\right]^{1/N}$$

- **Minimum total delay broad function of N**
- **Relationship between # of stages resulting in minimum delay (N_{op}) and gain (V_{out}/V_{in}) approximately:**

$$N_{opt} \approx 1 + \log_2 A_T \quad for\ A < 1000$$

$$N_{opt} \approx 1.2 \ln A_T \quad for\ A \geq 1000$$

Delay/(C/g_m)

V_{out}/V_{in} / N	10	100	1000	10K
1	10	100	1000	10K
2	4.5	14.1	44.7	141
3	3.9	8.4	18.2	39.1
4	3.9	7.0	12.4	22.1
5	4.1	6.5	10.4	16.4
6	4.4	6.4	9.5	13.9
7	4.7	6.5	9.1	12.6
8	5.0	6.7	8.9	11.9
9	5.4	6.9	8.9	11.5
10	5.7	7.2	9.0	11.4
11	6.1	7.5	9.2	11.3
12	6.4	7.8	9.4	11.4
20	9.3	10.5	11.7	13.2

Ref: J.T. Wu, et al., "A 100-MHz pipelined CMOS comparator " *IEEE Journal of Solid-State Circuits,* vol. 23, pp. 1379 - 1385, December 1988.