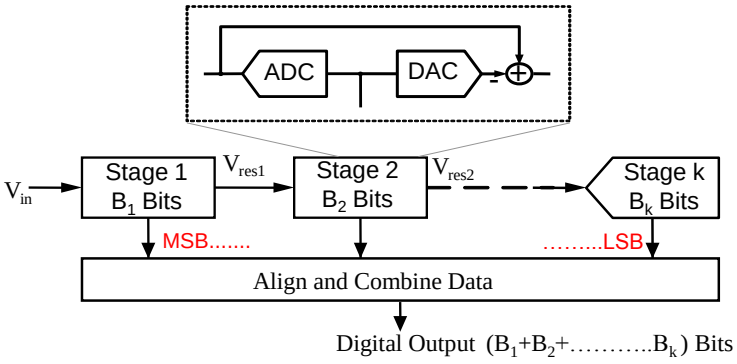
EE247
Lecture 22

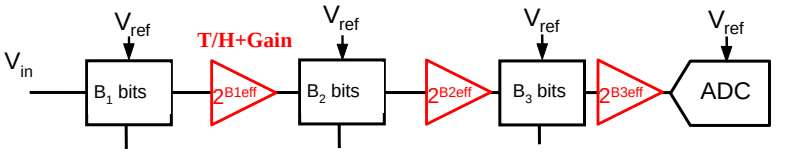
- Pipelined ADCs (continued)
  - Effect sub-ADC, gain stage, sub-DAC non-idealities on overall ADC performance (continued)
    - Correction for inter-stage gain nonlinearity
  - Implementation
    - Combining the bits
    - Practical circuits
    - Stage scaling
    - Stage implementation
      - Circuits
      - Noise budgeting
    - How many bits per stage?
  - Algorithmic ADCs utilizing pipeline structure
  - Advanced background calibration techniques
- Time Interleaved Converters
- ADC figures of merit

Pipeline ADC
Block Diagram



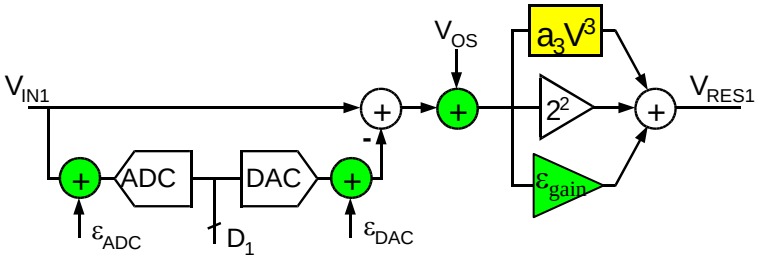
- Idea: Cascade several low resolution stages to obtain high overall resolution (e.g. 10bit ADC can be built with series of 10 ADCs each 1-bit only!)
- Each stage performs coarse A/D conversion and computes its quantization error, or "residue"

Summary So Far
Pipelined A/D Converters



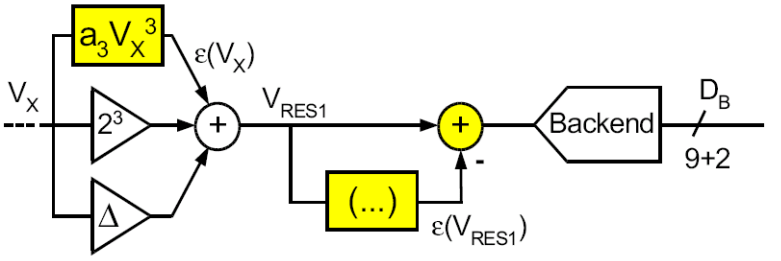
- Cascade of low resolution stages
  - By adding inter-stage gain= 2^{Beff}
    - No need to scale down Vref for stages down the pipe
    - Reduced accuracy requirement for stages coming after stage 1
  - Addition of Track & Hold function to interstage-gain
    - Stages can operate concurrently
    - Throughput increased to as high as one sample per clock cycle
    - Latency function of number of stages & conversion-per-stage
  - Correction for circuit non-idealities
    - Built-in redundancy compensate for sub-ADC inaccuracies such as comparator offset (interstage gain: $G=2^{Bneff}$, $B_{neff} < B_n$)
    - Error associated with gain stage and sub-DAC calibrated out

Pipelined ADC
Error Correction/Calibration Summary



Error	Correction/Calibration
ε_{ADC}, V_{os}	Redundancy either same stage or next stage
ε_{gain}	Digital adjustment
ε_{DAC}	Either sufficient component matching or digital calibration
Inter-stage amplifier non-linearity	?

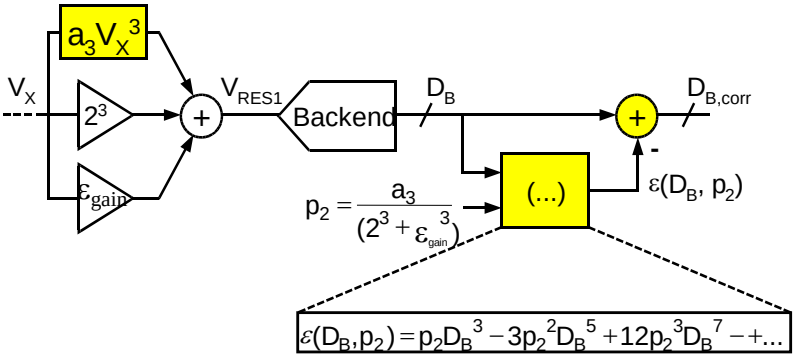
Inter-stage Gain Nonlinearity



- Invert gain stage non-linear polynomial
- Express error as function of V_{RES1}
- Push error compensator into digital domain through backend ADC

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

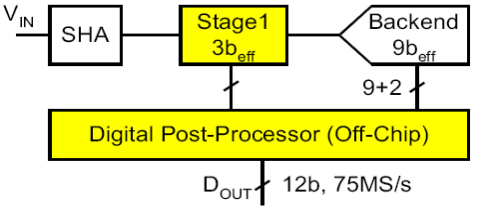
Inter-stage Gain Nonlinearity



- Pre-measured & stored in table look-up form
- p_2 continuously estimated & updated (account for temp. & other variations)

Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

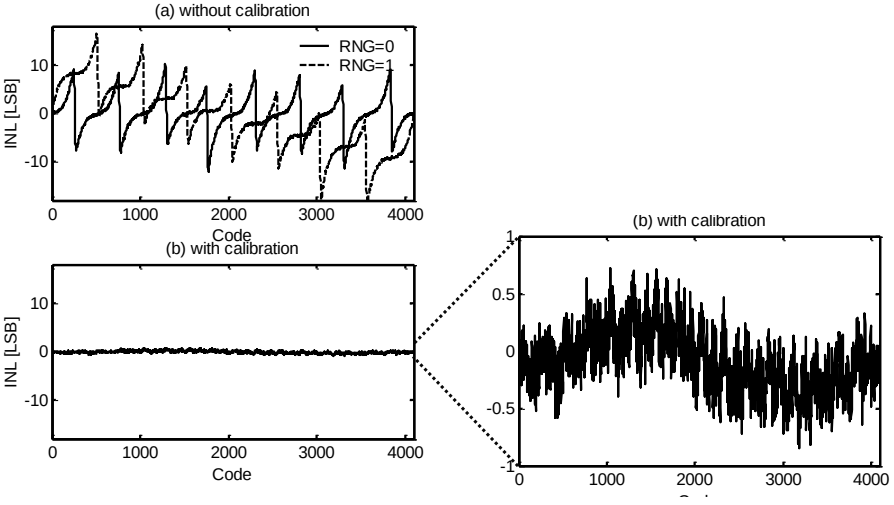
Inter-stage Gain Nonlinearity Compensation
Proof of Concept Evaluation Prototype



- Re-used 14-bit ADC in 0.35μm from Analog Devices [Kelly, ISSCC 2001]
- Modified only 1st stage with 3-b_{eff} → open-loop amplifier built with simple diff-pair + resistive load instead of the conventional feedback around high-gain amp
- Conventional 9-b_{eff} backend, 2-bit redundancy in 1st stage
- Real-time post-processor off-chip (FPGA)

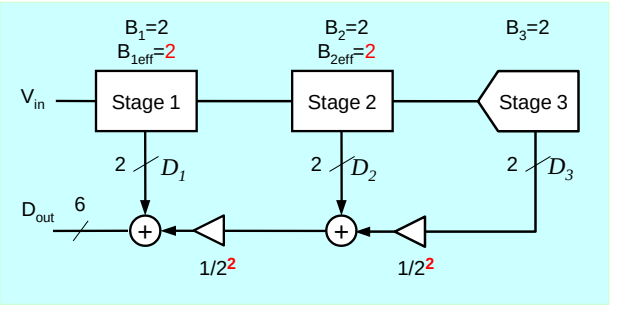
Ref: B. Murmann and B. E. Boser, "A 12-b, 75MS/s Pipelined ADC using Open-Loop Residue Amplification," *ISSCC Dig. Techn. Papers*, pp. 328-329, 2003

Measurement Results
12-bit ADC w Extra 2-bits for Calibration



Combining the Bits

- Example: Three 2-bit stages, no redundancy



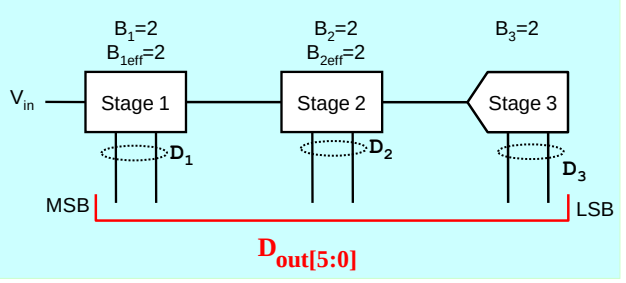
$$D_{out} = D_1 + \frac{1}{2^{B1eff}} D_2 + \frac{1}{2^{B1eff} \cdot 2^{B2eff}} D_3$$

$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

Combining the Bits

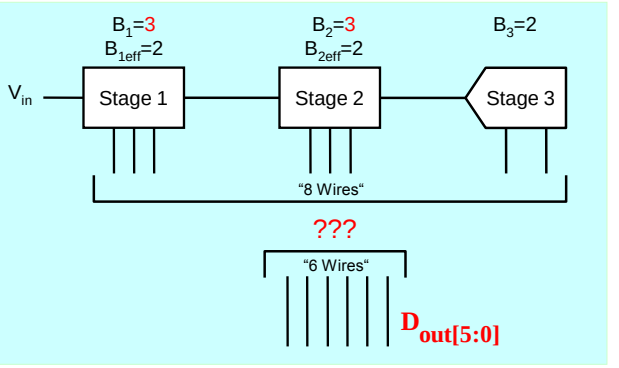
```
D1     XX
D2       XX
D3         XX
-------------
Dout   DDDDDD
```

- Only bit shifts
- No arithmetic circuits needed



Combining the Bits Including Redundancy

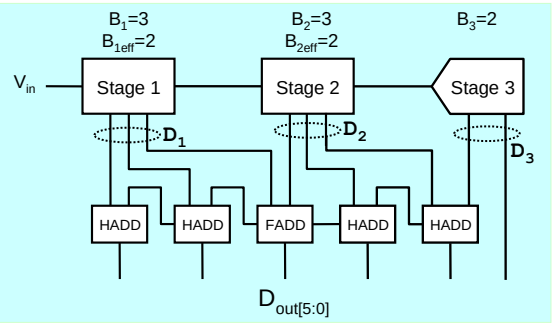
- Example: Three 2-bit stages, incorporating 1- bit redundancy in stages 1 and 2



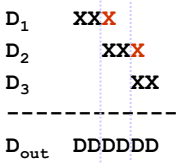
Combining the Bits

$$D_{out} = D_1 + \frac{1}{2^{B1eff}} D_2 + \frac{1}{2^{B1eff} \cdot 2^{B2eff}} D_3$$

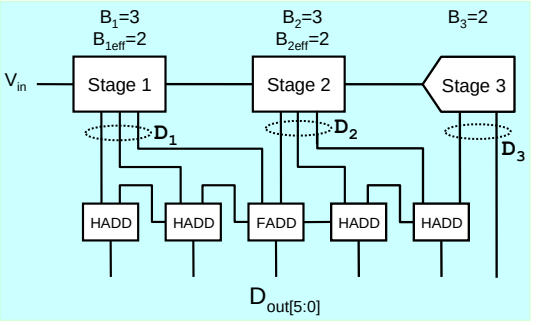
$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$



- Bits overlap
- Need adders

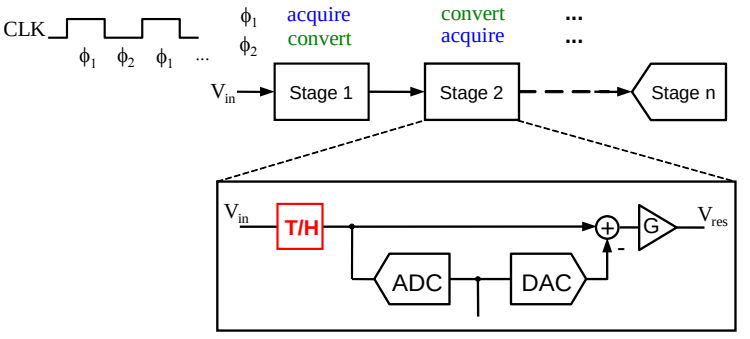


Combining the Bits Example



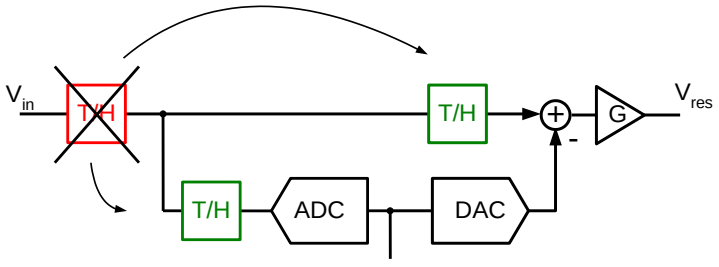

```
D1      001
D2        111
D3          10
------------
Dout    011000
```


Pipelined ADC Stage Implementation



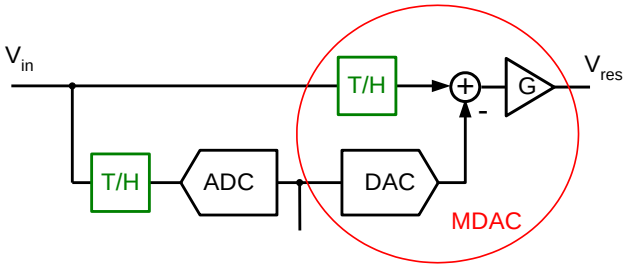
- Each stage needs T/H hold function
- Track phase: Acquire input/residue from previous stage
- Hold phase: sub-ADC decision, compute residue

Stage Implementation



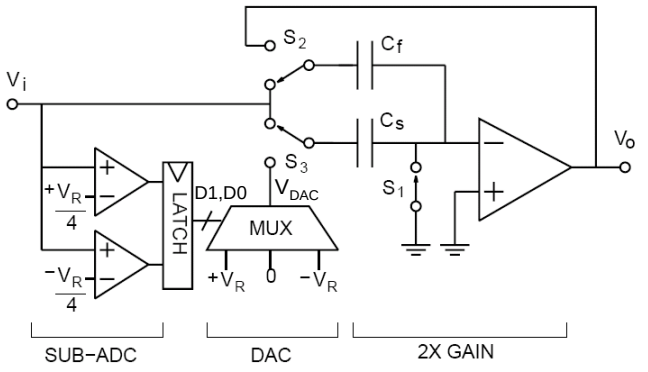
- Usually no dedicated T/H amplifier in each stage (Except first stage in some cases – why?)
- T/H implicitely contained in stage building blocks

Stage Implementation



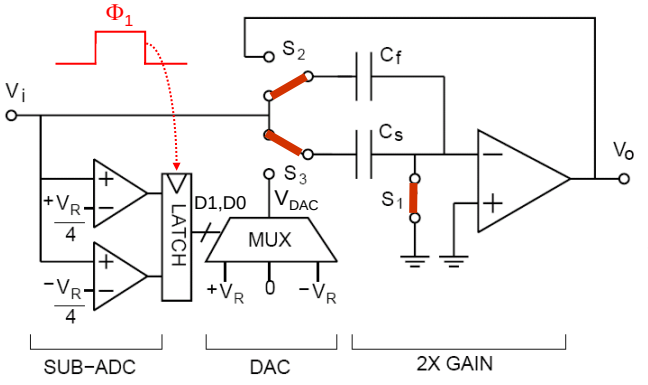
- DAC-subtract-gain function can be lumped into a single switched capacitor circuit
- "MDAC"

1.5-Bit Stage Implementation Example



Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation Acquisition Cycle



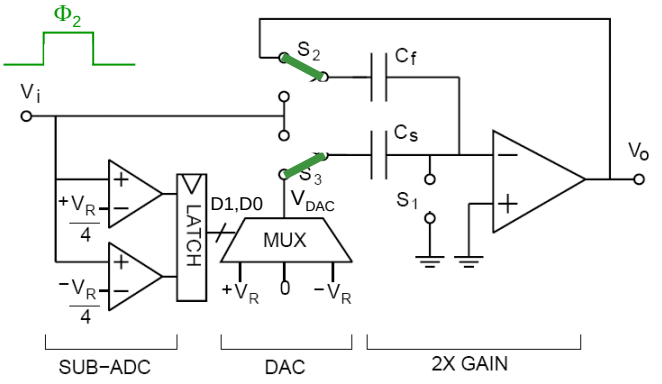
$Vc_f=Vc_s=V_i$

$Q_{Cs}=C_s x V_i$

$Q_{Cf}=C_f x V_i$

Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation
Conversion Cycle



Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

1.5-Bit Stage Implementation
Conversion Cycle

V_{DAC} induces equal currents in C_s and C_f :

$$V_{DAC} \times C_s = -V_o \times C_f$$

$$Q_{Cf} = -V_{DAC} \times C_s$$

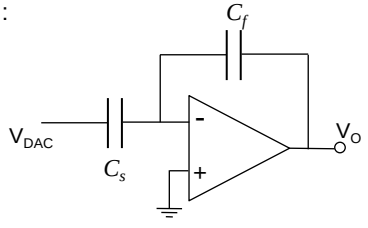
$$Q_{Cf}^{Total}\Big|_{\phi 2} = Q_{Cf}\Big|_{\phi 1} + Q_{Cs}\Big|_{\phi 1} - V_{DAC} \times C_s$$

$$V_o \times C_f = V_i \times C_f + V_i \times C_s - V_{DAC} \times C_s$$

$$V_o = V_i\left(1 + \frac{C_s}{C_f}\right) - V_{DAC} \times \frac{C_s}{C_f}$$

$$C_s = C_f$$

$$V_o = 2V_i - V_{DAC}$$



	D1,D0	V_{DAC}
$V_i > V_R/4$	1 1	$-V_R$
$-V_R/4 < V_i < V_R/4$	0 1	0
$V_i < -V_R/4$	0 0	$+V_R$

1.5 Bit Stage Implementation Example

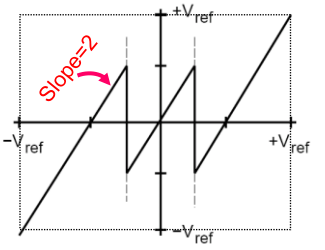
$$V_o = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_i - \frac{C_s}{C_f}V_{ref} & \text{if } V_i > V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i & \text{if } -V_{ref}/4 \le V_i \le +V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i + \frac{C_s}{C_f}V_{ref} & \text{if } V_i < -V_{ref}/4 \end{cases}$$

Note:

Interstage gain set by C ratios

→ Accuracy better than 0.1%

→Up to 10bit level no need for gain calibration



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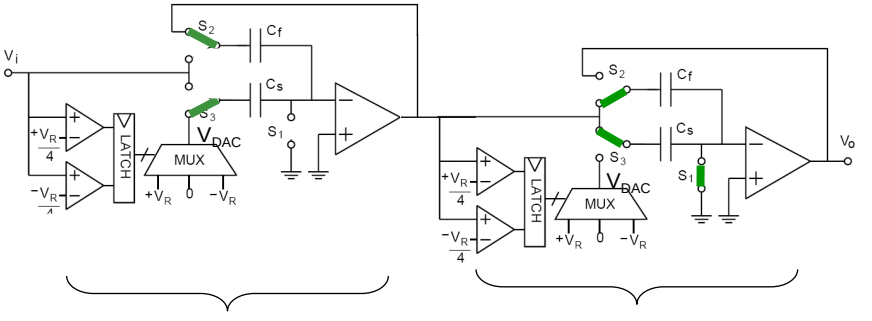
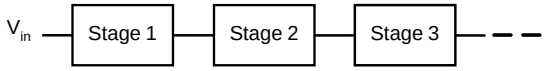
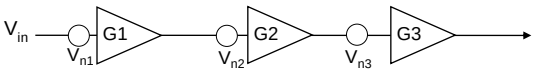
1.5-Bit Stage Implementation Timing of Stages



Pipelined ADC Stage Power Dissipation & Noise

- Typically pipeline ADC noise dominated by inter- stage gain blocks
- Sub-ADC comparator noise translates into comparator threshold uncertainty and is compensated for by redundancy

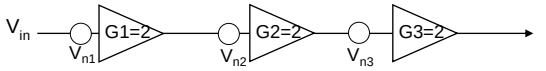


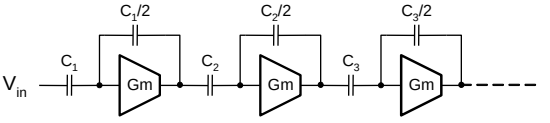


$$V_{noise}^{in} = \sqrt{V_{n1}^2 + \frac{V_{n2}^2}{G1^2} + \frac{V_{n3}^2}{G1^2 G2^2} + \ldots}$$

Pipelined ADC Stage Scaling

- Example: Pipeline using 1-bit$_{eff}$ stages



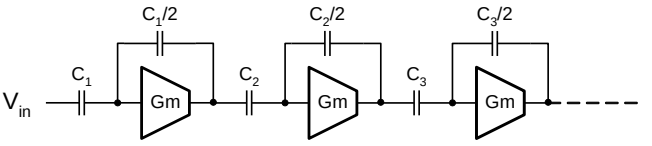


- Total input referred noise power:

$$N_{tot} \propto kT\left[\frac{1}{C_1} + \frac{1}{G1^2 C_2} + \frac{1}{G1^2 G2^2 C_3} + \ldots\right]$$

$$N_{tot} \propto kT\left[\frac{1}{C_1} + \frac{1}{4C_2} + \frac{1}{16C_3} + \ldots\right]$$

Pipelined ADC Stage Scaling

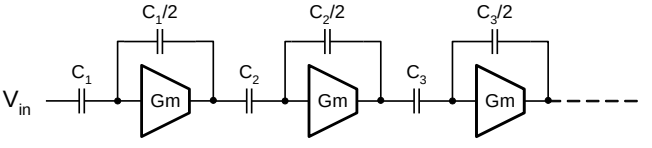


$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+...\right]$$

- If all caps made the same size, backend stages contribute very little noise
- Wasteful power-wise, because:
  - Power ~ Gm
  - Speed ~ Gm/C

    Fixed speed → Gm/C filxed → Power ~ C

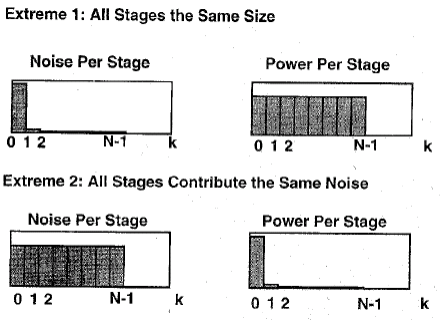
Pipelined ADC Stage Scaling



$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+...\right]$$

- How about scaling caps down by $G^2=2^2=4x$ per stage?
  - Same amount of noise from every stage
  - All stages contribute significant noise
  - To keep overall noise the same → noise/stage must be reduced
  - Power ~ Gm ~ C goes up!

Stage Scaling
Example: 2-bit$_{eff}$ /stage

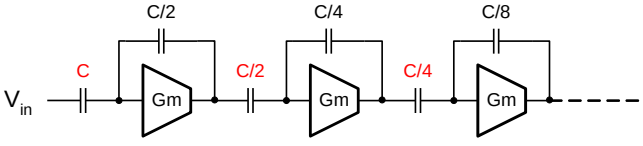


- Optimum capacitior scaling lies approximately midway between these two extremes

Ref: D. W. Cline, P.R. Gray "A power optimized 13-b 5MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

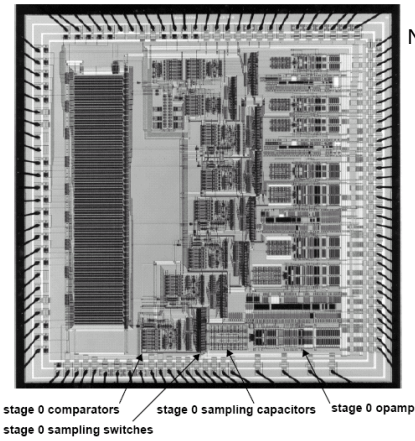
Pipeline ADC
Stage Scaling

- Power minimum is "shallow“
- Near optimum solution in practice: Scale capacitors by stage gain
- E.g. for effective stage resolution of 1bit (Gain=2):



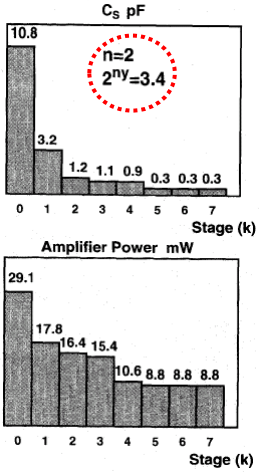
$$N_{tot} \propto kT\left[\frac{1}{C}+\frac{1}{2C}+\frac{1}{4C}+...\right]$$

Stage Scaling Example



Note:
Resolution per stage:
→2bits

→G=4



Ref: D. W. Cline, P.R Gray "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2um CMOS," JSSC 3/1996

How Many Bits Per Stage?

- Many possible architectures
  - E.g. B_{1eff}=3, B_{2eff}=1, ...
    vs. B_{1eff}=1, B_{2eff}=1, B_{3eff}=1, ...
- Complex optimization problem, fortunately optimum tends to be shallow...
- Qualitative answer:
  - Maximum speed for given technology
    - Use small resolution-per-stage (large feedback factor)
  - Maximum power efficiency for fixed, "low" speed
    - Try higher resolution stages
    - Can help alleviate matching & noise requirements in stages following the 1st stage
      Ref: Singer VLSI 96, Yang, JSSC 12/01 (14bit ADC w/o calibration)

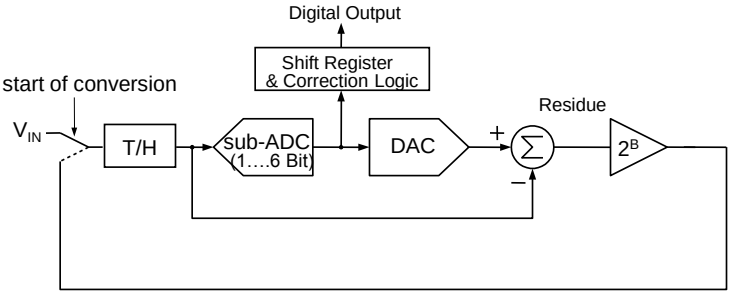
14 & 12-Bit State-of-the-Art Implementations

Reference	Yang (JSSC 12/2001) 0.35μ/3V	Loloee (ESSIRC 2002) 0.18μ/3V
Bits	14	12
Architecture	3-1-1-1-1-1-1-1-1-3	1-1-1-1-1-1-1-1-1-1-2
SNR/SFDR	~73dB/88dB	~66dB/75dB
Speed	75MS/s	80MS/s
Power	340mW	260mW

10 & 8-Bit State-of-the-Art Implementations

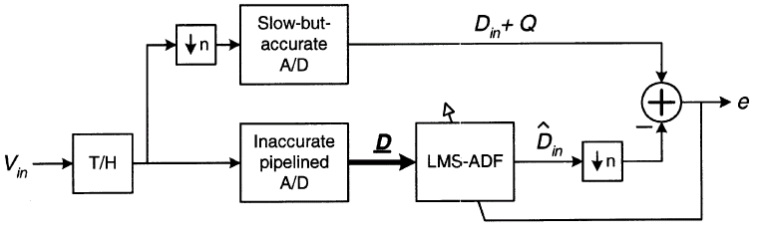
Reference	Yoshioko et al (ISSCC 2005) 0.18μ/1.8V	Kim et al (ISSCC 2005) 0.18μ/1.8V
Bits	10	8
Architecture	1.5bit/stage	2.8 -2.8 - 4
SNR/SFDR	~55dB/66dB	~48dB/56dB
Speed	125MS/s	200MS/s
Power	40mW	30mW

Algorithmic ADC



- Essentially same as pipeline, but a single stage is reused for all partial conversions
- For overall $B_{overall}$ bits → need $B_{overall}/B_{stage}$ clock cycles per conversion
  - → Small area, slow
  - → Trades conversion time for area

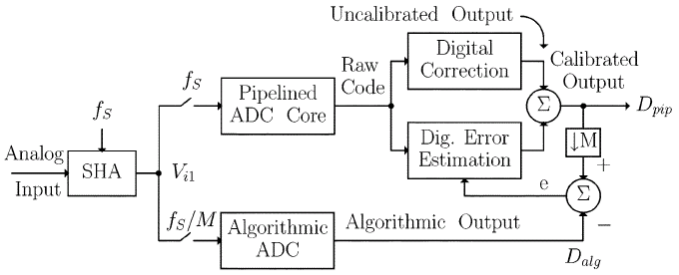
Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters



- Slow, but accurate ADC operates in parallel with pipelined (main) ADC
- Slow ADC samples input signal at a lower sampling rate (f_s/n)
- Difference between corresponding samples for two ADCs (e) used to correct fast ADC digital output via an adaptive digital filter (ADF) based on minimizing the Least-Mean-Squared error

Ref: Y. Chiu, *et al,* "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," IEEE TRANS. CAS, VOL. 51, NO. 1, JANUARY 2004

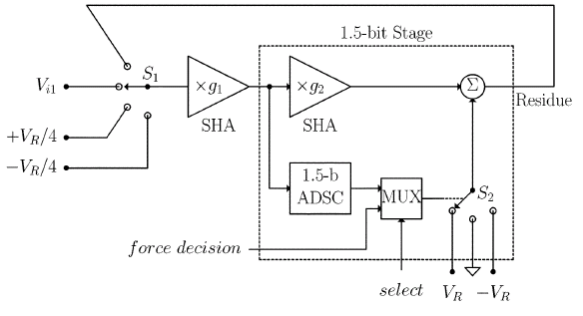
Example: "A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration"



- Pipelined ADC operates at 20Ms/s @ has 1.5bit/stage
- Slow ADC → Algorithmic type operating at 20Ms/32=625ks/s
- Digital correction accounts for bit redundancy
- Digital error estimator → minimizes the mean-squared-error

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

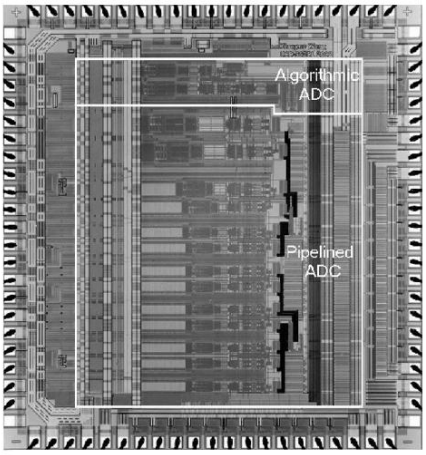
Algorithmic ADC Used for Calibration of Pipelined ADC (continued from previous page)



- Uses replica of pipelined ADC stage
- Requires extra SHA in front to hold residue
- Undergoes a calibration cycle periodically prior to being used to calibrate pipelined ADC

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Sampling capacitors scaled ($1B_{eff}$/stage):

- Input SHA: 6pF
- Pipelined ADC: 2pF,0.9,0.4,0.2, 0.1,0.1…
- Algorithmic ADC: 0.2pF

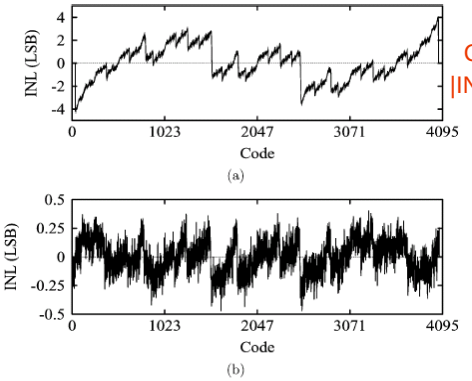
Chip area: 13.2mm^2

- Does not include digital calibration circuitry estimated ~1.7mm^2
- Area of Algorithmic ADC <20%

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results

12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

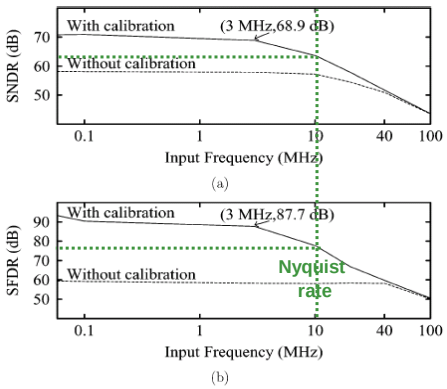


Without Calibration |INL|<4.2LSB

With Calibration |INL|<0.5LSB

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration



Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

Measurement Results
12-bit 20-MS/s Pipelined ADC with Digital Background Calibration

PERFORMANCE SUMMARY (3.3 V, 25 °C)

Process	0.35μm 2P4M CMOS	
Sampling rate	20 Msample/s	
Active area	7.5 mm^2	
Full-Scale Input	1.6 Vp-p	
	Without Cal.	With Cal.
Analog Power Diss.	190 mW	226 mW
Total Power Diss.	217 mW	254 mW
Max. |INL| (Pip. ADC)*	4.21 LSB	0.47 LSB
Max. |DNL| (Pip. ADC)*	0.60 LSB	0.41 LSB
SNDR (Alg. ADC)*	49.6 dB	59.6 dB
SNDR (Pip. ADC)*	58.2 dB	70.8 dB
SFDR (Pip. ADC)*	59.4 dB	93.3 dB
THD (Pip. ADC) *	–59.4 dB	–92.9 dB
PSRR*	65.0 dB	64.8 dB
CMRR*	73.6 dB	73.4 dB

*f_{in}=58 kHz

Does not include digital calibration circuitry estimated ~1.7mm^2

Alg. ADC SNDR dominated by noise

Ref: X. Wang, P. J. Hurst, *S.* H. Lewis, " A 12-bit 20-MS/s pipelined analog-to-digital converter with nested digital background calibration", IEEE JSSC, vol. 39, pp. 1799 - 1808, Nov. 2004

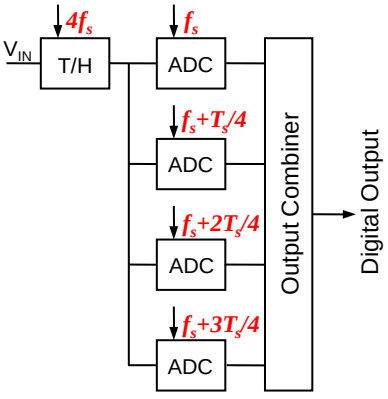
ADC Architectures

- Slope type converters
- Successive approximation
- Flash
- Interpolating & Folding
- Residue type ADCs
  - Two-step Flash
  - Pipelined ADCs

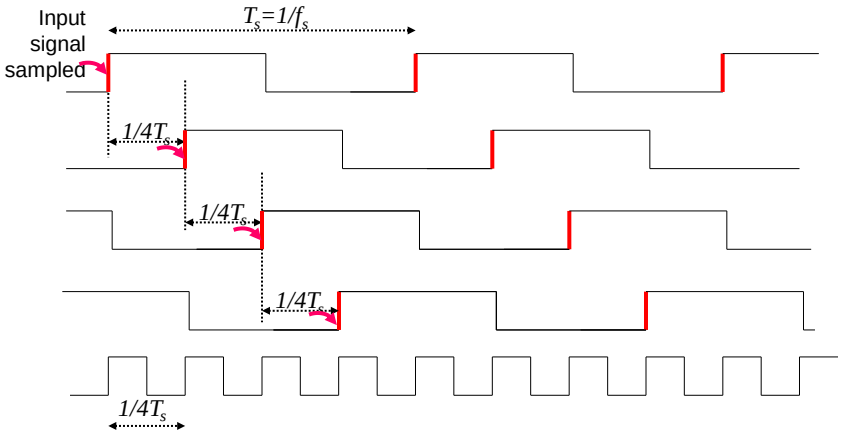
➡ • Time-interleaved / parallel converter
- Oversampled ADCs

Time Interleaved Converters

- Example:
  - 4 ADCs operating in parallel at sampling frequency f_s
  - Each ADC converts on one of the 4 possible clock phases
  - Overall sampling frequency= $4f_s$
  - Note T/H has to operate at $4f_s$!
- Extremely fast:
  Typically, limited by speed of T/H
- Accuracy limited by mismatch among individual ADCs (timing, offset, gain, …)



Time Interleaved Converters Timing



- Note: Effective sampling rate→ $4xf_s$

ADC Figures of Merit

- Objective: Establish measure/s to compare performance of various ADCs
- Can use FOM to combine several performance metrics to get one single number
- What are reasonable FOM for ADCs?

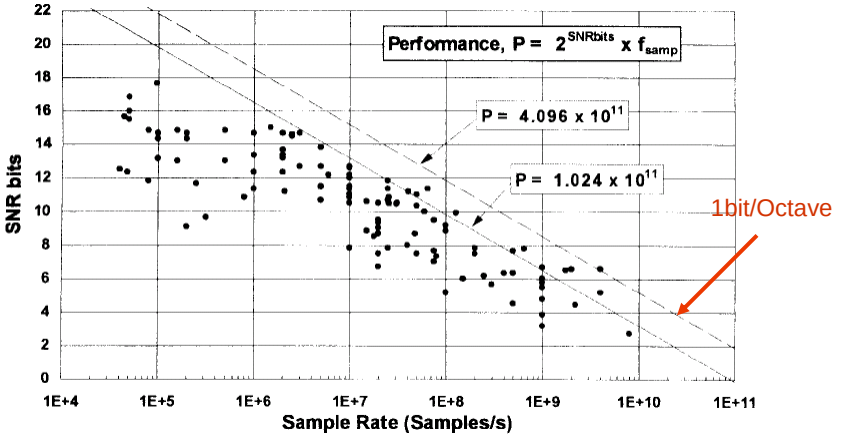
ADC Figures of Merit

$$FOM_1 = f_s \cdot 2^{ENOB}$$

- This FOM suggests that adding an extra bit to an ADC is just as hard as doubling its bandwidth
- Is this a good assumption?

Ref: R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999

Survey Data



Ref: R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999

ADC Figures of Merit

$$FOM_2 = \frac{Power}{f_s \cdot 2^{ENOB}} \quad [J/conv]$$

- Sometimes inverse of this metric is used
- In typical circuits power ~ speed, FOM_2 captures this tradeoff correctly
- How about power vs. ENOB?
  - One more bit 2x in power?

Ref: R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999

ADC Figures of Merit

- One more bit means...
  - 6dB SNR, 4x less noise power, 4x larger C
  - Power ~ Gm ~ C increases 4x
- Even worse: Flash ADC
  - Extra bit means 2x number of comparators
  - Each of them needs double precision
  - Transistor area 4x, Current 4x to keep same current density
  - Net result: Power increases 8x

ADC Figures of Merit

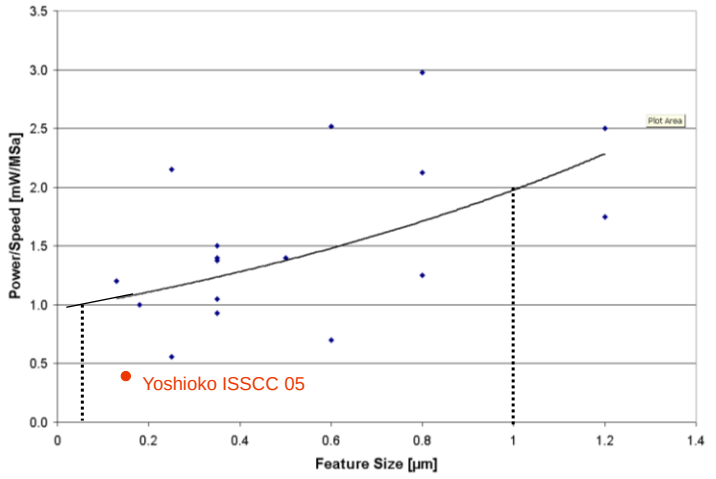
- FOM_2 seems not entirely appropriate, but somehow still standard in literature, papers
- "Tends to work" because:
  - Not all power in an ADC is "noise limited“
  - E.g. Digital power, biasing circuits, etc.
- Better use FOM_2 to compare ADCs with same resolution!

ADC Figures of Merit

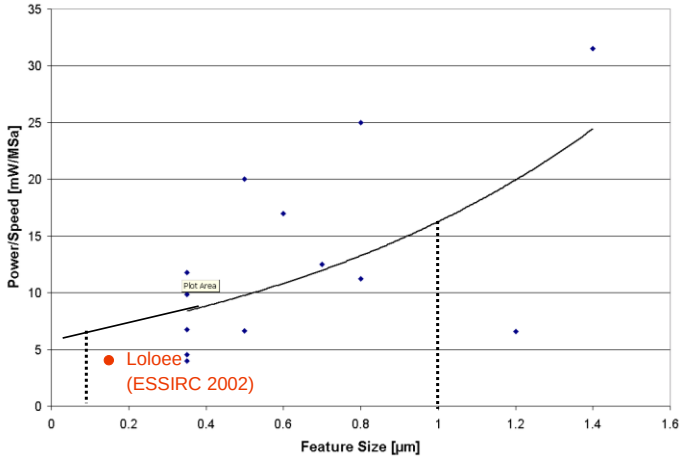
$$FOM_3 = \frac{Power}{Speed}$$

- Compare only power of ADCs with approximately same ENOB
- Useful numbers:
  - 10b (~9 ENOB) ADCs: 1 mW/MSample/sec
    Note the ISSCC 05 example: 0.33mW/MS/sec!
  - 12b (~11 ENOB) ADCs: 4 mW/MSample/sec

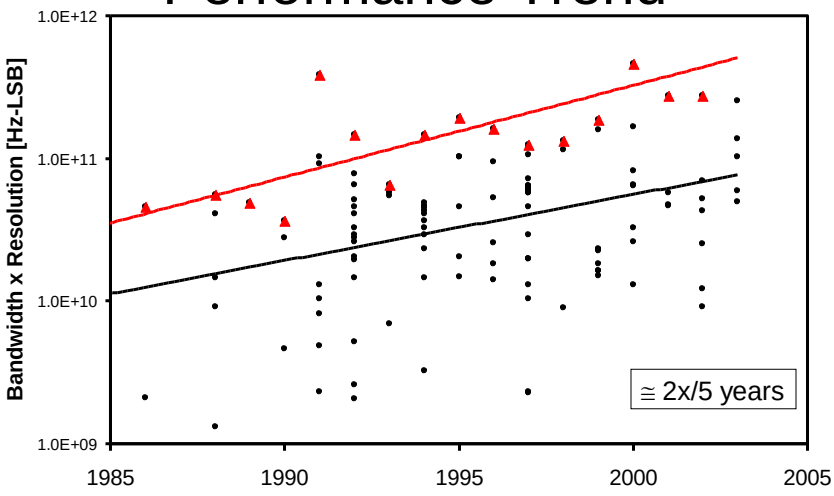
10-Bit ADC Power/Speed



12-Bit ADC Power/Speed



Performance Trend



ADC Architectures

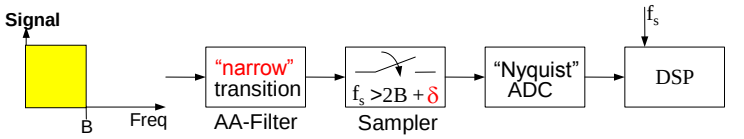
- Slope type converters
- Successive approximation
- Flash
- Interpolating & Folding
- Residue type ADCs
  - Two-step Flash
  - Pipelined ADCs
- Time-interleaved / parallel converter
- Oversampled ADCs

Analog-to-Digital Converters

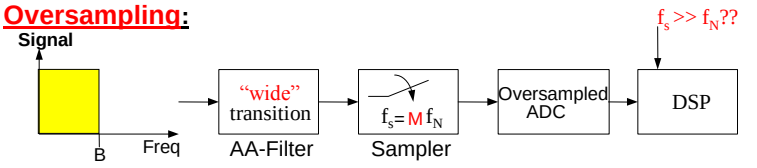
- Two categories:
  - Nyquist rate ADCs → $f_{sig}^{max} \sim 0.5 x f_{sampling}$
    - Maximum achievable signal bandwidth higher compared to oversampled type
    - Resolution limited to max. ~14 to 16bits
  - Oversampled ADCs → $f_{sig}^{max} << 0.5 x f_{sampling}$
    - Maximum possible signal bandwidth lower compared to nyquist rate ADCs
    - Maximum achievable resolution high (18 to 20bits!)

The Case for Oversampling

Nyquist sampling:

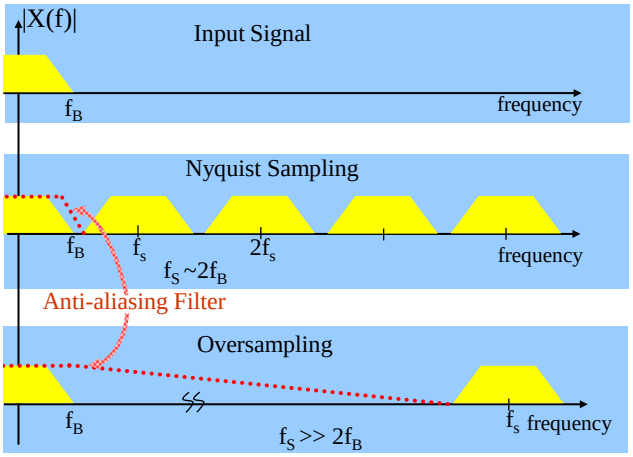


Oversampling:



- Nyquist rate f_N ~2B
- Oversampling rate M = f_s/f_N >> 1

Nyquist v.s. Oversampled Converters Antialiasing Requirements

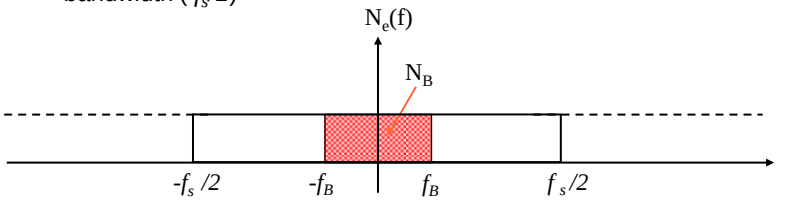


Oversampling Benefits

- Almost no stringent requirements imposed on analog building blocks
- Takes advantage of the availability of low cost, low power digital filtering
- Relaxed transition band requirements for analog anti-aliasing filters
- Reduced baseband quantization noise power
- Allows trading speed for resolution

ADC Converters
Baseband Noise

- For a quantizer with quantization step size Δ and sampling rate f_s:
  - Quantization noise power distributed uniformly across Nyquist bandwidth ($f_s/2$)



  - Power spectral density:

$$N_e(f) = \frac{\overline{e^2}}{f_s} = \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}$$

  - Noise is distributed over the Nyquist band $-f_s/2$ *to* $f_s/2$

Oversampled Converters
Baseband Noise

$$S_B = \int_{-f_B}^{f_B} N_e(f)\,df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\,df$$

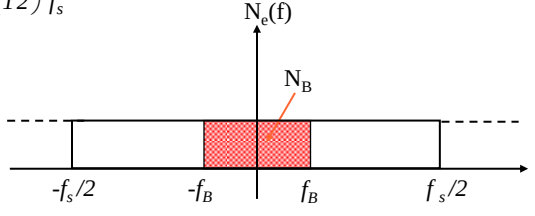
$$= \frac{\Delta^2}{12}\left(\frac{2f_B}{f_s}\right)$$

where for $f_B = f_s/2$

$$S_{B0} = \frac{\Delta^2}{12}$$

$$S_B = S_{B0}\left(\frac{2f_B}{f_s}\right) = \frac{S_{B0}}{M}$$

where $M = \frac{f_s}{2f_B}$ = *oversampling ratio*



Oversampled Converters
Baseband Noise

$$S_B = S_{B0}\left(\frac{2f_B}{f_s}\right) = \frac{S_{B0}}{M}$$

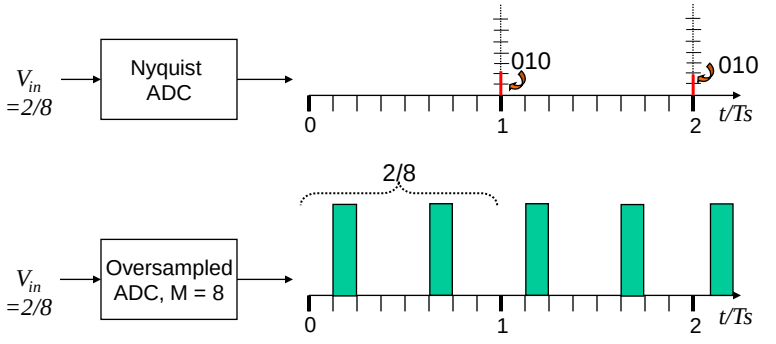
$$where\ M = \frac{f_s}{2f_B} = oversampling\ ratio$$

2X increase in M
- → 3dB reduction in S_B
- → ½ bit increase in resolution/octave oversampling

To further increase the improvement in resolution:

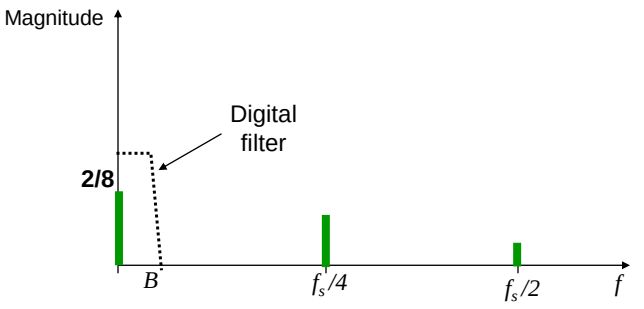
- Embed quantizer in a feedback loop (patented by Cutler in 1960s!)
  - →Noise shaping (sigma delta modulation)

Pulse-Count Modulation



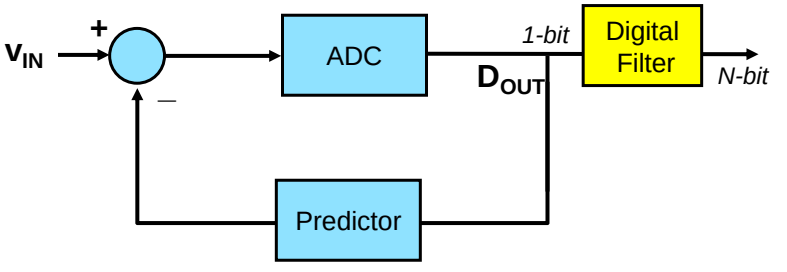
Mean of pulse-count signal approximates analog input!

Pulse-Count Output Spectrum



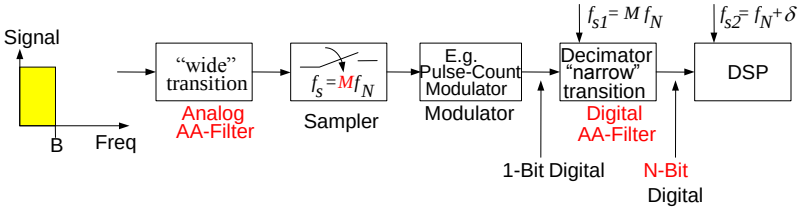
- Signal band of interest: low frequencies, f < B << f_s
- Quantization error: high frequency, B … f_s / 2
- Separate with digital low-pass filter!

Oversampled ADC
Predictive Coding



- Quantize the difference signal rather than the signal itself
- Smaller input to ADC → Buy dynamic range
- Only works if combined with oversampling
- 1-Bit digital output
- Digital filter computes "average" →N-bit output

Oversampled ADC



Decimator:

- Digital (low-pass) filter
- Removes quantization noise for f > B
- Provides anti-alias filtering for DSP
- Narrow transition band, high-order (digital filters with high order consume significantly smaller power & area compared to analog filters)
- 1-Bit input, N-Bit output (essentially computes "average")

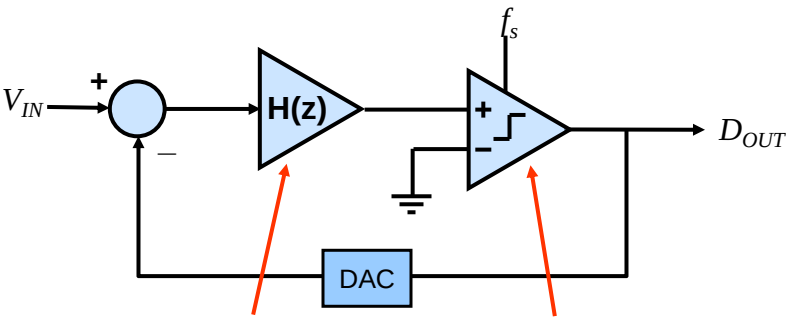
Modulator or Analog Front End (AFE)

- Objectives:
  - Convert analog input to 1-Bit pulse density stream
  - Move quantization error to high frequencies f >>B
  - Operates at high frequency $f_s >> f_N$
    - M = 8 … 256 (typical)….1024
    - Since modulator operated at high frequencies → need to keep analog circuitry "simple"

→ ΣΔ = ΔΣ Modulator

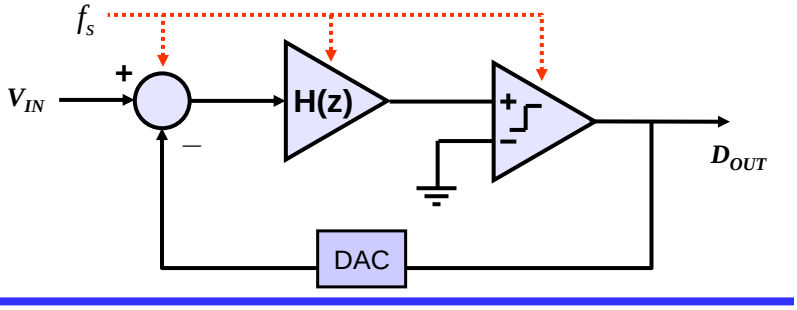
Sigma- Delta Modulators

Analog 1-Bit ΣΔ modulators convert a continuous time analog input v_{IN} into a 1-Bit sequence D_{OUT}

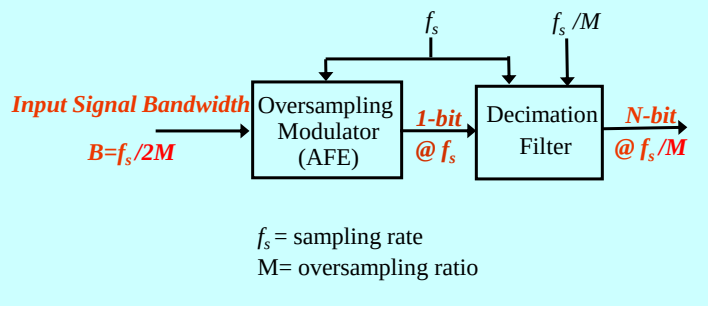


Sigma-Delta Modulators

- The loop filter H can be either switched-capacitor or continuous time
- Switched-capacitor filters are “easier” to implement + frequency characteristics scale with clock rate
- Continuous time filters provide anti-aliasing protection



Oversampling A/D Conversion

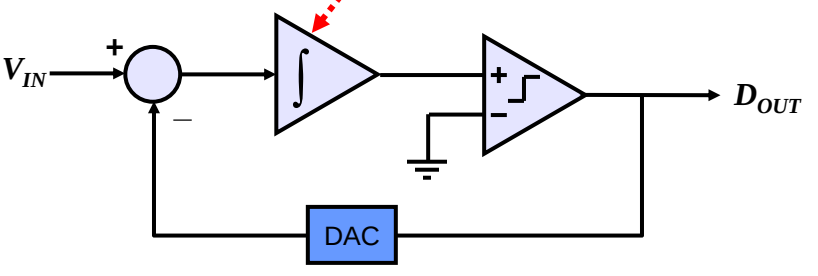


- Analog front-end → oversampled noise-shaping modulator
  - Converts original signal to a 1-bit digital output at the high rate of ($2BXM$)
- Digital back-end → digital filter (decimator)
  - Removes out-of-band quantization noise
  - Provides anti-aliasing to allow re-sampling @ lower sampling rate

1st Order ΣΔ Modulator

1st order modulator, simplest loop filter → an integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$



Note: Non-linear system with memory → difficult to analyze