EE247
Lecture 24

Oversampled ADCs (continued)

- Comparison of limit cycle oscillations 2[nd] order vs 1[st] order ΣΔ modulator

– 2nd order ΣΔ modulator
- Practical implementation
  – Effect of various building block nonidealities on the ΣΔ performance
    - Integrator maximum signal handling capability
    - Integrator finite DC gain
    - Comparator hysteresis (minimum signal handling capability)
    - Integrator non-linearity
    - Effect of KT/C noise
    - Finite opamp bandwidth
    - Opamp slew limited settling
  – Implementation example

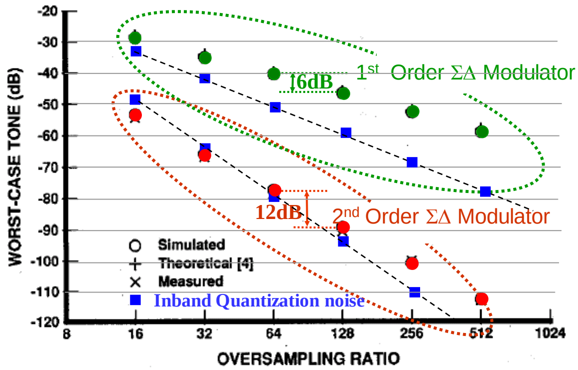
– Higher order ΣΔ modulators
- Cascaded modulators (multi-stage)
- Single-loop single-quantizer modulators with multi-order filtering in the forward path

Limit Cycle Oscillation

- Issue particular to ΣΔ modulator type data converters:
  – In response to low level DC inputs → quantization noise becomes periodic and some of the components could fall with in the passband of interest and thus limit the dynamic range
  – More pronounced in 1[st] order ΣΔ modulators compared to higher order (e.g. 2[nd] order)
- Solution:
  - ➢ Use dithering (inject noise-like signal at the input): to randomize quantization noise
    - If circuit thermal noise is large enough → acts as dither
    - Typically, in the design of ΣΔ modulator integrating C values chosen carefully so that inband thermal noise level exceeds quantization noise

Limit Cycle Tones in 1st Order & 2nd Order ΣΔ Modulator

- Higher oversampling ratio → lower tones
- 2nd order tones much lower compared to 1st
- 2X increase in M decreases the tones by 6dB for 1st order loop and 12dB for 2nd order loop

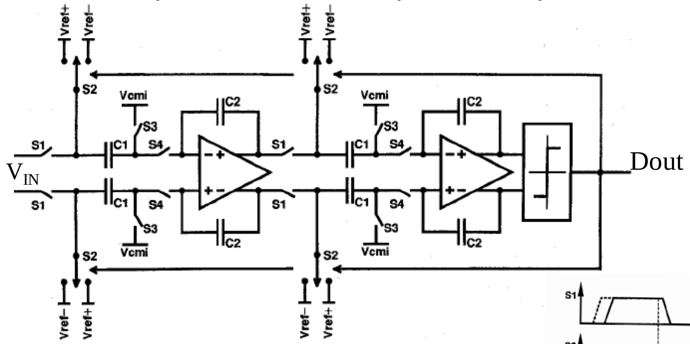


Ref: B. P. Brandt, et al., "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.
R. Gray, "Spectral analysis of quantization noise in a single-loop sigma–delta modulator with dc input," *IEEE Trans. Commun.,* vol. 37, pp. 588–599, June 1989.

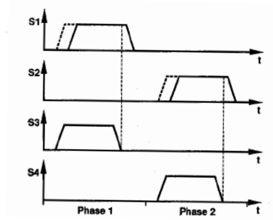
ΣΔ Implementation Practical Design Considerations

- Internal node scaling & clipping
- Effect of finite opamp gain & nonlinearity
- KT/C noise
- Opamp noise
- Finite opamp bandwidth
- Opamp slew limited settling
- Effect of comparator nonidealities
- Power dissipation considerations

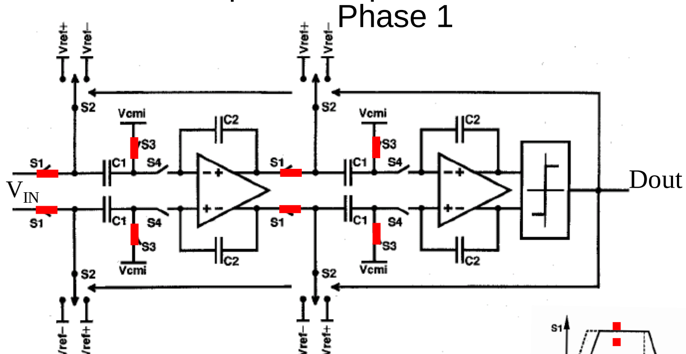
2nd Order ΣΔ Modulator
Example: Switched-Capacitor Implementation



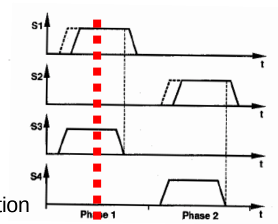
- Fully differential front-end
- Two bottom-plate integrators
- 1-bit DAC is made of switches and Vrefs



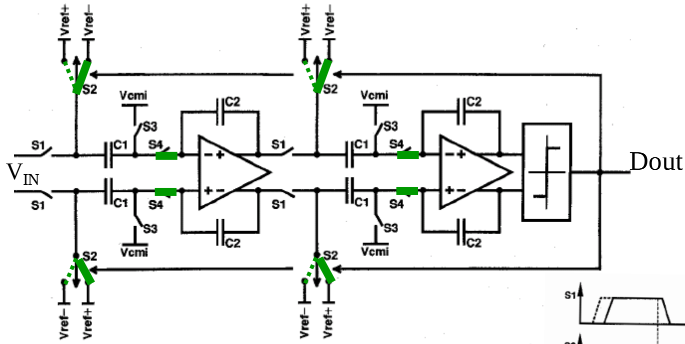
Switched-Capacitor Implementation 2nd Order ΣΔ
Phase 1

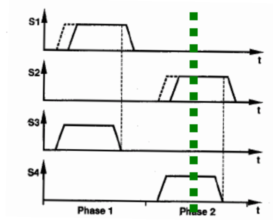


During phase 1:
- 1st integrator samples Vin on 1st stage C1
- 2nd integrator samples output of 1st integrator
- Comparator senses polarity of 2nd intg. output → result saved in output latch
- S3 opens prior to S1 → minimize effect of charge injection



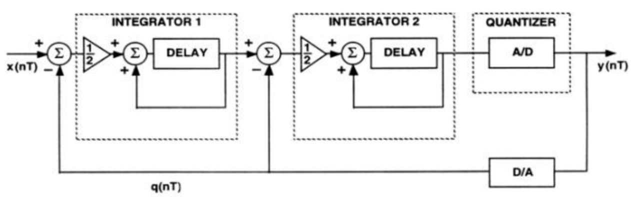
Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Phase 2





- Note: S2 connects integrator inputs to **+** or **–** Vref, polarity depends on whether Dout is **0** or **1**
- Input sampled during ϕ_1 – or + C1xVref transferred to C2 → DAC output subtraction & integration

Switched-Capacitor Implementation 2nd Order $\Sigma\Delta$ Nodes Scaled for Maximum Dynamic Range

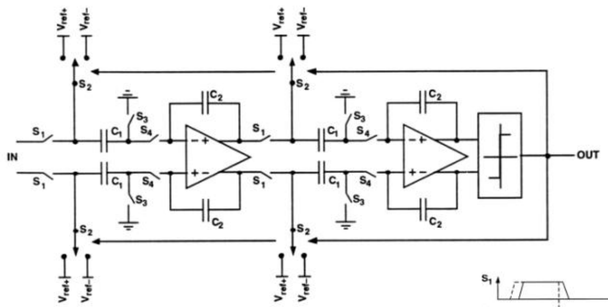


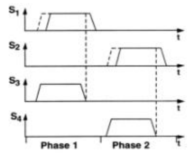
- Modification (gain of ½ in front of integrators) reduce & optimize required signal range at the integrator outputs ~ 1.7x input full-scale (Δ)
- Note: Non-idealities associated with 2nd integrator and quantizer when referred to the $\Sigma\Delta$ input is attenuated by 1st integrator high gain

  → The only building block requiring low-noise and high accuracy is the 1st integrator

Ref: B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation A/D Converters," IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1298-1308, Dec. 1988.

2nd Order ΣΔ Modulator
Switched-Capacitor Implementation





- The ½ loss in front of each integrator implemented by choice of:

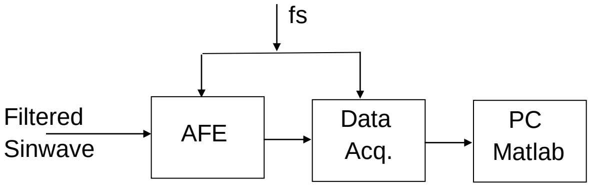
$\boxed{C_2=2C_1}$ $\rightarrow f_0^{intg}=f_s/(4\pi)$

Design Phase Simulations

- Design of oversampled ADCs requires simulation of extremely long data traces due to the oversampled nature of the system
- SPICE type simulators:
  - Normally used to test for gross circuit errors only
  - Too slow for detailed performance verification
- Typically, behavioral modeling is used in MATLAB-like environments
- Circuit non-idealities either computed or found by using SPICE at subcircuit level
- Non-idealities introduced in the behavioral model one-by-one first to fully understand the effect of each individually
- Next step is to add as many of the non-idealities simultaneously as possible to verify whether there are interaction among non-idealities

Testing of AFE

- Typically in the design phase, provisions are made to test the AFE separate from Decimator
- Output of the AFE (0,1) is acquired by a data acquisition board or logic analyzer
- Matlab-like program is used to analyze data e.g. perform filtering & measure SNR, SNDR…..
- During pre-silicon design phase, output of AFE is filtered in software & Matlab used to measure SNR, SNDR

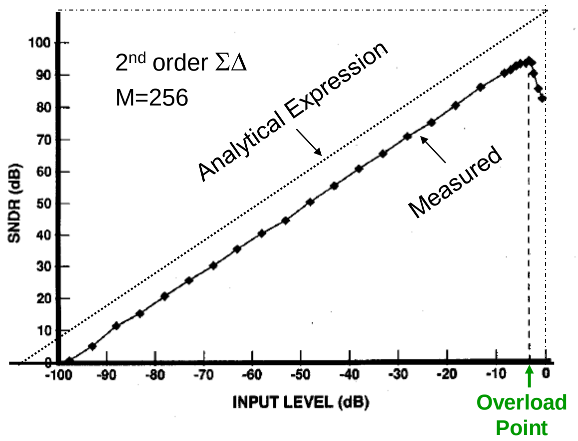


Example: Testing ΣΔ ADC

Note:

The Nyquist ADC tests such as INL and DNL test do not apply to ΣΔ modulator type ADCS

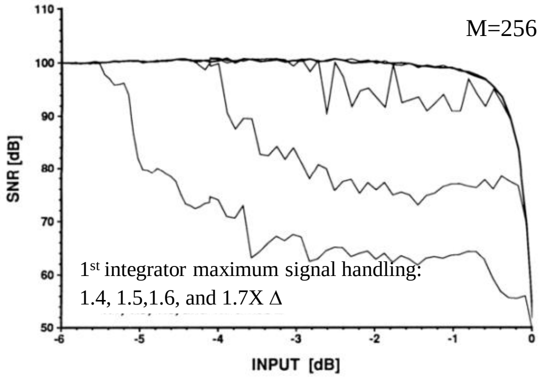
ΣΔ testing is performed via SNDR as a function of input signal level



2^{nd} Order ΣΔ

Effect of 1^{st} Integrator Maximum Signal Handling Capability on SNR

– Behavioral model
– Non-idealities tested one by one

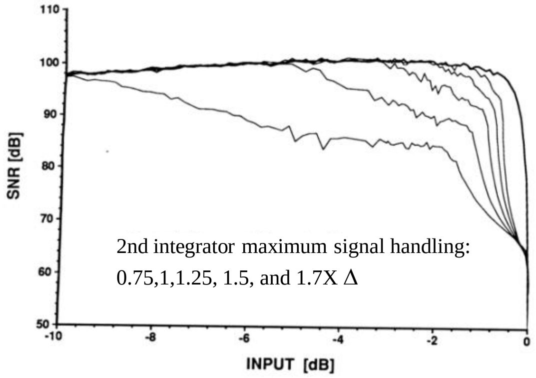


- Effect of 1^{st} Integrator maximum signal handling capability on converter SNR
  → No SNR loss for max. sig. handling >1.7Δ

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2^{nd} Order ΣΔ

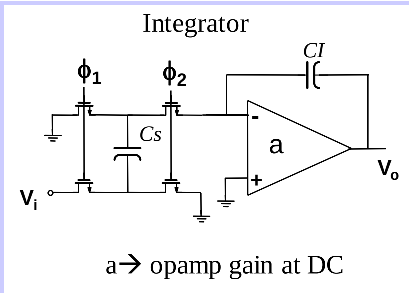
Effect of 2^{nd} Integrator Maximum Signal Handling Capability on SNR



- Effect of 2nd Integrator maximum signal handling capability on SNR
  → No SNR loss for max. sig. handling >1.7 Δ

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2^{nd} Order ΣΔ
Effect of Integrator Finite DC Gain

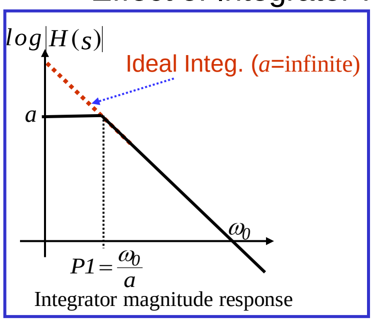


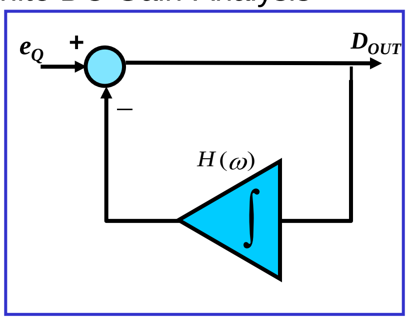
$$H(z)_{ideal} = \frac{Cs}{CI} \times \frac{z^{-1}}{1 - z^{-1}}$$

$$H(z)_{Finit\,DC\,Gain} = \frac{Cs}{CI} \times \frac{\left(\dfrac{a}{1+a+\dfrac{Cs}{CI}}\right) z^{-1}}{1 - \left(\dfrac{1+a}{1+a+\dfrac{Cs}{CI}}\right) z^{-1}}$$

$$\rightarrow H(DC) = a$$

1^{nd} Order ΣΔ
Effect of Integrator Finite DC Gain Analysis





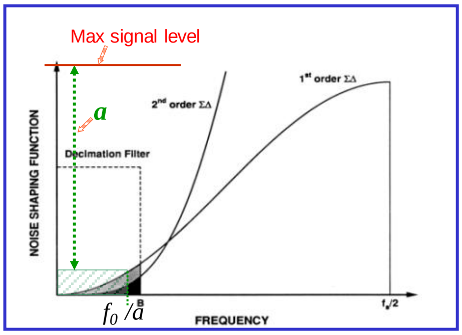
- Note: Quantization transfer function wrt output has integrator in the feedback path:

$$\frac{Dout}{e_Q} = \frac{1}{1+H(\omega)}$$

$$\rightarrow @\ DC\ for\ ideal\ integ:\ \frac{Dout}{e_Q} = 0$$

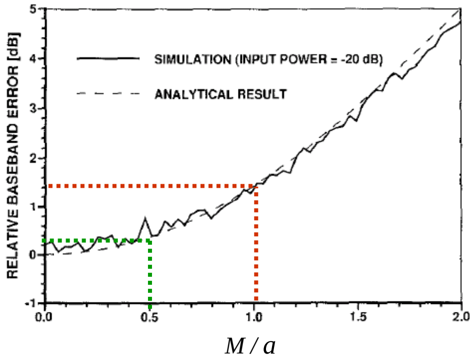
$$\rightarrow @\ DC\ for\ real\ integ:\ \frac{Dout}{e_Q} \approx \frac{1}{a}$$

1^{st} & 2^{nd} Order ΣΔ
Effect of Integrator Finite DC Gain



- Low integrator DC gain → Increase in total in-band quantization noise
- Can be shown: If $a > M$ (oversampling ratio) → Insignificant degradation in SNR
- Normally DC gain designed to be >> M in order to suppress nonlinearities

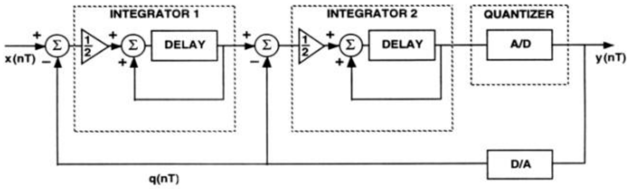
2^{nd} Order ΣΔ
Effect of Integrator Finite DC Gain



- *Example:* $a = 2M$ → 0.4dB degradation in SNR
  $a = M$ → 1.4dB degradation in SNR

Ref: B.E. Boser et. al, “The Design of Sigma-Delta Modulation A/D Converters,” JSSC, Dec. 1988.

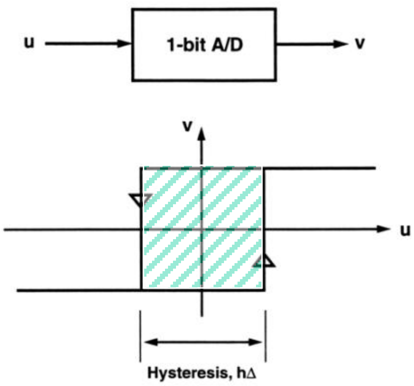
2nd Order ΣΔ
Effect of Comparator Non-Idealities on ΣΔ Performance



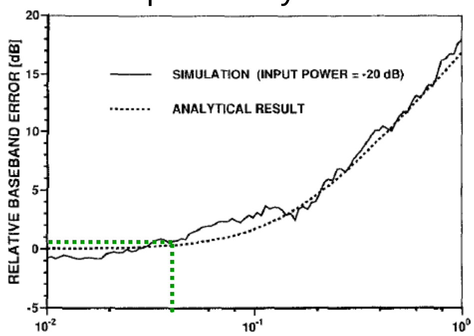
1-bit A/D → Single comparator
- Speed must be adequate for the operating sampling rate
- Input referred offset- feedback loop & high DC intg. gain suppresses the effect
  → ΣΔ performance quite insensitive to comparator offset
- Input referred comparator noise- same as offset
- Hysteresis= Minimum overdrive required to change the output

2nd Order ΣΔ
Comparator Hysteresis

Hysteresis=
Minimum overdrive
required to change
the output



2^{nd} Order ΣΔ
Comparator Hysteresis



Hysteresis/Δ

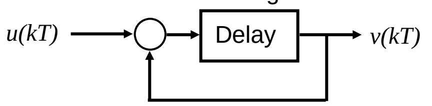
→ Comparator hysteresis < Δ/25 does not affect SNR

→ E.g. Δ=1V, comparator hysteresis up to 40mV tolerable

Key Point: One of the main advantages of ΣΔ ADCS → Highly tolerant of comparator and in general building-block non-idealities

2^{nd} Order ΣΔ
Effect of Integrator Nonlinearities

Ideal Integrator



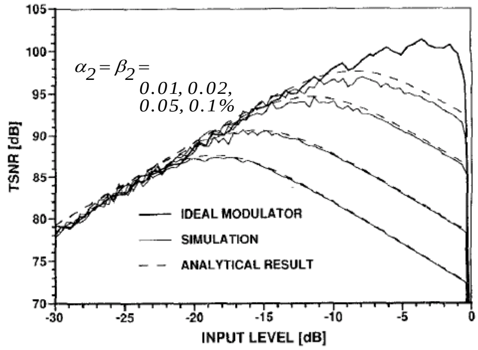
$$v(kT+T)=u(kT)+v(kT)$$

With non-linearity added:

$$v(kT+T)= u(kT)+\alpha_2\left[u(kT)\right]^2+\alpha_3\left[u(kT)\right]^3.....$$
$$+v(kT)+\beta_2\left[v(kT)\right]^2+\beta_3\left[v(kT)\right]^3+....$$

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

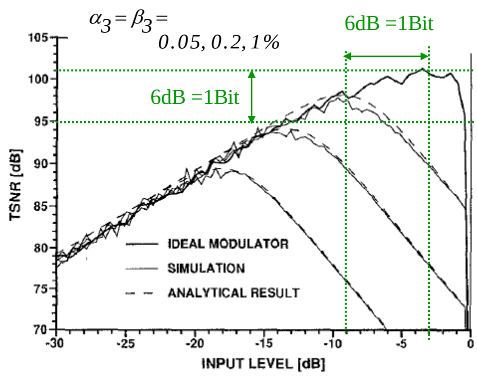
2^{nd} Order ΣΔ
Effect of Integrator Nonlinearities (Single-Ended)



- Simulation for single-ended topology
- Effect of even order nonlinearities can be significantly suppressed by using differential circuit topologies

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2^{nd} Order ΣΔ
Effect of Integrator Nonlinearities



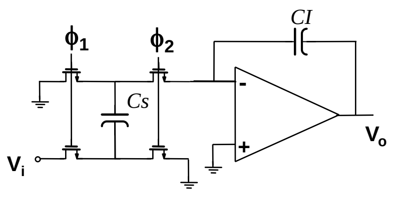
- Simulation for single-ended topology
- Odd order nonlinearities (3^{rd} in this case)

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2^{nd} Order ΣΔ
Effect of Integrator Nonlinearities

- Odd order nonlinearities (usually 3^{rd}) could cause significant loss of SNDR for high resolution oversampled ADCs
- Two significant source of non-linearities:
  - Non-linearities associated with opamp used to build integrators
    - Opamp open-loop non-linearities are suppressed by the loopgain since there is feedback around the opamp
      - Class A opamps tend to have lower open-loop gain but more linear output versus input transfer characteristic
      - Class A/B opamps typically have higher open-loop gain but non-linear transfer function. At times this type is preferred for ΣΔ AFE due to its superior slew rate compared to class A type
    - Integrator capacitor non-linearites
      - Poly-Sio2-Poly capacitors→ C non-linearity in the order of 10ppm/V
      - Metal-Sio2-Metal capacitors ~ 1ppm/V

2^{nd} Order ΣΔ
Effect of Integrator KT/C noise



$$\overline{v_n^2} = \frac{2KT}{Cs}$$

$$\overline{v_n^2} / f = 2\frac{kT}{Cs} \times \frac{1}{fs/2} = 4\frac{kT}{Cs \times fs}$$

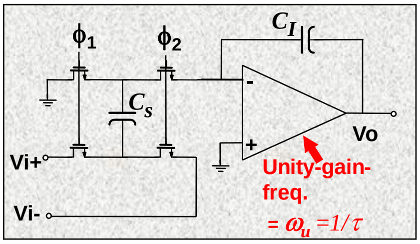
Total in-band noise:

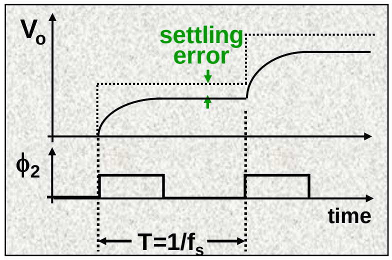
$$\overline{v_n^2}_{\ input-referred} = 4\frac{kT}{Cs \times fs} \times f_B$$

$$= \frac{2kT}{Cs \times M}$$

- For the example of digital audio with *16-bit (96dB)* & *M=256* (*110dB SQNR*)
  - →$Cs=1pF$ → $7\mu Vrms$ noise
  - →If $V_{FS}=2V_{p\text{-}p\text{-}d}$ then thermal noise @ $-101dB$ → degrades overall SNR by ~$9dB$
  - →$Cs=1pF,\ CI=2pF$ →**much smaller capacitor area (~$1/M$) compared to Nyquist ADC**
  - →Since thermal noise provides some level of dithering → better not choose much larger capacitors!

2^{nd} Order ΣΔ
Effect of Finite Opamp Bandwidth



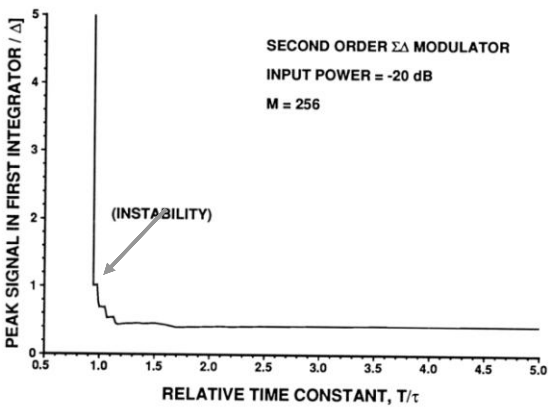


Assumptions:

Opamp → does not slew

Opamp has only one pole → exponential settling

2^{nd} Order ΣΔ
Effect of Finite Opamp Bandwidth

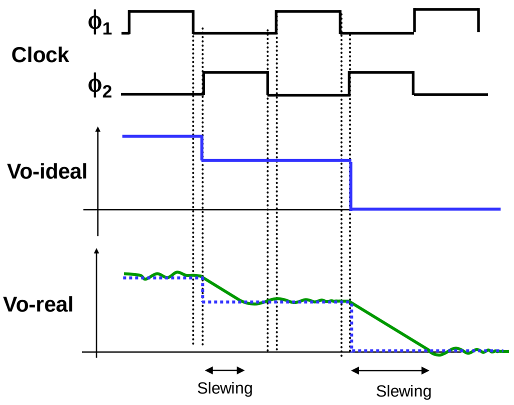


→ ΣΔ does not require high opamp bandwidth $T/\tau > 2$ or $f_u > 2f_s$ adequate

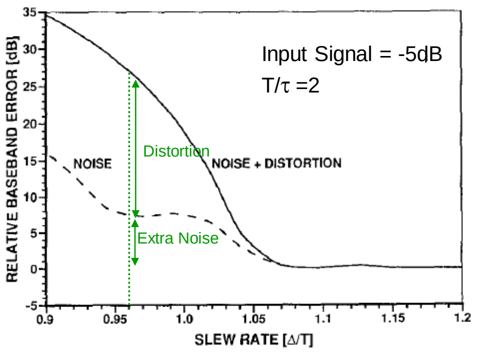
Note: Bandwidth requirements significantly more relaxed compared to Nyquist rate ADCs

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2nd Order ΣΔ
Effect of Slew Limited Settling



2nd Order ΣΔ
Effect of Slew Limited Settling



Assumption:

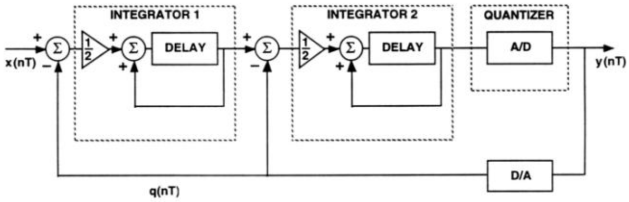
Opamp settling → includes a single-pole setting of $\tau = 1/2f_s$ + slewing

→ Low slew rate degrades SNR rapidly- increases quantization noise and also causes signal distortion

→ Minimum slew rate of $S_R^{min} \sim 1.2\ (\Delta \times f_s)$ required

Ref: B.E. Boser et. al, "The Design of Sigma-Delta Modulation A/D Converters," JSSC, Dec. 1988.

2^{nd} Order ΣΔ
Implementation Example: Digital Audio Application

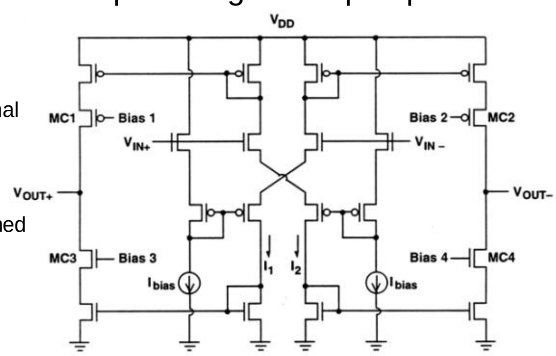


- In Ref.: 5V supply, Δ = 4Vp-p-d, f_s=12.8MHz→ M=256 → theoretical quantization noise @-110dB
- Minimum capacitor values computed based on -104dB noise wrt maximum signal
  - → Max. inband KT/C noise = $7\mu Vrms$ (thermal noise dominates → provide dithering & reduce limit cycle oscillations)
  - → $C1=(2kT)/(M\, v_n^2)=1pF \quad C2=2C1$

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2^{nd} Order ΣΔ
Implementation Example: Integrator Opamp

- Class A/B type opamp → High slew-rate
- S.C. common-mode feedback
- Input referred noise (both thermal and 1/f) important for high resolution performance
- Minimum required DC gain> M=256 , usually DC gain designed to be much higher to suppress nonlinearities (particularly, for class A/B amps)
- Minimum required slew rate of $1.2(\Delta.f_s)$ → 65V/usec
- Minimum opamp settling time constant → 1/2fs~30nsec

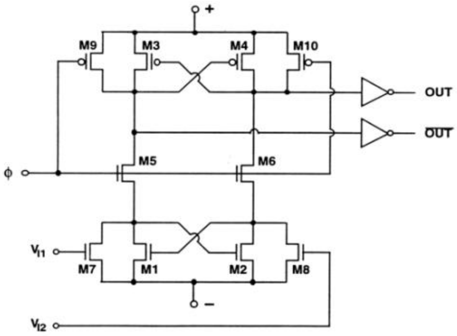


Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2^{nd} Order ΣΔ
Implementation Example: Comparator

- Comparator → simple design
- Maximum acceptable hysteresis or offset (based on analysis) → $\Delta/25 \sim 160$mV
- Have to make sure adequate speed for the chosen sampling freq.

→Since offset requirement not stringent→ No preamp needed, basically a latch with reset



Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2^{nd} Order ΣΔ
Implementation Example: Subcircuit Performance

Subcircuit Performance		Our computed minimum required	Over-Design Factor
Operational Amplifier			
DC gain	**67 dB**	DC Gain 48dB (compensates non-linear open-loop gain)	x8
Unity-gain frequency	**50 MHz**	Unity-gain freq =2fs=25MHz	x2
Slew rate	**350 V/μsec**	Slew rate = 65V/usec	x5
Linear output range	**6 V**	Output range 1.7Δ=6.8V!	X0.9
Sampling rate	**12.8 MHz**		
Integrator			
Settling time constant	**7.25 nsec**	Settling time constant= 30nsec	x4
Comparator			
Offset	**13 mV**	Comparator offset 160mV	x12

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

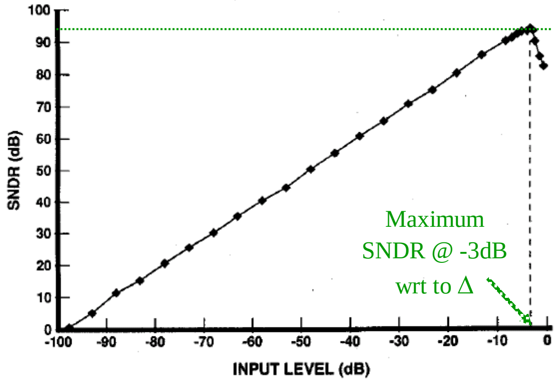
2^{nd} Order ΣΔ
Implementation Example: Digital Audio Applications

Measured SNDR

M=256, 0dB=4$V_{p\text{-}p\text{-}d}$

$f_{sampling}$: 12.8MHz

Test signal frequency: 2.8kHz



Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

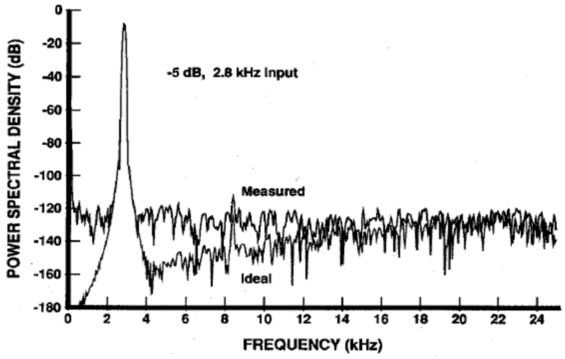
2^{nd} Order ΣΔ
Implementation Example: Digital Audio Applications

Measured Performance Summary
(Does Not Include Decimator)

Dynamic Range	98 dB (16 b)
Peak SNDR	94 dB
Sampling Rate	12.8 MHz
Oversampling Ratio	256
Output Rate	50 kHz
Signal Band	23 kHz
Differential Input Range	4 V
Supply Voltage	5 V
Power Supply Rejection	60 dB
Power Dissipation	13.8 mW
Area	0.39 mm^2
Technology	1-μm CMOS

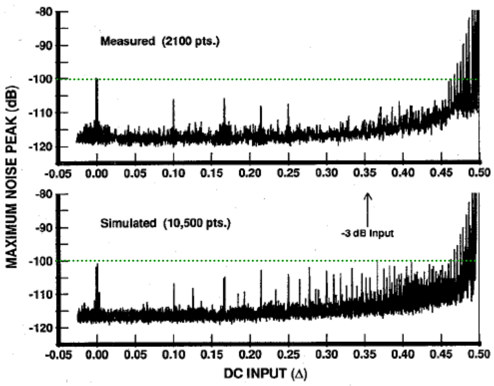
Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2^{nd} Order ΣΔ
Implementation Example: Digital Audio Applications



Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

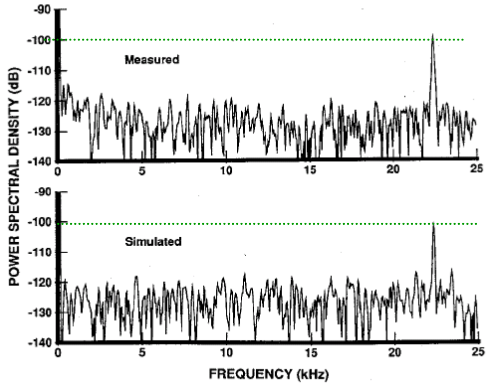
2^{nd} Order ΣΔ
Implementation Example: Digital Audio Applications



→ Measured & simulated in-band spurious tones as a function of DC input signal
→ Sampling rate=12.8MHz, M=256

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

2^{nd} Order ΣΔ
Implementation Example: Digital Audio Applications



→ Measured & simulated worst-case noise tone @ DC input of 0.00088Δ
→ Both indicate maximum tone @ 22.5kHz around -100dB level

Ref: B. P. Brandt, et. al, "Second-order sigma-delta modulation for digital-audio signal acquisition," IEEE Journal of Solid-State Circuits, vol. 26, pp. 618 - 627, April 1991.

Higher Order ΣΔ Modulator Dynamic Range

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^{L} E(z) \quad , \quad L \rightarrow \Sigma\Delta \text{ order}$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2 \qquad \text{sinusoidal input,} \quad STF = 1$$

$$\overline{S_Q} = \frac{\pi^{2L}}{2L+1}\frac{1}{M^{2L+1}}\frac{\Delta^2}{12}$$

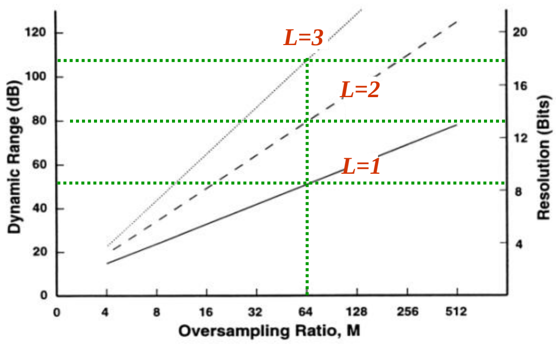
$$\frac{\overline{S_X}}{\overline{S_Q}} = \frac{3(2L+1)}{2\pi^{2L}}M^{2L+1}$$

$$DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}}M^{2L+1}\right]$$

$$\boxed{DR = 10\log\left[\frac{3(2L+1)}{2\pi^{2L}}\right] + (2L+1)\times 10\times \log M}$$

2X increase in M→(*6L+3*)dB or (*L+0.5*)-bit increase in DR

ΣΔ Modulator Dynamic Range As a Function of Modulator Order



- Potential stability issues for L >2

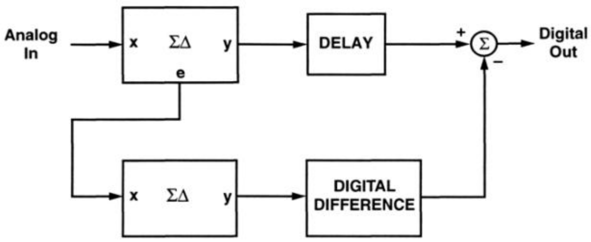
Higher Order ΣΔ Modulators

- Extending ΣΔ Modulators to higher orders by adding integrators in the forward path (similar to 2nd order)
  - → Issues with stability

- Two different architectural approaches used to implement ΣΔ modulators with order >2
  1. Cascade of lower order modulators (multi-stage)
  2. Single-loop single-quantizer modulators with multi-order filtering in the forward path

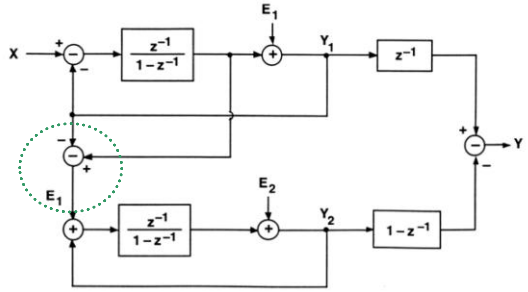
Higher Order ΣΔ Modulators

(1) Cascade of 2-Stages ΣΔ Modulators



- Main ΣΔ quantizes the signal
- The 1st stage quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2nd Order (1-1) Cascaded ΣΔ Modulators



$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$

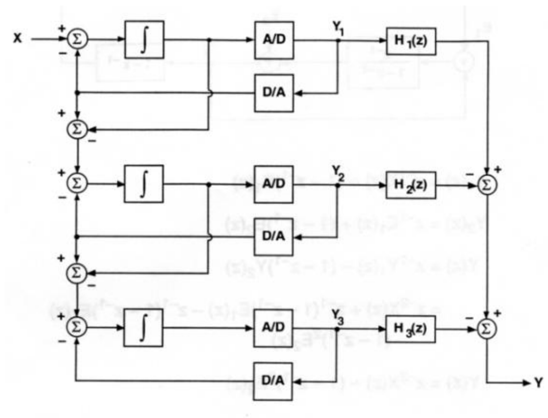
$$= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z) - (1 - z^{-1})^2E_2(z)$$

$$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$$

2nd order noise shaping

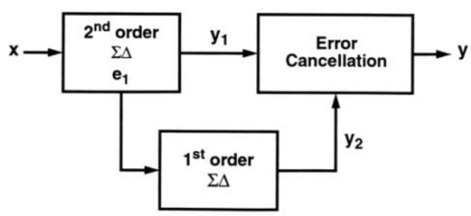
3rd Order Cascaded ΣΔ Modulators
(a) Cascade of 1-1-1 ΣΔs

- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH (multi-stage noise shaping)



3rd Order Cascaded ΣΔ Modulators
(b) Cascade of 2-1 ΣΔs

Advantages of 2-1 cascade compared to 1-1-1-:



- Low sensitivity to matching precision of analog/digital paths
- Low spurious limit cycle tone levels
- No potential instability

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

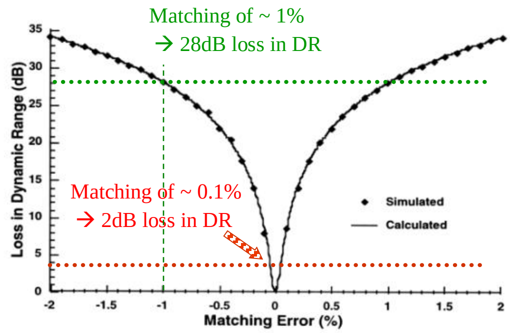
$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

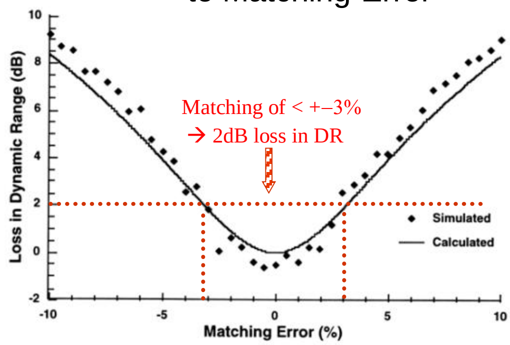
$$= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z) - (1 - z^{-1})^3 E_2(z)$$

3rd order noise shaping $\Rightarrow$ $\boxed{Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)}$

Sensitivity of Cascade of (1-1-1) ΣΔ Modulators to Matching of Analog & Digital Paths



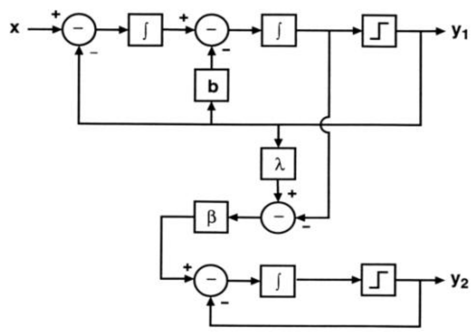
Sensitivity of Cascade of (2-1) ΣΔ Modulators to Matching Error



Main advantage of 2-1 cascade compared to 1-1-1 topology:

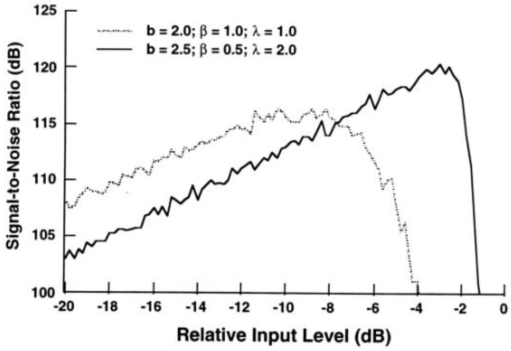
- Low sensitivity to matching of analog/digital paths (in excess of one order of magnitude less sensitive compared to (1-1-1)!)

Example: 2-1 Cascaded ΣΔ Modulators



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

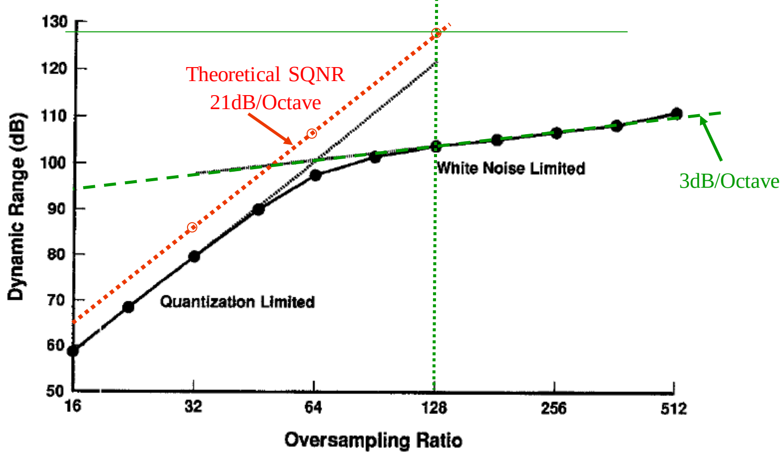
2-1 Cascaded ΣΔ Modulators



Effect of gain parameters on signal-to-noise ratio

Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

2-1 Cascaded ΣΔ Modulators
Measured Dynamic Range Versus Oversampling Ratio



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

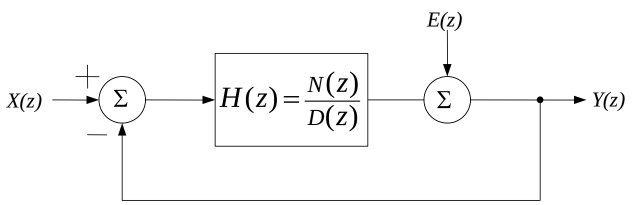
Comparison of 2nd order & Cascaded (2-1) ΣΔ Modulator Test Results

Digital Audio Application, f_N =44.1kHz *(Does not include Decimator)*		
Reference	Brandt ,JSSC 4/91	Williams, JSSC 3/94
Architecture	*2nd order*	*(2+1) Order*
Dynamic Range	*98dB (16-bits)*	*104dB (17-bits)*
Peak SNDR	*94dB*	*98dB*
Oversampling rate	*256 (theoretical → SQNR=109dB, 18bit)*	*128 (theoretical → SQNR=128dB, 21bit!)*
Differential input range	*4Vppd* *5V supply*	*8Vppd* *5V supply*
Power Dissipation	*13.8mW*	*47.2mW*
Active Area	*0.39mm²* (1μ tech.)	*5.2mm²* (1μ tech.)

Higher Order ΣΔ Modulators
(1) Cascaded Modulators Summary

- Cascade two or more stable ΣΔ stages
- Quantization error of each stage is quantized by the succeeding stage/s and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog/digital signal paths
- Quantization noise further randomized → less limit cycle oscillation problems
- Typically, no potential instability

Higher Order Lowpass ΣΔ Modulators
(2)Forward Path Multi-Order Filter



$$Y(z)=\frac{H(z)}{1+H(z)}X(z)+\frac{1}{1+H(z)}E(z)$$

$$NTF=\frac{Y(z)}{E(z)}=\frac{1}{1+H(z)}=\frac{D(z)}{D(z)+N(z)}$$

- Zeros of *NTF* (poles of *H(z)*) can be positioned to minimize baseband noise spectrum
- Approach: Design NTF first and solve for H(z)

- Main issue → Ensuring stability for 3rd and higher orders

5^{th}-order ΣΔ Modulator Design

- Procedure
  - Establish requirements
  - Design noise-transfer function, NTF
  - Determine loop-filter, H
  - Synthesize filter
  - Evaluate performance,
  - Establish stability criteria
  - Voltage scaling
  - Effect of component non-idealities

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters- S. Norsworthy et al. (eds), IEEE Press, 1997

Example: Modulator Specification

- Example: Audio ADC

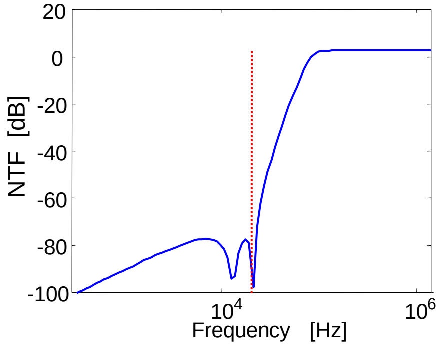
– Dynamic range	DR	18 Bits
– Signal bandwidth	B	20 kHz
– Nyquist frequency	f_N	44.1 kHz
– Modulator order	L	5
– Oversampling ratio	$M = f_s/f_N$	64
– Sampling frequency	f_s	2.822 MHz

- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB

Noise Transfer Function, NTF(z)

```
% stop-band attenuation Rstop=80dB, L=5 ...
L=5;
Rstop = 80;
B=20000;
[b,a] = cheby2(L, Rstop, B, 'high');

NTF = filt(b, a, ...);
```

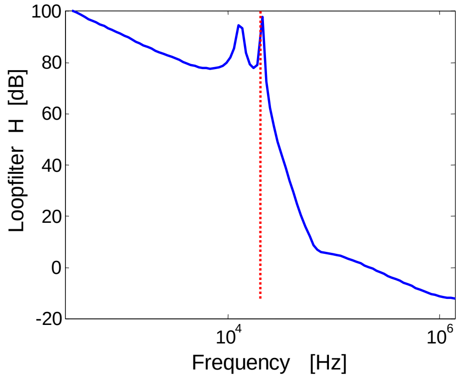


Chebychev II filter chosen
→ zeros in stop-band

Loop-Filter Characteristics H(z)

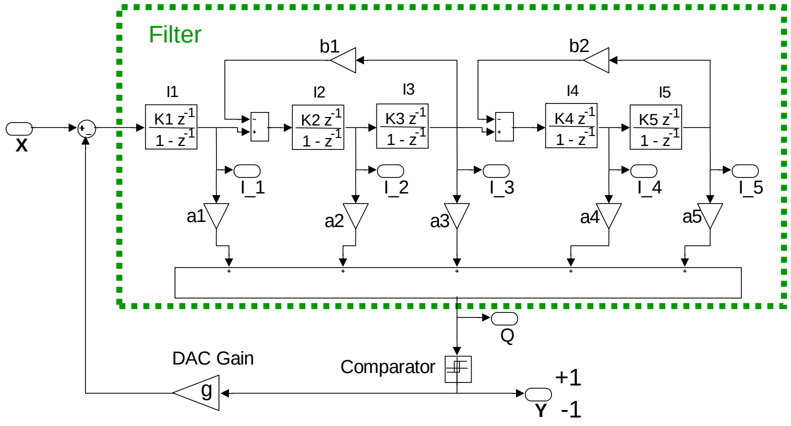
$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

$$\rightarrow H(z) = \frac{1}{NTF} - 1$$



Note: For 1st order $\Sigma\Delta$ an integrator is used instead of the high order filter shown

Modulator Topology Simulation Model

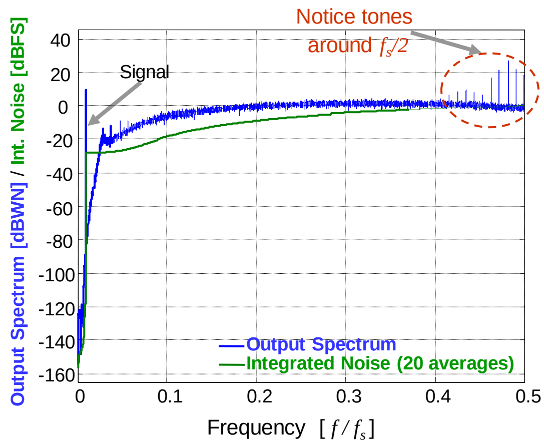


Filter Coefficients

a1=1;	k1=1;	b1=1/1024;
a2=1/2;	k2=1;	b2=1/16-1/64;
a3=1/4;	k3=1/2;	
a4=1/8;	k4=1/4;	
a5=1/8;	k5=1/8;	g =1;

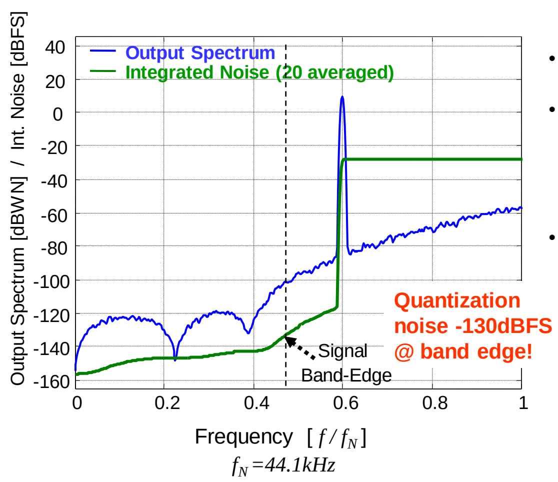
Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1

5th Order Noise Shaping AFE Simulation Results



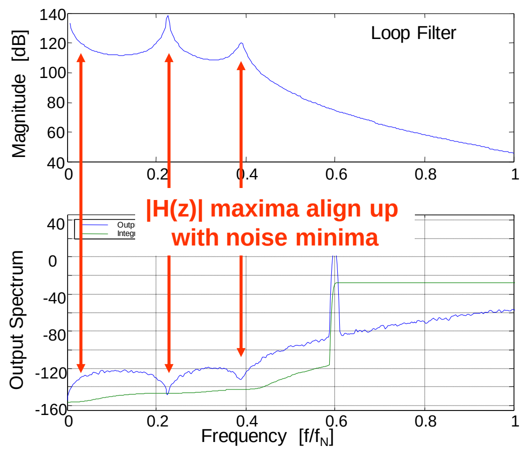
- Mostly quantization noise, except at low frequencies
- Let's zoom into the baseband portion…

5th Order Noise Shaping



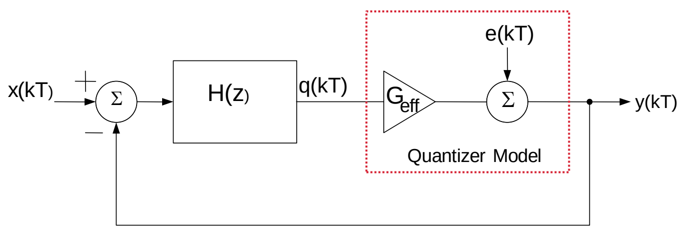
- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise are allowed to dominate & thus provide dithering to eliminate limit cycle oscillations

In-Band Noise Shaping



- Lot's of gain in the loop filter pass-band
- Forward path filter not necessarily stable!
- Remember that:
  - ✓NTF ~ 1/H→ small within passband since H is large
  - ✓STF=H/(1+H) → ~1 within passband

Stability Analysis



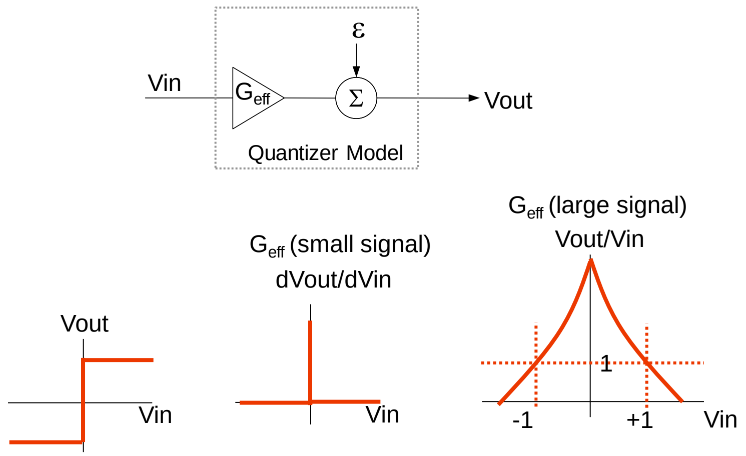
- Approach: linearize quantizer and use linear system theory!
- One way of performing stability analysis→ use RLocus in Matlab with H(z) as argument and Geff as variable
- Effective quantizer gain

$$G_{eff}^2 = \overline{y^2} \Big/ \overline{q^2}$$

- Can obtain G_{eff} from simulation

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters- S. Norsworthy et al. (eds), IEEE Press, 1997

Quantizer Gain (G_{eff})



Stability Analysis

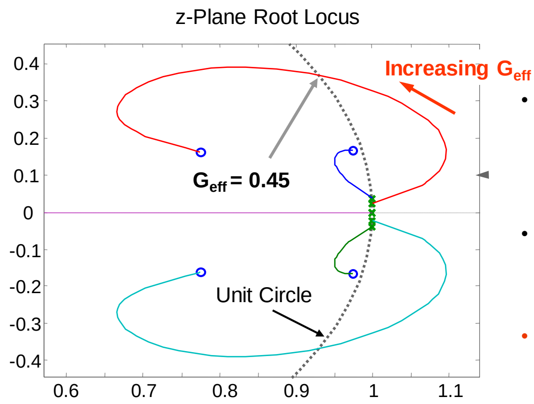
$$STF = \frac{G \cdot H(z)}{1 + G \cdot H(z)}$$

$$H(z) = \frac{N(z)}{D(z)}$$

$$\rightarrow STF = \frac{G \cdot N(z)}{D(z) + G \cdot N(z)}$$

- Zeros of STF same as zeros of H(z)
- Poles of STF vary with G
- For G=small (no feedback) poles of the STF same as poles of H(z)
- For G=large, poles of STF move towards zeros of H(z)
- Draw root-locus: for G values for which poles move to LHP (s-plane) or inside unit circle (z-plane) → system is stable

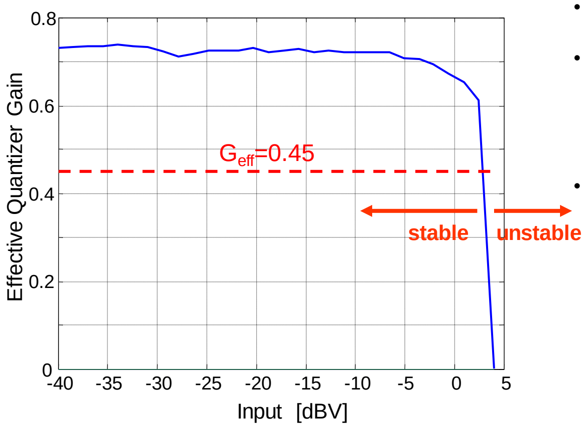
Modulator z-Plane Root-Locus



- As G_{eff} increases, poles of STF move from
  - poles of H(z) (G_{eff} = 0) to
  - zeros of H(z) (G_{eff} = ∞)
- Pole-locations inside unit-circle correspond to stable STF and NTF
- Need G_{eff} > 0.45 for stability

– Note: Final exam does NOT include Root Locus

Effective Quantizer Gain, Geff



- Large inputs → comparator input grows
- Output is fixed (±1)
  → G_{eff} drops
  → modulator unstable for large inputs
- Solution:
  - Limit input amplitude
  - Detect instability (long sequence of +1 or -1) and reset integrators
  - Be ware that signals grow slowly for nearly stable systems → use long simulations