EE247
Lecture 25

Oversampled ADCs (continued)

- Higher order ΣΔ modulators
  - Last lecture→ Cascaded ΣΔ modulators (MASH) (continued)
  - Single-loop single-quantizer modulators with multi-order filtering in the forward path
    - Example: 5th order Lowpass ΣΔ
      - Modeling
      - Noise shaping
      - Effect of various nonidealities on the ΣΔ performance
  - Bandpass ΣΔ modulators

EE247
Lecture 25

•Administrative

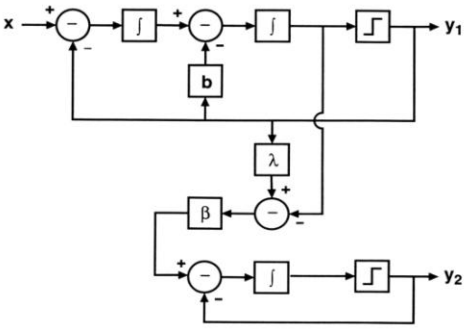
- Final exam:
  - Date: Tues. Dec. 14th
  - Time: 8am-11am
  - Location: 299 Cory (change of location)
  - Closed book/course notes
  - No calculators/cell phones/PDAs/Computers
  - You can bring two 8x11 paper with your own notes
  - Final exam covers the entire course material unless specified

EE247
Lecture 25

Project:

- Project reports due today
- Please make an appointment with the instructor via sign-up sheet for a 20 minute meeting per team for Wed. Dec. 1th
- Prepare to give a 10 minute presentation regarding the project during the class period on Dec. 2nd /Dec. 7th
  - Highlight the important aspects of your approach towards the implementation of the ADC – teach us
  - If the project is joint effort, both team members should present
  - Email your PowerPoint presentation files to the instructor two hours prior to class to be put in one presentation file in order to conserve class time

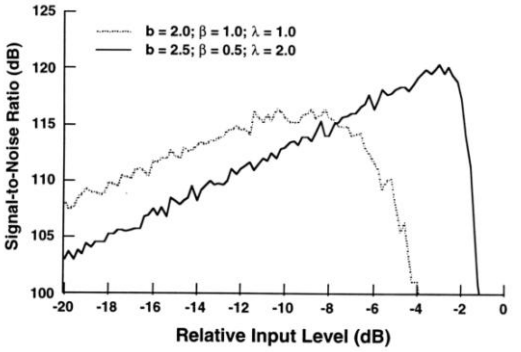
Example: 2-1 Cascaded ΣΔ Modulators



- Various combinations of variables b, λ, β can be used
- Authors have explored combination resulting in max. DR

Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

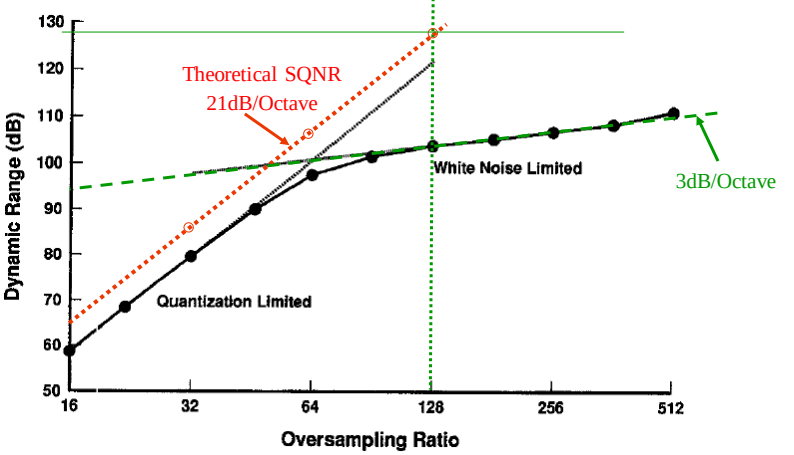
2-1 Cascaded ΣΔ Modulators



Effect of gain parameters on signal-to-noise ratio

Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

2-1 Cascaded ΣΔ Modulators
Measured Dynamic Range Versus Oversampling Ratio



Ref: L. A. Williams III and B. A. Wooley, "A third-order sigma-delta modulator with extended dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 193 - 202, March 1994.

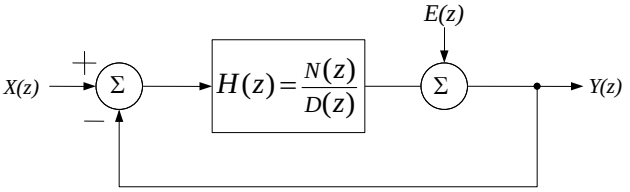
Comparison of 2nd order & Cascaded (2-1) ΣΔ Modulator Test Results

Digital Audio Application, $f_N = 44.1kHz$ *(Does not include Decimator)*		
Reference	Brandt ,JSSC 4/91	Williams, JSSC 3/94
Architecture	*2nd order*	*(2+1) Order*
Dynamic Range	*98dB (16-bits)*	*104dB (17-bits)*
Peak SNDR	*94dB*	*98dB*
Oversampling rate	*256 (theoretical → SQNR=109dB, 18bit)*	*128 (theoretical → SQNR=128dB, 21bit!)*
Differential input range	*4Vppd* *5V supply*	*8Vppd* *5V supply*
Power Dissipation	*13.8mW*	*47.2mW*
Active Area	*0.39mm²* (1μ tech.)	*5.2mm²* (1μ tech.)

Higher Order ΣΔ Modulators (1) Cascaded Modulators Summary

- Cascade two or more stable ΣΔ stages
- Quantization error of each stage is quantized by the succeeding stage/s and subtracted digitally
- Order of noise shaping equals sum of the orders of the stages
- Quantization noise cancellation depends on the precision of analog/digital signal paths
- Quantization noise further randomized → less limit cycle oscillation problems
- Typically, no potential instability

Higher Order Lowpass ΣΔ Modulators
(2) Forward Path Multi-Order Filter



$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z)$$

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = \frac{D(z)}{D(z)+N(z)}$$

- Zeros of NTF (poles of $H(z)$) can be positioned to minimize baseband noise spectrum
- Approach: Design NTF first and solve for H(z)
- Main issue → Ensuring stability for 3rd and higher orders

High Order ΣΔ Modulator Design

- Procedure
  - Establish requirements & determine order
  - Design noise-transfer function, NTF
  - Determine loop-filter, H
  - Synthesize filter
  - Evaluate performance
  - Establish stability criteria
  - Node voltage scaling for maximum DR
  - Effect of component non-idealities

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters- S. Norsworthy et al. (eds), IEEE Press, 1997

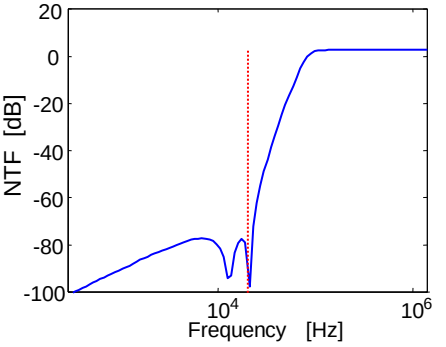
Example: Modulator Specification

- Example: Audio ADC
  - Dynamic range — DR — 18 Bits
  - Signal bandwidth — B — 20 kHz
  - Nyquist frequency — f_N — 44.1 kHz
  - Modulator order — L — 5
  - Oversampling ratio — $M = f_s/f_N$ — 64
  - Sampling frequency — f_s — 2.822 MHz
- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB

Noise Transfer Function, NTF(z)

```
% stop-band attenuation Rstop=80dB, L=5 ...
L=5;
Rstop = 80;
B=20000;
[b,a] = cheby2(L, Rstop, B, 'high');
NTF = filt(b, a, ...);
```

Chebychev II filter chosen
→ zeros in stop-band

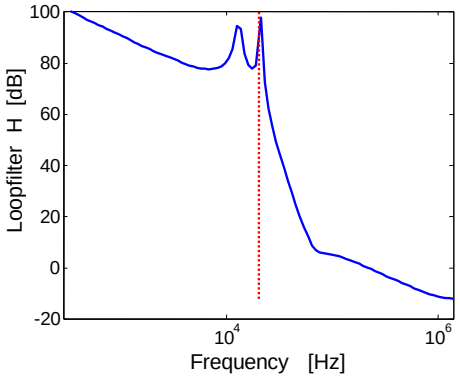


Loop-Filter Characteristics H(z)

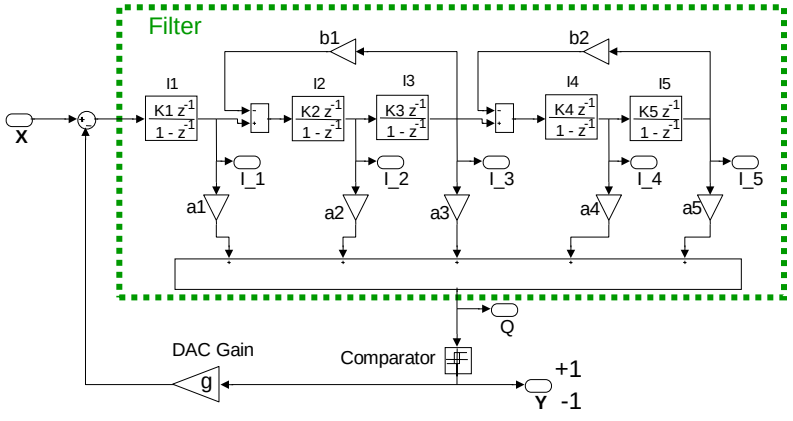
$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

$$\rightarrow H(z) = \frac{1}{NTF} - 1$$

Note: For 1st order ΣΔ an integrator is used instead of the high order filter shown



Modulator Topology Simulation Model



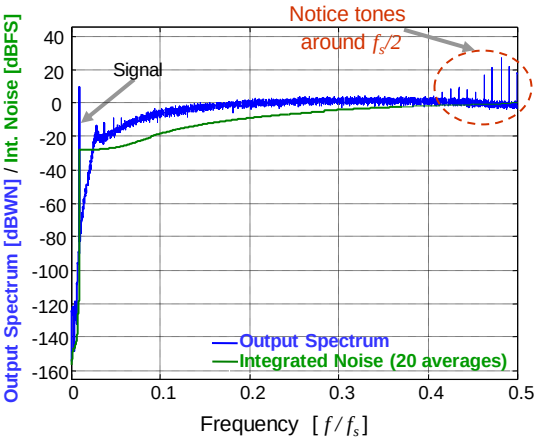
Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, "Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections", U.S. Patent 5061925, 1990, figure 3 and table 1

Filter Coefficients

```
a1=1;          k1=1;          b1=1/1024;
a2=1/2;        k2=1;          b2=1/16-1/64;
a3=1/4;        k3=1/2;
a4=1/8;        k4=1/4;
a5=1/8;        k5=1/8;        g =1;
```

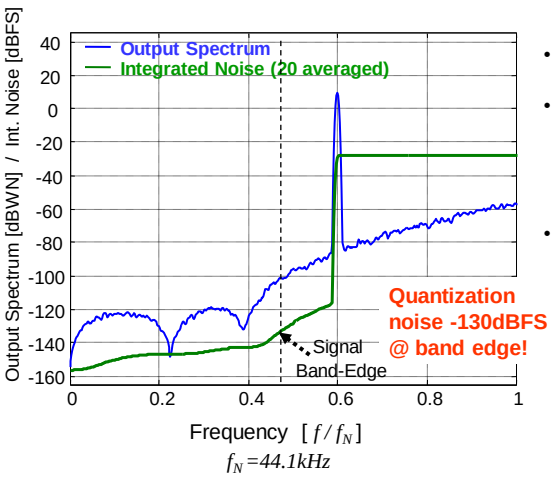
Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, "Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections", U.S. Patent 5061925, 1990, figure 3 and table 1

5th Order Noise Shaping AFE Simulation Results



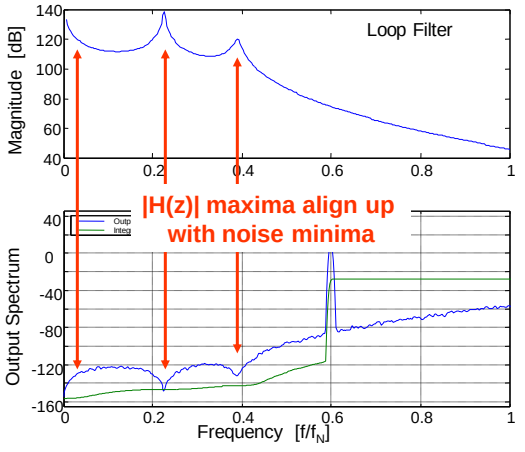
- Mostly quantization noise, except at low frequencies
- Let's zoom into the baseband portion…

5th Order Noise Shaping



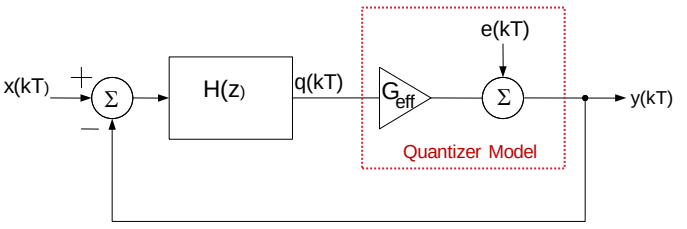
- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise allowed to dominate & thus provide dithering to eliminate limit cycle oscillations

In-Band Noise Shaping



- Lot's of gain in the loop filter pass-band
- Forward path filter not necessarily stable!
- Remember that:
  - ✓NTF ~ 1/H→ small within passband since H is large
  - ✓STF=H/(1+H) → ~1 within passband

Stability Analysis



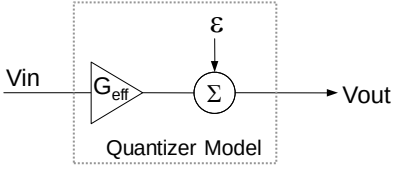
- Approach: linearize quantizer and use linear system theory!
- Effective quantizer gain

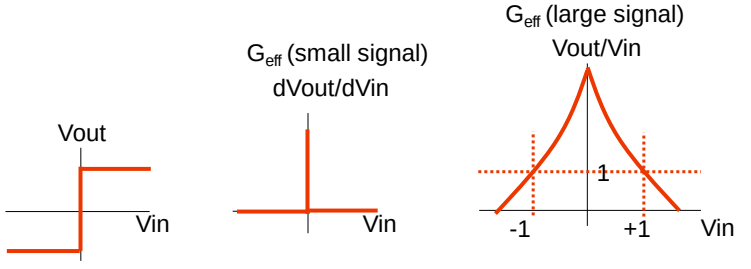
$$G_{eff}^2 = \frac{\overline{y^2}}{\overline{q^2}}$$

- One way of performing stability analysis→ use RLocus in Matlab with H(z) as argument and G_{eff} as variable
- Can obtain G_{eff} from simulation

Ref: R. W. Adams and R. Schreier, "Stability Theory for ΔΣ Modulators," in Delta-Sigma Data Converters- S. Norsworthy et al. (eds), IEEE Press, 1997

Quantizer Gain (G_{eff})





Stability Analysis

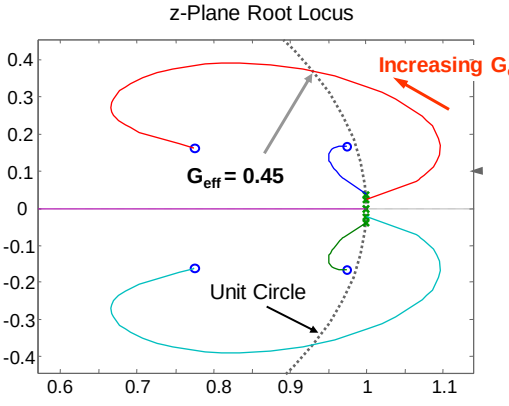
$$STF = \frac{G \cdot H(z)}{1 + G \cdot H(z)}$$

$$H(z) = \frac{N(z)}{D(z)}$$

$$\rightarrow STF = \frac{G \cdot N(z)}{D(z) + G \cdot N(z)}$$

- Zeros of STF same as zeros of H(z)
- Poles of STF vary with G
- For G=small (no feedback) poles of the STF same as poles of H(z)
- For G=large, poles of STF move towards zeros of H(z)
- Draw root-locus: for G values for which poles move to LHP (s-plane) or inside unit circle (z-plane) → system is stable

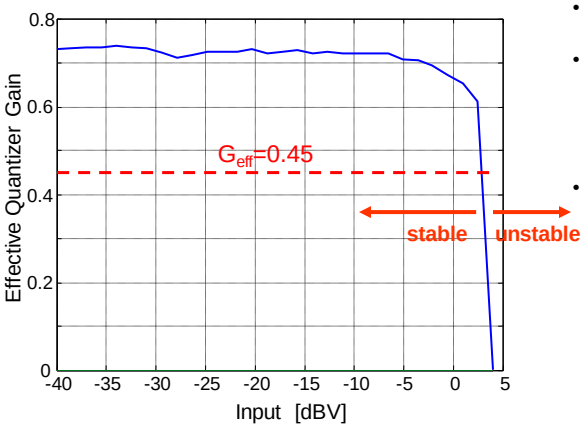
Modulator z-Plane Root-Locus



- As G_{eff} increases, poles of STF move from
  - poles of H(z) (G_{eff} = 0) to
  - zeros of H(z) (G_{eff} = ∞)
- Pole-locations inside unit-circle correspond to stable STF and NTF
- Need G_{eff} > 0.45 for stability

– Note: Final exam does NOT include Root Locus

Effective Quantizer Gain, Geff

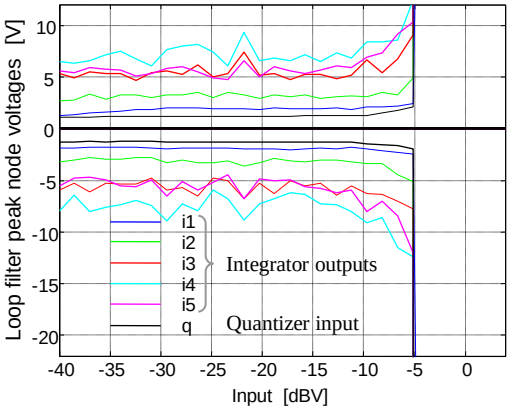


- Large inputs → comparator input grows
- Output is fixed (±1)
  → G_{eff} drops
  → modulator unstable for large inputs

- Solution:
  - Limit input amplitude
  - Detect instability (long sequence of +1 or -1) and reset integrators

  - Be ware that signals grow slowly for nearly stable systems → use long simulations

Internal Node Voltages

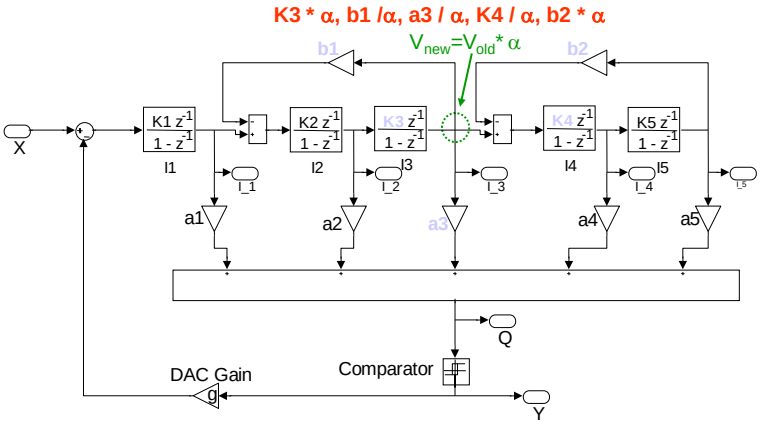


- Internal signal peak amplitudes are weak function of input level (except near overload)

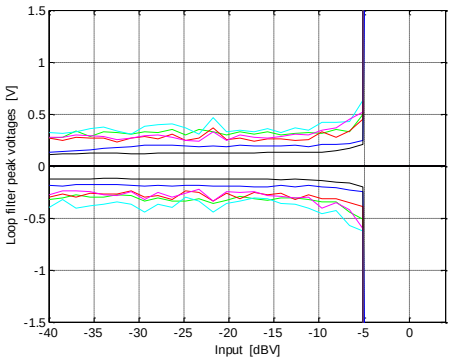
- Maximum peak-to-peak voltage swing approach +-10V! Exceed supply voltage!

- Solution:
  - Node scaling based on max. signal handling capability of integrators

Node Scaling Example:
3rd Integrator Output Voltage Scaled by α



Node Voltage Scaling



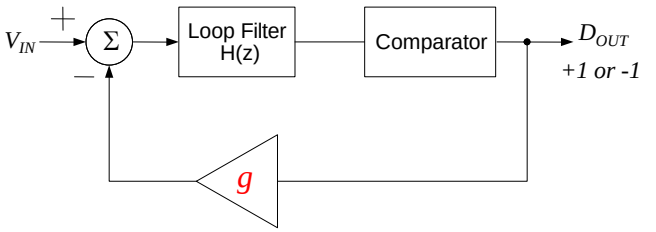
α=1/10
→
k1=1/10;
k2=1;
k3=1/4;
k4=1/4;
k5=1/8;
a1= 1;
a2=1/2;
a3=1/2;
a4=1/4;
a5=1/4;
b1=1/512;
b2=1/16-1/64;
g =1;

- Integrator output range reasonable for new parameters
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?

Input Range Scaling

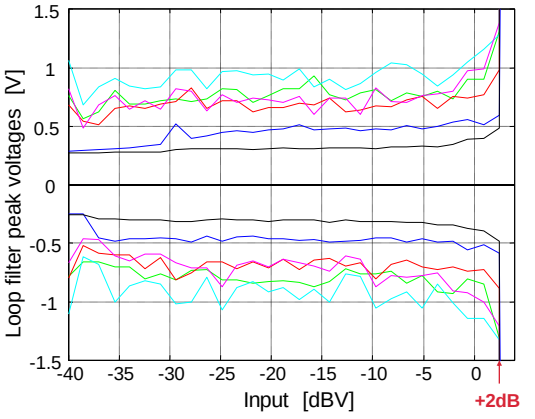
Increasing the DAC levels by using higher value for g reduces the analog to digital conversion gain:

$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{H(z)}{1+gH(z)} \cong \frac{1}{g}$$



Increasing V_{IN} & g by the same factor leaves 1-Bit data unchanged

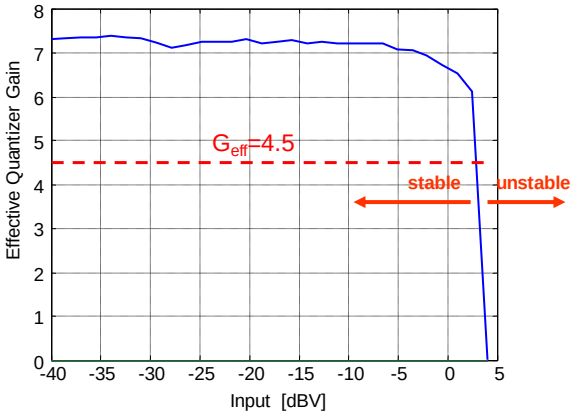
Scaled Stage 1 Model



g modified:
From 1 to 2.5;

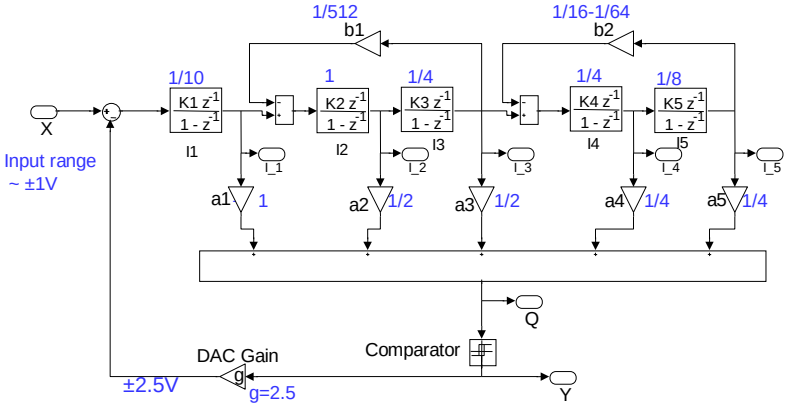
→Overload input level shifted up by ~8dB

Stability Verification
Post Scaling



Note: Operating the AFE at signals <0dBV ensures system stability

5th Order Modulator
Final Parameter Values



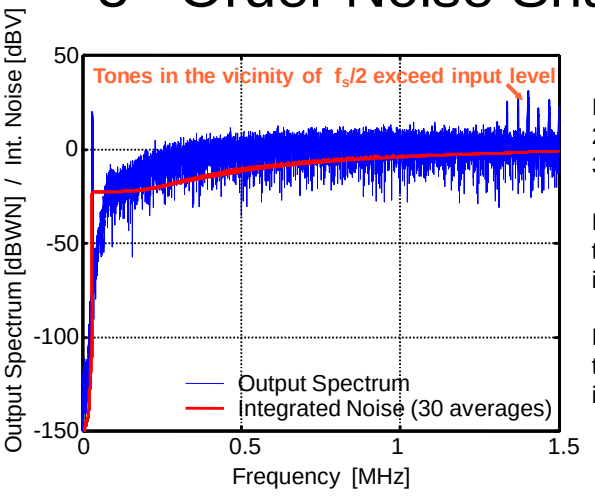
Stable input range with margin ~ ±1V

Summary

- Stage 1 model verified –
  stable and meets SQNR specification

- Stage 2 issues in 5th order ΣΔ modulator
  - DC inputs
  - Spurious tones
  - Dither
  - kT/C noise

5th Order Noise Shaping

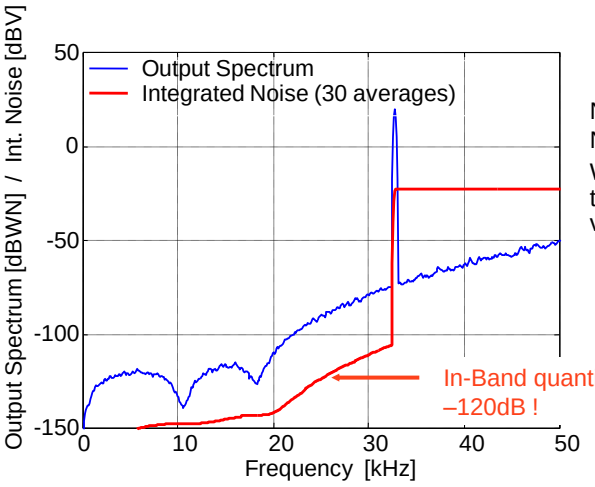


Input: 0.1V, sinusoid
2^{15} point DFT
30 averages

Note: Large spurious tones
in the vicinity of $f_s/2$

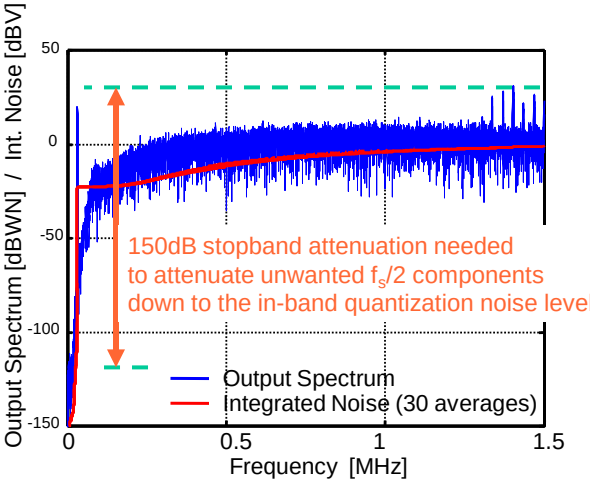
Let us check whether tones appear inband?

In-Band Noise



Note:
No in-band tones!
While Large spurious tones appear in the vicinity of $f_s/2$

5th Order Noise Shaping



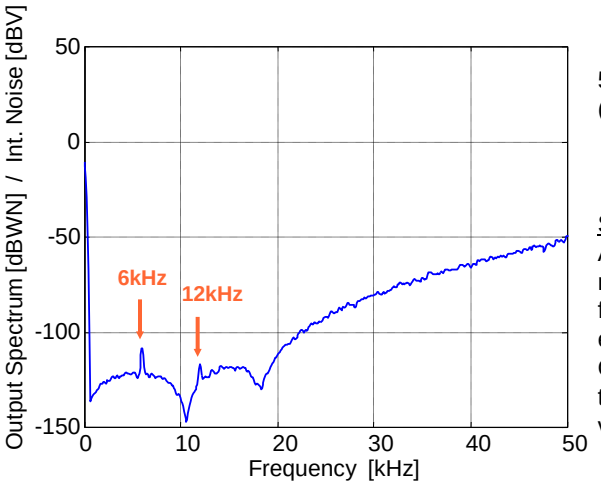
Input: 0.1V, sinusoid
2^{15} point DFT
30 averages

Note: Required digital filter overall out-of-band attenuation function of tones in the vicinity of fs/2 & in-band quantization noise

Out-of-Band vs In-Band Signals

- A digital (low-pass) filter with suitable coefficient precision can eliminate out-of-band quantization noise
- No filter can attenuate unwanted in-band components without attenuating the signal
- Have to make sure that the components at $f_s/2$-f_{in} will not "mix" down to the signal band
  - One possibility: Since DAC is a multiplexer/multiplier small portion of output signal in the vicinity of $f_s/2$-f_{in} could be aliased down to the band of interest.
  - Remedy: Good isolation between DAC Vref and AFE output

ΣΔ Tones Generated by Small DC Input Signals

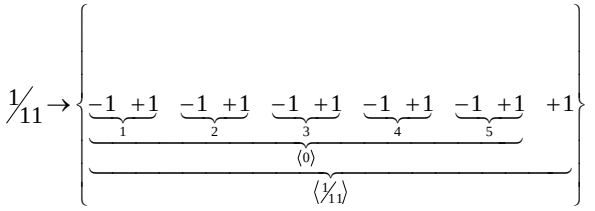


5mV DC input
(V_{DAC} → 2.5V)

Simulation technique:
A random 1st sample randomizes the noise from DC input and enables averaging. Otherwise the small tones will not become visible.

Limit Cycles

- Representing a DC term with a –1/+1 pattern … e.g.



- Spectrum: $\frac{f_s}{11} \quad 2\frac{f_s}{11} \quad 3\frac{f_s}{11} \quad \ldots$

Limit Cycles

- The frequency of the tones are indeed quite predictable
  - Fundamental

$$f_\delta = f_s \frac{V_{DC}}{V_{DAC}} = 3MHz \frac{5mV}{2.5V} = \underline{6kHz}$$

  - Tone velocity (useful for debugging)

$$\frac{df_\delta}{dV_{DC}} = \frac{f_s}{V_{DAC}}$$

$$\frac{df_\delta}{dV_{DC}} = \underline{1.2kHz/mV}$$

  - Note: For digital audio in this case DC signal>20mV generates tone with $f_\delta > 24kHz$ → out-of-band → no problem

Dither

- DC inputs can be represented by many possible bit patterns
- Including some that are random (non-periodic) but still average to the desired DC input
- The spectrum of a non-periodic sequence has no spurious tones
- How can we get a ΣΔ modulator to produce such "randomized" sequences?

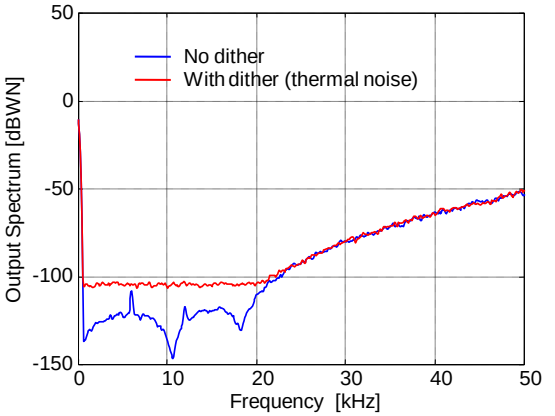
Dither

- The target DR for our audio ΣΔ is 18 Bits, or 113dB
- Designed SQNR~-120dB allows thermal noise to dominate at -115dB level
- Let's choose the sampling capacitor such that it limits the dynamic range:

$$DR = \frac{\frac{1}{2}(V_{FS})^2}{\overline{v_n^2}} \qquad V_{FS} = 1Vp$$

$$\rightarrow \qquad \sqrt{\overline{v_n^2}} = \sqrt{\frac{1}{2DR}}(V_{FS}) = \underline{1\mu V}$$

Effect of Dither on In-Band Spurious Tones



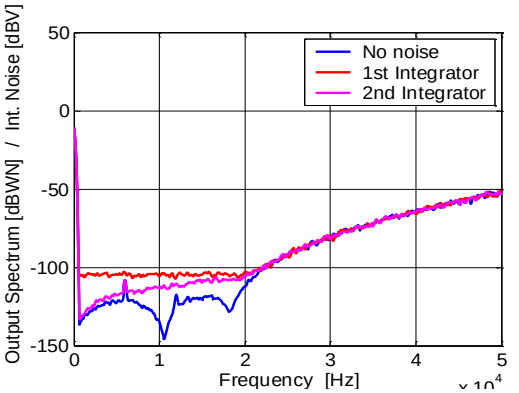
5mV DC input

- Thermal noise added at the input of the 1st integrator
- In-band spurious tones disappear
- Note: they are not just buried
- How can we tell?

kT/C Noise

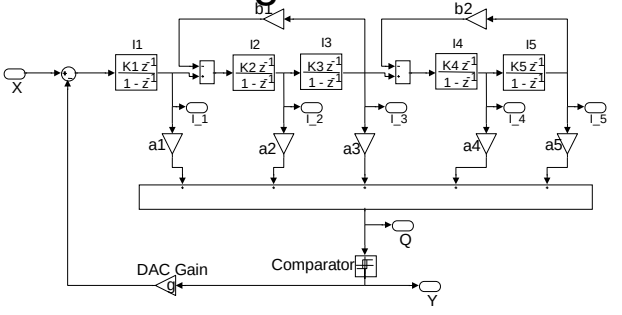
- So far we've looked at noise added to the input of the $\Sigma\Delta$ modulator, which is also the input of the first integrator
- Now let's add noise also to the input of the second integrator
- Let's assume a 1/16 sampling capacitor value for the 2nd integrator wrt the 1st integrator
  - This gives 4μV rms noise

kT/C Noise



- 5mV DC input
- Noise from 2nd integrator smaller than 1st integrator noise shaped
- Why?

Effect of Integrator kT/C Noise

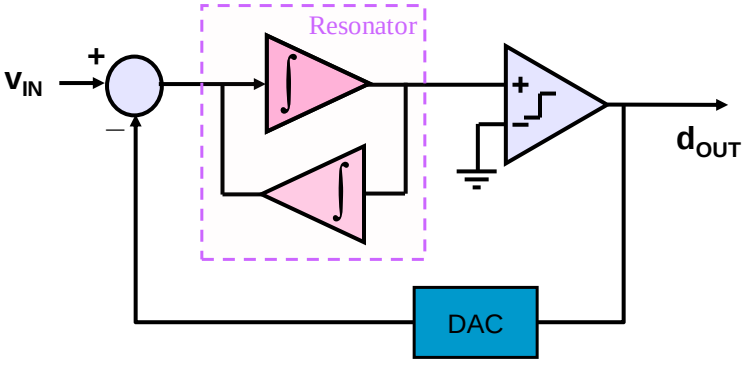


- Noise from 1st integrator is referred directly to the input
- Noise from 2nd integrator is first-order noise shaped
- Noise from subsequent integrators → attenuated even further
  - → Especially for high oversampling ratios, only the first 1 or 2 integrators add significant thermal noise. This is true also for other imperfections (similar to pipelined ADCs!)

Summary

- The model can drive almost all capacitor sizing decisions based on:
  - Gain scaling
  - kT/C noise
  - Dither
- Dither quite effective in the elimination of native in-band tones
- Extremely clean & well-isolated V_{ref} is required for high-dynamic range applications e.g. digital audio

Bandpass ΔΣ Modulator



- Replace the integrator in 1st order lowpass ΣΔ with a resonator

  → 2nd order bandpass ΣΔ

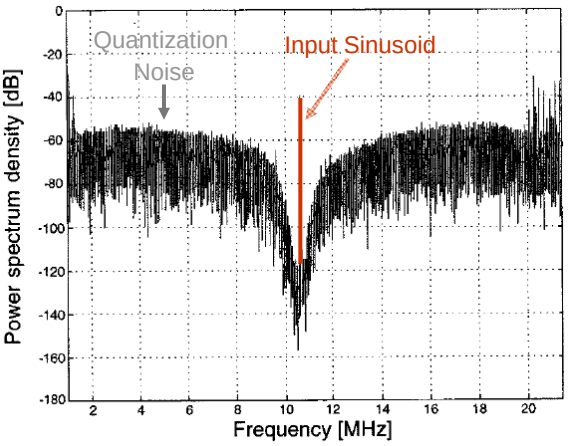
Bandpass ΔΣ Modulator Example: 6th Order

Measured output for a bandpass ΣΔ (prior to digital filtering)

Key Point:

NTF→ notch type shape

STF→ bandpass shape



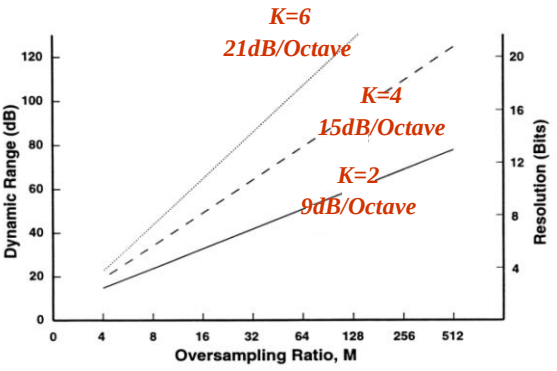
Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

Bandpass ΣΔ Characteristics

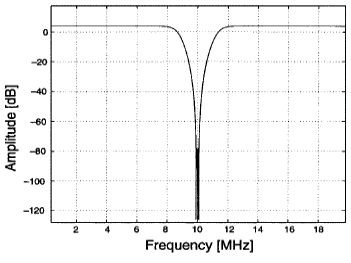
- Oversampling ratio defined as $f_s/2B$ where B = signal bandwidth
- Typically, sampling frequency is chosen to be $f_s=4xf_{center}$ where f_{center}→ bandpass filter center frequency
- STF has a bandpass shape while NTF has a notch or band-reject shape
- To achieve same resolution as lowpass, need twice as many integrators

Bandpass ΣΔ Modulator Dynamic Range As a Function of Modulator Order (K)

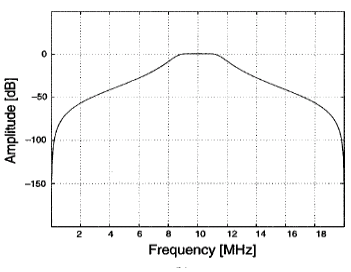


- Bandpass ΣΔ resolution for order K is the same as lowpass ΣΔ resolution with order L= K/2

Example: Sixth-Order Bandpass ΣΔ Modulator



Simulated noise transfer function



Simulated signal transfer function

Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

Example: Sixth-Order Bandpass ΣΔ Modulator

Features & Measured Performance

Analog input full-scale	4.4V (differential)
Sampling frequency (F_S)	42.8MHz ← $f_s=4xf_{center}$
Center frequency (f_0)	10.7MHz
Signal bandwidth	200kHz ← B
OSR	107 ← $OSR=f_s/2B$
Dynamic range	74dB (200kHz band)
	88dB (9kHz band)
Peak SNDR	61dB
IMD (@-15dB)	71dBc
Active die area	$1mm^2$
Power supply	3.3V
Power consumption	76mW (adaptive biasing)
	126mW (standard biasing)
Technology	0.35µm CMOS

Ref:

Paolo Cusinato, et. al, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass Modulator with 74-dB Dynamic Range ", IEEE JSSCC, VOL. 36, NO. 4, APRIL 2001

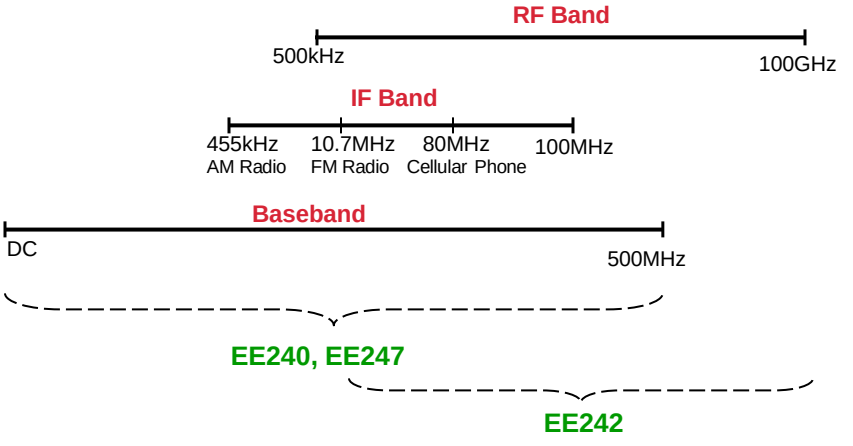
Summary
Oversampled ADCs

- Noise shaping utilized to reduce baseband quantization noise power
- Reduced precision requirement for analog building blocks compared to Nyquist rate converters
- Relaxed transition band requirements for analog anti-aliasing filters due to oversampling
- Takes advantage of low cost, low power digital filtering
- Speed is traded for resolution
- Typically used for lower frequency applications compared to Nyquist rate ADCs

Material Covered in EE247

- Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Interpolating & Folding, Pipeline ADCs,….
    - Self-calibration techniques
    - Oversampled converters

E.E. Circuit Courses vs. Frequency Range



Acknowledgements

- The course notes for EE247 are based on numerous sources including:
  - Prof. P. Gray's EE290 course
  - Prof. B. Boser's EE247 course notes
  - Prof. B. Murmann's Nyquist ADC notes
  - Fall 2004 thru 2009 EE247 class feedback
  - Last but not least, Fall 2010 EE247 class
    - The instructor would like to thank the class of 2010 for their enthusiastic & active participation!