## Lecture 4

When we perform a sequence of computations using a digital circuit, we switch the input voltages between logic 0 and logic 1.


The output of the digital circuit fluctuates between logic 0 and logic 1 as computations are performed.

We compute with pulses
We send beautiful pulses in


But we receive lousy-looking pulses at the output


Capacitor charging effects are responsible!
Every node in a circuit has capacitance to ground, and it's the charging of these capacitances that limits real circuit performance (speed)

## RC Response

Internal Model of Logic Gate


Behavior of $\mathrm{V}_{\text {out }}$ after change in $\mathrm{V}_{\text {in }}$



EECS 40 Spring 2003 Lecture 4

## RC Response Derivation

KCL at node "out":
Current into "out" from the left: $\left(V_{\text {in }}-V_{\text {out }}\right) / R$

Current out of "out" down to ground:


$$
\mathrm{CdV} \mathrm{Vout} / \mathrm{dt}
$$

KCL: $\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) / \mathrm{R}=\mathrm{CdV}$ out $/ \mathrm{dt}$

$$
\begin{gathered}
\text { "Time Constant" } \\
\tau=R C
\end{gathered}
$$

$\rightarrow \quad \frac{\mathrm{d} \mathrm{V}_{\text {out }}}{\mathrm{dt}}=\frac{1}{\mathrm{RC}}\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right)$ (

Solution:

$$
V_{\text {out }}(t)=V_{\text {in }}+\left[V_{\text {out }}(t=0)-V_{\text {in }}\right] e^{-t /(R C)}
$$

## Charging and Discharging

$$
V_{\text {out }}(t)=V_{\text {in }}\left(1-e^{-t / \tau}\right)+V_{\text {out }}(t=0) e^{-t / \tau}
$$

Charging: $V_{\text {in }}>V_{\text {out }}(t=0)$


Discharging: $\mathrm{V}_{\text {in }}<\mathrm{V}_{\text {out }}(\mathrm{t}=0)$

$63 \%$ of transition complete after $1 \tau$

## Common Cases

Transition from logic 0 to logic 1 Transition from logic 1 to logic 0

$$
\begin{array}{cc}
\text { (charging) } & \text { (discharging) } \\
V_{\text {out }}(t)=V_{1}\left(1-e^{-t / \tau}\right) & V_{\text {out }}(t)=V_{1} e^{-t / \tau}
\end{array}
$$

( $\mathrm{V}_{1}$ is logic 1 voltage)



## Charging and discharging in RC Circuits (The official EE40 Easy Method)

## Method of solving for any node voltage in a single capacitor circuit.

1) Simplify the circuit so it looks like one resistor, a source, and a capacitor (it will take another two weeks to learn all the tricks to do this.) But then the circuit looks like this:
2) The time constant is $\tau=\mathrm{RC}$.
3) Solve for the capacitor voltage before the transient, $\mathrm{V}_{\text {out }}(\mathrm{t}=0)$

4) Solve the for asymptotic value of capacitor voltage. Hint: Capacitor eventually conducts no current (dV/dt dies out asymptotically).
5) Sketch the transient. It is $63 \%$ complete after one time constant.
6) Write the equation by inspection.

## Example

$$
\mathrm{R}=1 \mathrm{k} \Omega, \mathrm{C}=1 \mathrm{pF} .
$$

Assume $\mathrm{V}_{\text {in }}$ has been zero for a long time, then steps from zero to 10 V at $\mathrm{t}=0$.


At $t=0$, since $V_{\text {in }}$ has been constant for a long time, the circuit is in "steady-state". Capacitor current is zero (since $\mathrm{dV} / \mathrm{dt}=0$ ), so by KVL, $\operatorname{Vout}(\mathrm{t}=0)=0$.

Asymptotically, the capacitor will have no current, so the capacitor voltage will be equal to $\mathrm{V}_{\text {in }}, 10 \mathrm{~V}$ (resistor will have 0 V ).
The time constant $\tau=\mathrm{RC}=1 \mathrm{~ns}$.
We can plug into the equation and draw the graph $\rightarrow$

$$
V_{\text {out }}(t)=10-10 e^{-t / 1 ~ n s}
$$



## PULSE DISTORTION



## PULSE DISTORTION



The pulse width must be long enough, or we get severe pulse distortion.

We need to reach a recognizable logic level.



## EXAMPLE

Suppose a voltage pulse of width $5 \mu \mathrm{~s}$ and height 4 V is applied to the input of the circuit at the right.

Sketch the output voltage.


First, the output voltage will increase to approach the 4 V input, following the exponential form. When the input goes back down, the output voltage will decrease back to zero, again following exponential form.

How far will it increase? Time constant $=\mathrm{RC}=2.5 \mu \mathrm{~s}$ The output increases for $5 \mu \mathrm{~s}$ or 2 time constants.
It reaches $1-e^{-2}$ or $86 \%$ of the final value.
$0.86 \times 4 \mathrm{~V}=3.44 \mathrm{~V}$ is the peak value.


The equation for the output is:

$$
V_{\text {out }}(t)=\left\{\begin{array}{l}
4-4 \mathrm{e}^{-\mathrm{t} / 2.5 \mu \mathrm{~s}} \text { for } 0 \leq \mathrm{t} \leq 5 \mu \mathrm{~s} \\
3.44 \mathrm{e}^{-(\mathrm{t}-5 \mu \mathrm{~s}) / 2.5 \mu \mathrm{~s}} \text { for } \mathrm{t}>5 \mu \mathrm{~s}
\end{array}\right.
$$

## APPLICATIONS

- Now we can find "propagation delay" $t_{p}$; the time between the input reaching $50 \%$ of its final value and the output to reaching $50 \%$ of final value.
- For instantaneous input transitions between 0 V and logic 1 , $0.5=\mathrm{e}^{-\mathrm{tp}}$
$\mathrm{t}_{\mathrm{p}}=-\ln 0.5=0.69$
It takes 0.69 time constants, or 0.69 RC .
- We can find the time it takes for the output to reach other desired levels. For example, we can find the time required for the output to go from 0 V to the minimum voltage level recognizable as logic 1 (known as $\mathrm{V}_{\mathrm{HH}}$ )
- Knowing these delays helps us design clocked circuits.

