Lecture #14

OUTLINE

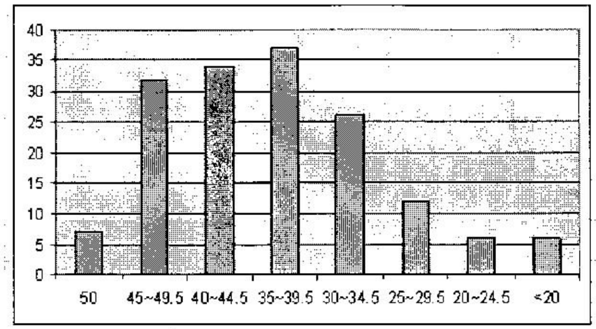
- Midterm #1 stats
- The pn Junction Diode
  - Depletion region & junction capacitance
  - *I-V* characteristic
  - Circuit applications and analysis

Reference Reading

- **Rabaey *et al.***
  - Chapter 3.2.1 to 3.2.2
- **Hambley**
  - Chapter 10.1 to 10.4

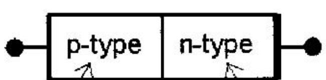
Midterm #1 Statistics

average:	37.8125
standard deviation	8.256644
total students	160
50	7
45~49.5	32
40~44.5	34
35~39.5	37
30~34.5	26
25~29.5	12
20~24.5	6
<20	6

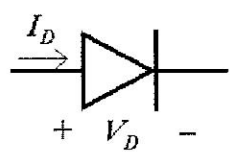


The *pn* Junction Diode

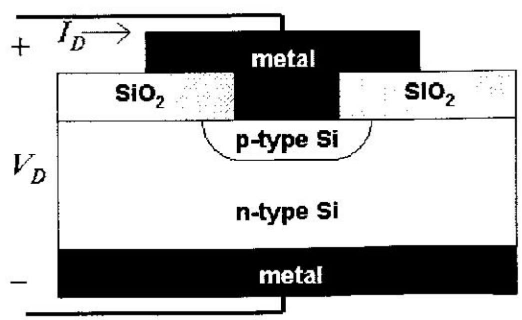
Schematic diagram



Circuit symbol



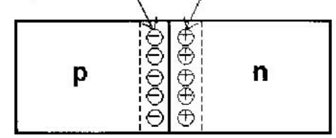
Physical structure:
(an example)



For simplicity, assume that the doping profile changes abruptly at the junction.

Depletion Region

- When the junction is first formed, mobile carriers ***diffuse*** across the junction (due to the concentration gradients)
  - Holes diffuse from the p side to the n side, leaving behind negatively charged acceptor ions
  - Electrons diffuse from the n side to the p side, leaving behind positively charged donor ions

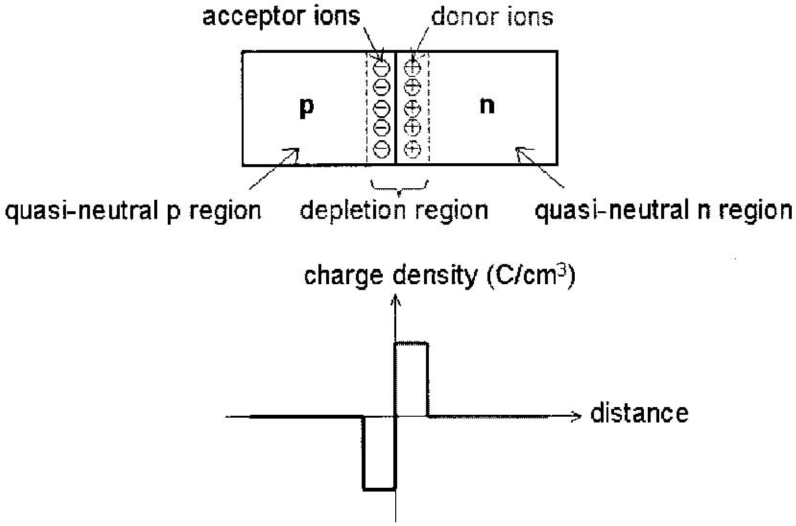


→**A region depleted of mobile carriers is formed at the junction.**

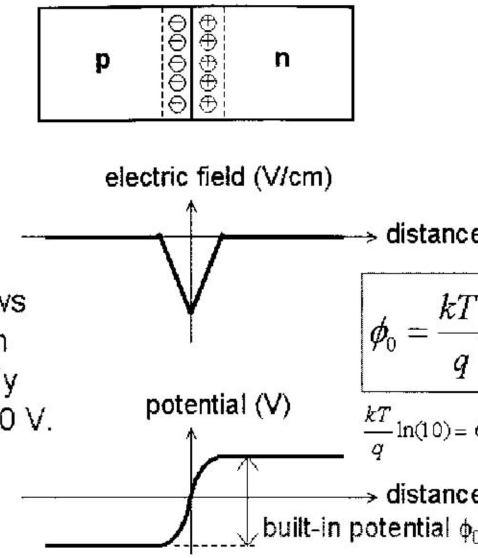
- The space charge due to immobile ions in the depletion region establishes an electric field which opposes carrier diffusion.

Charge Density Distribution

Charge is stored in the depletion region.



Electric Field and Built-In Potential ϕ_0

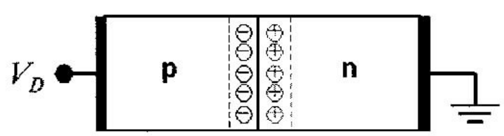


No net current flows across the junction when the externally applied voltage is 0 V.

$$\phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$\frac{kT}{q}\ln(10) = 60\text{mV for } T = 300\text{K}$

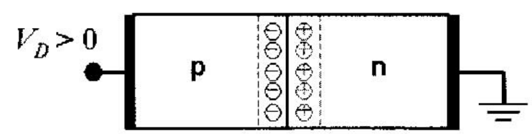
Effect of Applied Voltage



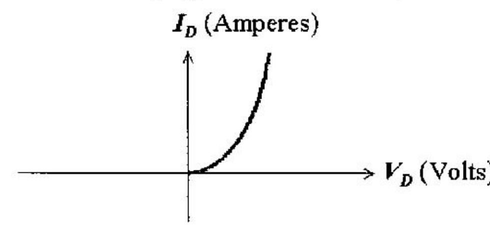
- The quasi-neutral p and n regions have low resistivity, whereas the depletion region has high resistivity. Thus, when an external voltage V_D is applied across the diode, almost all of this voltage is dropped across the depletion region. (Think of a voltage divider circuit.)
- If $V_D > 0$ (***forward bias***), the potential barrier to carrier diffusion is reduced by the applied voltage.
- If $V_D < 0$ (***reverse bias***), the potential barrier to carrier diffusion is increased by the applied voltage.

Forward Bias

- As V_D increases, the potential barrier to carrier diffusion across the junction decreases*, and current increases exponentially.



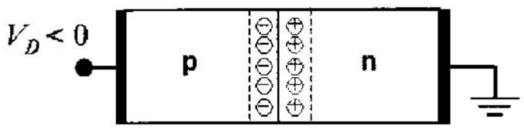
The carriers which diffuse across the junction become minority carriers in the quasi-neutral regions; they then recombine with majority carriers, "dying out" with distance.



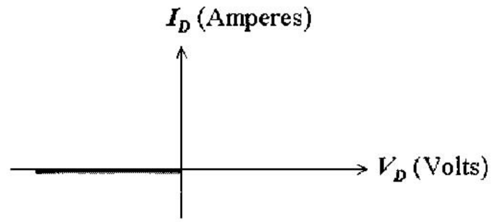
* Hence, the width of the depletion region decreases.

Reverse Bias

- As $|V_D|$ increases, the potential barrier to carrier diffusion across the junction increases*; thus, no carriers diffuse across the junction.



A very small amount of reverse current ($I_D < 0$) does flow, due to minority carriers diffusing from the quasi-neutral regions into the depletion region and drifting across the junction.

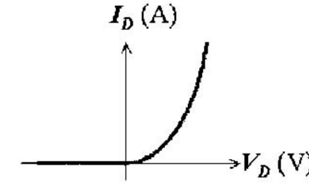


* Hence, the width of the depletion region increases.

I-V Characteristic

Exponential diode equation: $$I_D = I_S (e^{qV_D/kT} - 1)$$

$$\frac{kT}{q} = 0.026 \text{ Volts for } T = 300\text{K}$$



I_S is the diode ***saturation current***

- function of n_i^2, A_D, N_A, N_D, length of quasi-neutral regions
- typical range of values: 10^{-14} to 10^{-17} A/μm^2

Note that $e^{0.6/0.026} = 10^{10}$ and $e^{0.72/0.026} = 10^{12}$

→ I_D is in the mA range for V_D in the range 0.6 to 0.7 V, typically.

Depletion Region Width W_j

- The width of the depletion region is a function of the bias voltage, and is dependent on N_A and N_D:

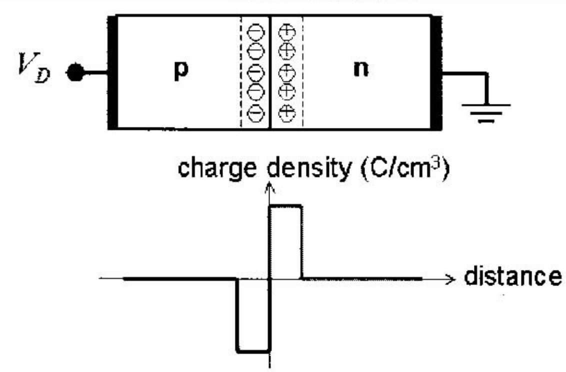
$$W_j = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(\phi_0 - V_D)}$$

- If one side is much more heavily doped than the other (which is commonly the case), then this can be simplified:

$$W_j \cong \sqrt{\frac{2\varepsilon_{Si}}{qN}(\phi_0 - V_D)} \qquad \varepsilon_{Si} = 10^{-12} \text{ F/cm}$$

where N is the doping concentration on the more lightly doped side

Junction Capacitance



- The charge stored in the depletion region changes with applied voltage. This is modeled as junction capacitance

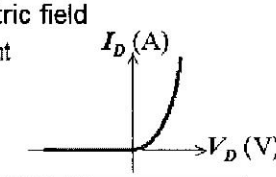
$$C_j = \frac{A_D \varepsilon_{Si}}{W_j}$$

Summary: *pn*-Junction Diode Electrostatics

- A depletion region (in which ***n*** and ***p*** are each much smaller than the net dopant concentration) is formed at the junction between p- and n-type regions
  - A built-in potential barrier (voltage drop) exists across the depletion region, opposing carrier diffusion (due to a concentration gradient) across the junction: $\phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$
    - At equilibrium (V_D=0), no net current flows across the junction
  - Width of depletion region $W_j \cong \sqrt{\frac{2\varepsilon_{Si}}{qN}(\phi_0 - V_D)}$
    - decreases with increasing forward bias (p-type region biased at higher potential than n-type region)
    - increases with increasing reverse bias (n-type region biased at higher potential than p-type region)
  - Charge stored in depletion region → capacitance $C_j = \frac{A_D \varepsilon_{Si}}{W_j}$

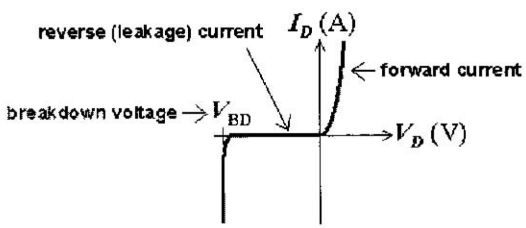
Summary: *pn*-Junction Diode *I-V*

- Under forward bias, the potential barrier is reduced, so that carriers flow (by diffusion) across the junction
  - Current increases exponentially with increasing forward bias
  - The carriers become minority carriers once they cross the junction; as they diffuse in the quasi-neutral regions, they recombine with majority carriers (supplied by the metal contacts)
    "injection" of minority carriers
- Under reverse bias, the potential barrier is increased, so that negligible carriers flow across the junction
  - If a minority carrier enters the depletion region (by thermal generation or diffusion from the quasi-neutral regions), it will be swept across the junction by the built-in electric field
    "collection" of minority carriers → reverse current



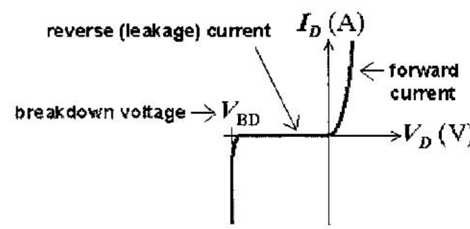
pn-Junction Reverse Breakdown

- As the reverse bias voltage increases, the peak electric field in the depletion region increases. When the electric field exceeds a critical value ($E_{crit} \cong 2\text{x}10^5$ V/cm), the reverse current shows a dramatic increase:

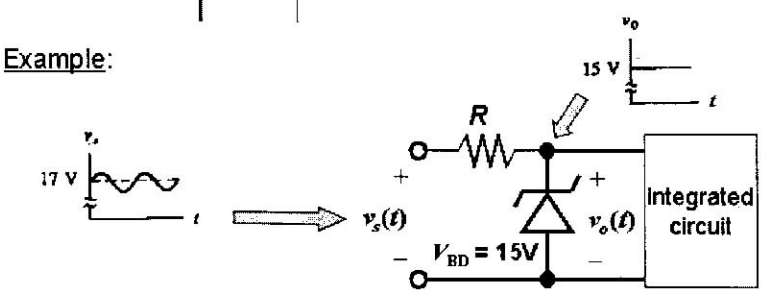


Zener Diode

A ***Zener diode*** is designed to operate in the breakdown mode.



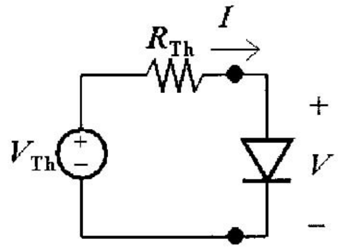
Example:



Circuit Analysis with a Nonlinear Element

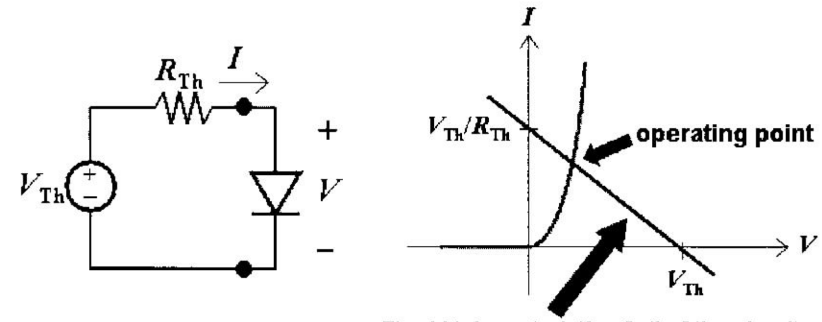
Since the pn junction is a nonlinear circuit element, its presence complicates circuit analysis.

(Node and loop equations become transcendental.)



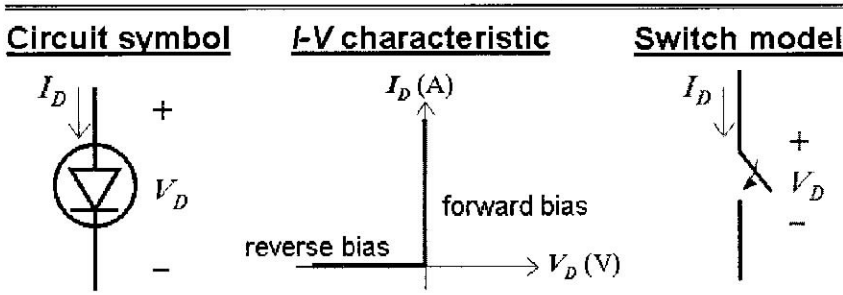
Load Line Analysis Method

1. Graph the *I-V* relationships for the non-linear element and for the rest of the circuit
2. The operating point of the circuit is found from the intersection of these two curves.



The *I-V* characteristic of all of the circuit except the non-linear element is called the ***load line***

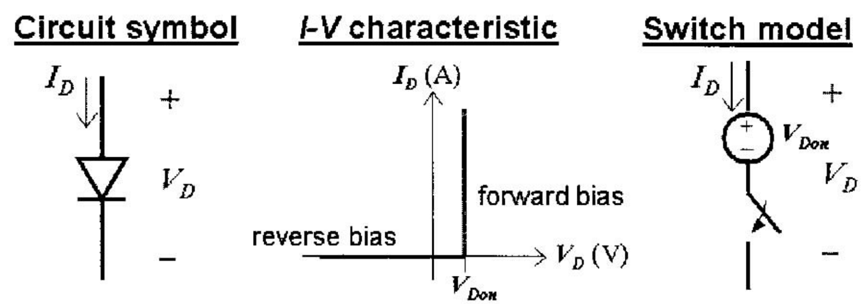
Ideal Diode Model of pn Diode



- An ideal diode passes current only in one direction.
- An ***ideal diode*** has the following properties:
  - when $I_D > 0$, $V_D = 0$
  - when $V_D < 0$, $I_D = 0$

  Diode behaves like a switch:
  - closed in forward bias mode
  - open in reverse bias mode

Large-Signal Diode Model



For a Si pn diode, $V_{Don} \cong 0.7$ V

RULE 1: When $I_D > 0$, $V_D = V_{Don}$

RULE 2: When $V_D < V_{Don}$, $I_D = 0$

Diode behaves like a voltage source in series with a switch:
- closed in forward bias mode
- open in reverse bias mode

How to Analyze Circuits with Diodes

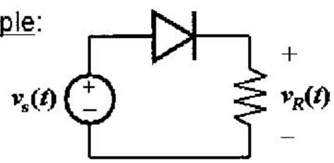
A diode has only two states:

- **forward biased:** $I_D > 0$, $V_D = 0$ V (or 0.7 V)
- **reverse biased:** $I_D = 0$, $V_D < 0$ V (or 0.7 V)

Procedure:

1. Guess the state(s) of the diode(s)
2. Check to see if KCL and KVL are obeyed.
3. If KCL and KVL are not obeyed, refine your guess
4. Repeat steps 1-3 until KCL and KVL are obeyed.

Example:

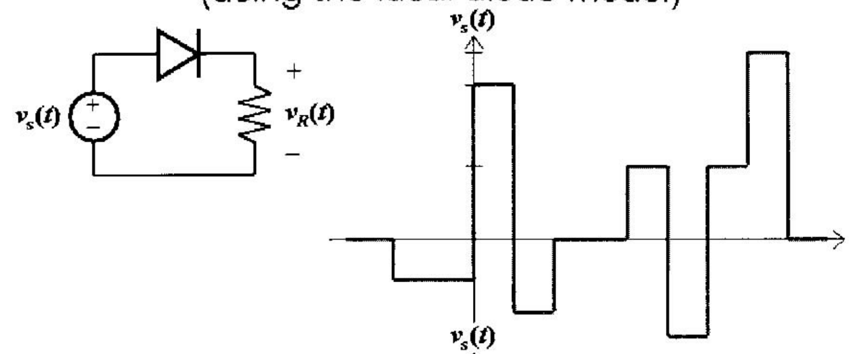


If $v_s(t) > 0$ V, diode is forward biased (else KVL is disobeyed – try it)

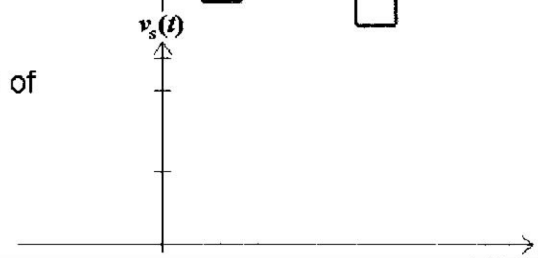
If $v_s(t) < 0$ V, diode is reverse biased (else KVL is disobeyed – try it)

Application Example #1

(using the ideal diode model)

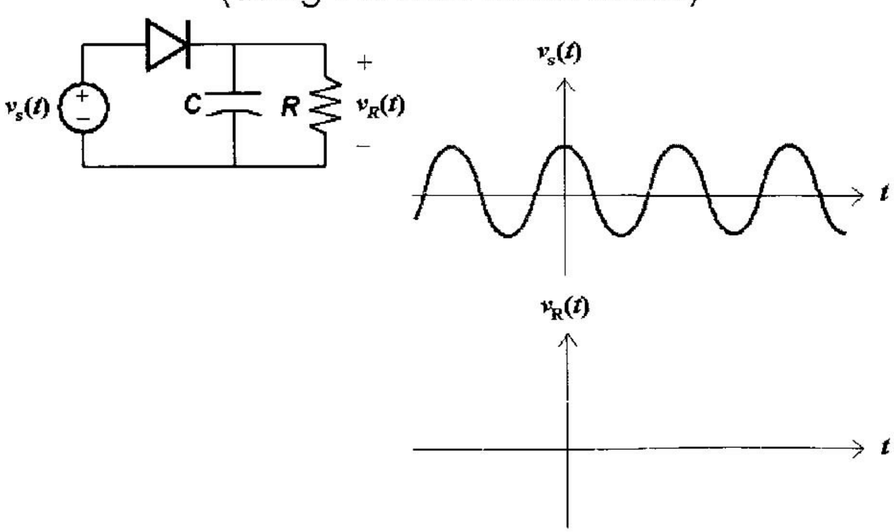


"rectified" version of input waveform:



Application Example #2

(using the ideal diode model)

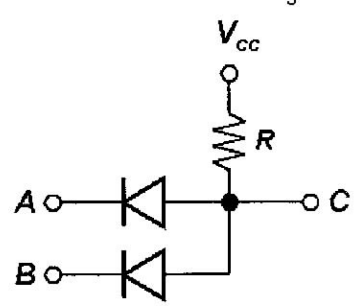


Diode Logic

- Diodes can be used to perform logic functions:

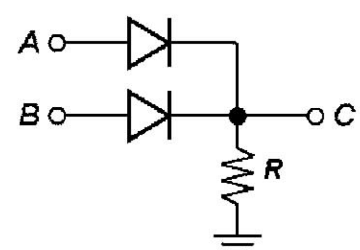
AND gate

output voltage is high only if both A and B are high



OR gate

output voltage is high if either (or both) A and B are high



Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")
Between what voltage levels does C vary?