Lecture #25

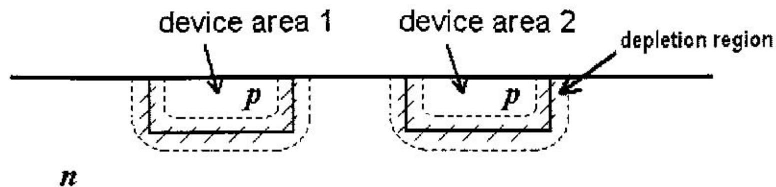
OUTLINE

- Device isolation methods
- Electrical contacts to Si
- Mask layout conventions
- Process flow examples
  - Resistor
  - N-channel MOSFET
  - CMOS process flow
- Circuit extraction from layout

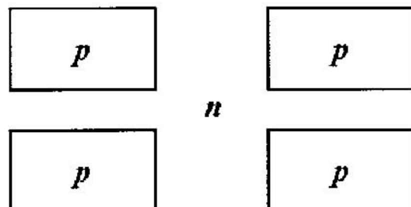
Device Isolation Methods

(1) pn-junction isolation:

Cross-Sectional View:

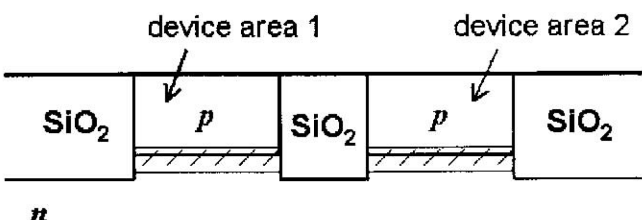


Top View:

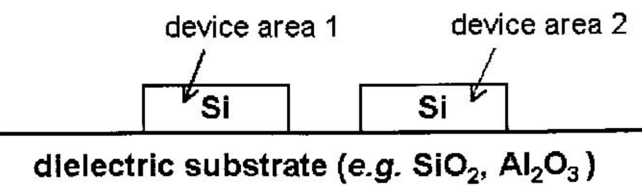


- The substrate is biased to ensure that the pn junctions are never forward biased

(2) Oxide isolation:



(3) Silicon-on-Insulator substrate:

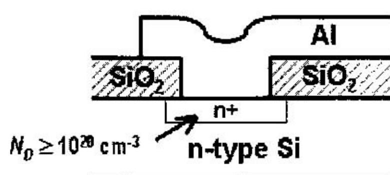


dielectric substrate (*e.g.* SiO_2, Al_2O_3)

Electrical Contacts to Si

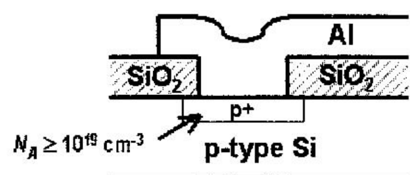
- In order to achieve a low-resistance ("ohmic") contact between metal and silicon, the silicon must be heavily doped:

Metal contact to n-type Si



$N_D \geq 10^{20}$ cm^{-3}

Metal contact to p-type Si



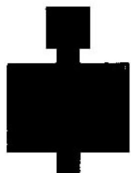
$N_A \geq 10^{19}$ cm^{-3}

→ **To contact the body of a MOSFET, locally heavy doping is used.**

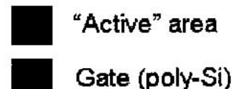
Mask Layout

- Typically, multiple lithography steps are needed in order to fabricate an integrated circuit.
  - Each lithography step utilizes a mask with the desired pattern for a specific layer.
- Computer-aided design (CAD) tools are used to generate the masks
  - The desired pattern for each layer is drawn, and can be overlaid with the patterns for other layers, to make sure that they are properly aligned to each other

Layout Example:
MOSFET gate pattern overlaid with "active area" pattern

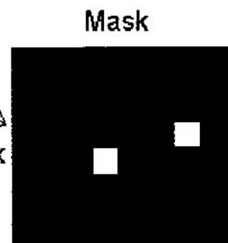


Process layers:

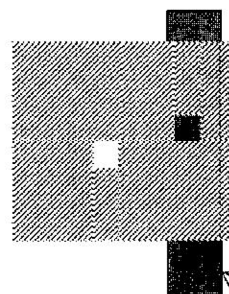


What if the physical mask looks like this?

Mask



Layout:



Layout is all color, with the exception of a few holes

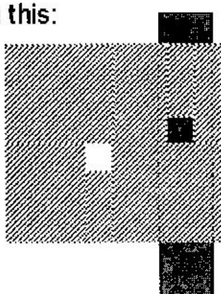
→ ***very* inconvenient to draw and to display**

Dark-Field / Light-Field Convention

A dark-field mask blocks our view of underlying layers

…but if we draw the "negative" (or "complement") of masks that are dark-field, the CAD layout is much easier, and the overlaid layers are easier to visualize

Rather than this:



Draw only the "holes" on the layout, *i.e.* the clear areas

To indicate that the CAD layout is the negative of the mask, label it "dark field". "Clear field" indicates a "positive" mask.

Process Flow Example #1: Resistor

Three-mask process:

Starting material: p-type wafer with $N_A = 10^{16}$ cm^{-3}

Step 1: grow 500 nm of SiO_2

Step 2: pattern oxide using the oxide mask (dark field)

Step 3: implant phosphorus and anneal to form an n-type layer with $N_D = 10^{20}$ cm^{-3} and depth 100 nm

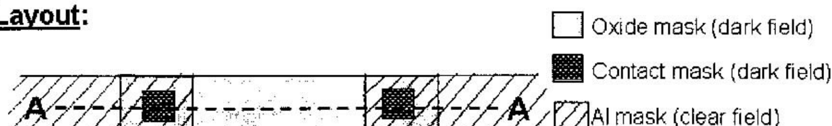
Step 4: deposit oxide to a thickness of 500 nm

Step 5: pattern deposited oxide using the contact mask (dark field)

Step 6: deposit aluminum to a thickness of 1 μm

Step 7: pattern using the aluminum mask (clear field)

Layout:



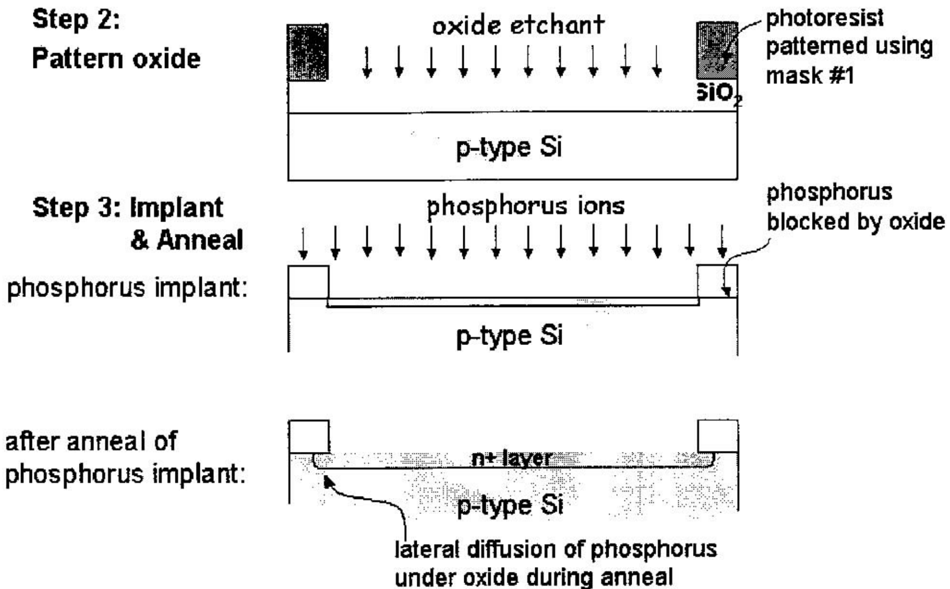
A-A Cross-Section

Step 2: Pattern oxide

Step 3: Implant & Anneal

phosphorus implant:

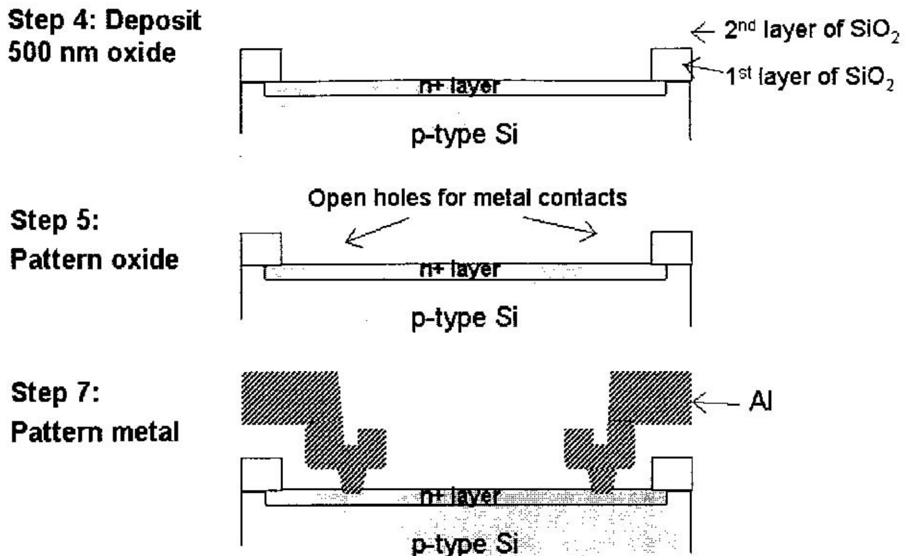
after anneal of phosphorus implant:



Step 4: Deposit 500 nm oxide

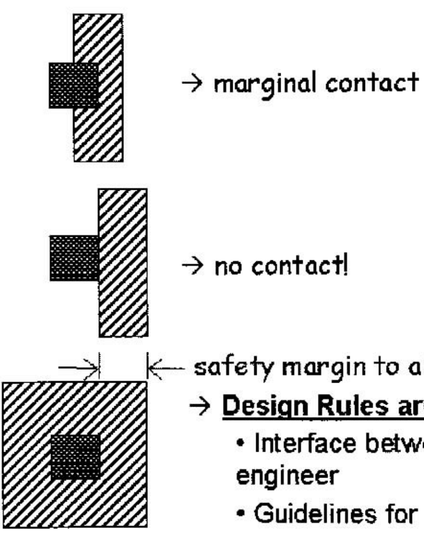
Step 5: Pattern oxide

Step 7: Pattern metal



Importance of Layer-to-Layer Alignment

Example: metal line to contact hole

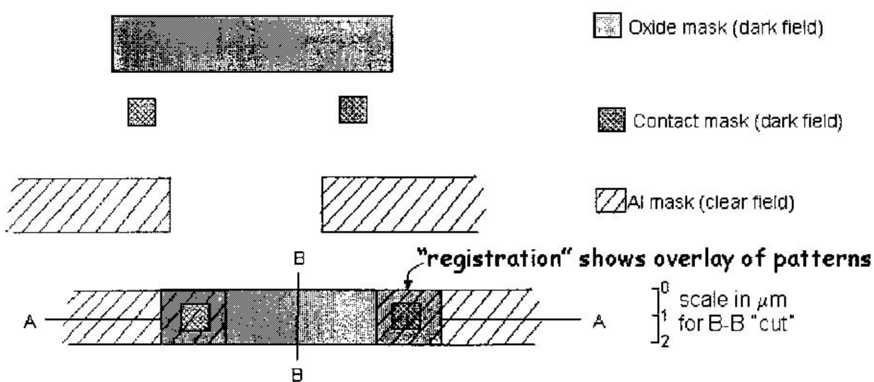


Example of Design Rule:
If the minimum feature size is 2λ, then the safety margin for overlay error is λ.

→ **Design Rules are needed:**
- Interface between designer & process engineer
- Guidelines for designing masks

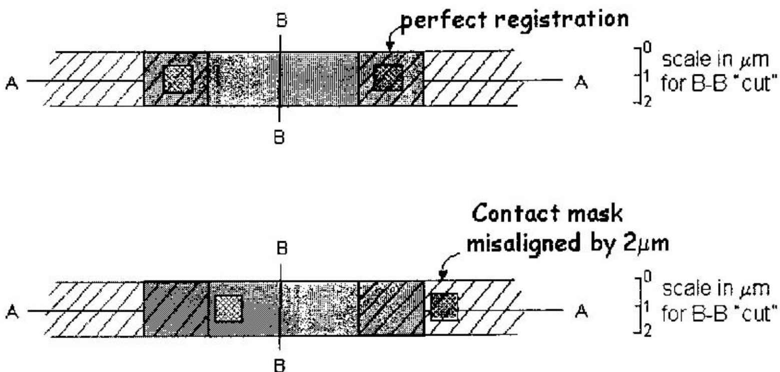
IC RESISTOR MASK LAYOUTS – REGISTRATION OF EACH MASK

Registration of mask patterns is critical → show separate layouts to avoid ambiguity



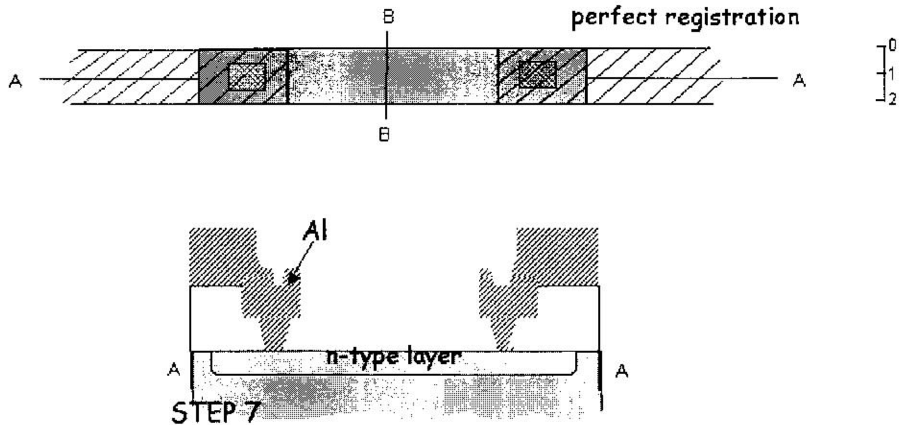
Registration of one mask to the next (also called "alignment" and "overlay") is a crucial aspect of lithography

Same Layout but with misregistration (misalignment)

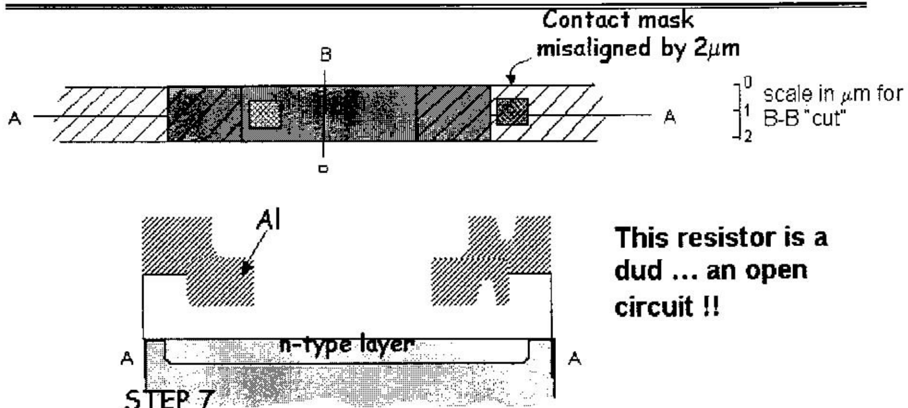


Lets look again at cross-section A-A to understand the consequence of this misalignment. Note contact mask ⟶ 2μm

Layout with no misregistration (misalignment)



Layout with misregistration (misalignment)

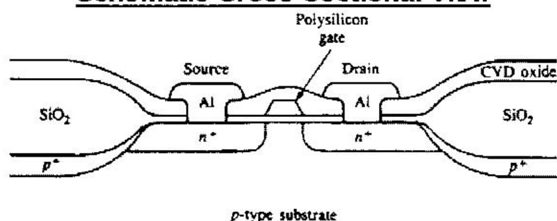


This resistor is a dud … an open circuit !!

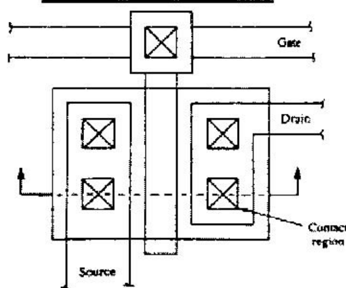
Thus we need safety margins in layout which take into account the possible tolerances in fabrication. Each process has a set of "**design rules**" which specify the safety margins.

N-channel MOSFET

Schematic Cross-Sectional View



Layout (Top View)



4 lithography steps are required:

1. active area
2. gate electrode
3. contacts
4. metal interconnects

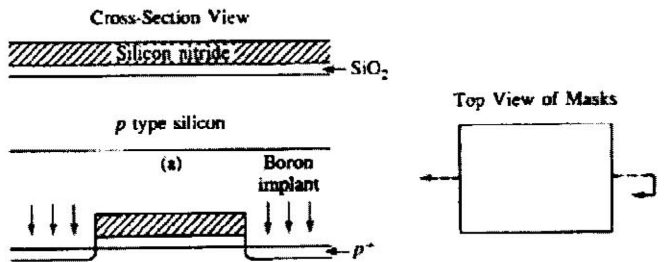
Process Flow Example #2: nMOSFET

1) Thermal oxidation (~10 nm "pad oxide")

2) Silicon-nitride (Si_3N_4) deposition by CVD (~40nm)

3) Active-area definition (lithography & etch)

4) Boron ion implantation ("channel stop" implant)



5) Thermal oxidation to grow oxide in "field regions"

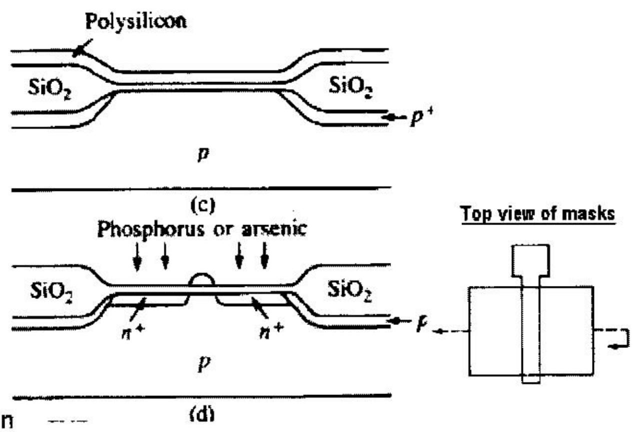
6) Si_3N_4 & pad oxide removal

7) Thermal oxidation ("gate oxide")

8) Poly-Si deposition by CVD

9) Poly-Si gate-electrode patterning (litho. & etch)

10) P or As ion implantation to form n+ source and drain regions

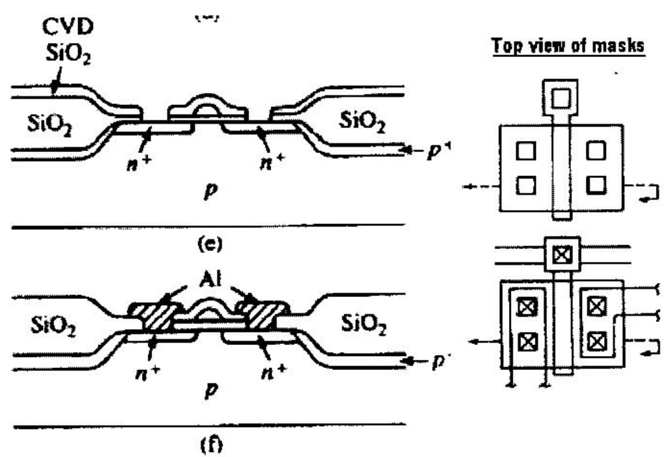


11) SiO_2 CVD

12) Contact definition (litho. & etch)

13) Al deposition by sputtering

14) Al patterning by litho. & etch to form interconnects

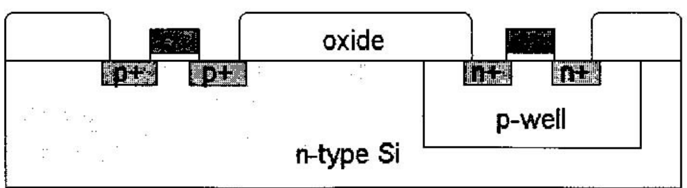


CMOS Technology

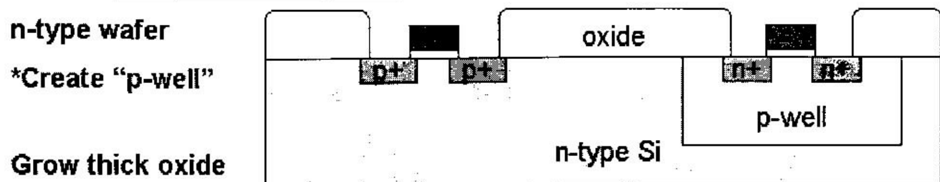
Challenge: Build both NMOS & PMOS transistors on a single silicon chip

- NMOSFETs need a p-type substrate
- PMOSFETs need an n-type substrate

→ Requires extra process steps!



Conceptual CMOS Process Flow



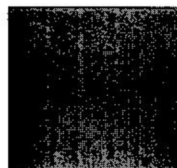
- n-type wafer
- *Create "p-well"
- Grow thick oxide
- *Remove thick oxide in transistor areas ("active region")
- Grow gate oxide
- Deposit & *pattern poly-Si gate electrodes
- *Dope n channel source and drains (need to protect PMOS areas)
- *Dope p-channel source and drains (need to protect NMOS areas)
- Deposit insulating layer (oxide)
- *Open contact holes
- Deposit and *pattern metal interconnects

→ At least 3 more masks, as compared to NMOS process

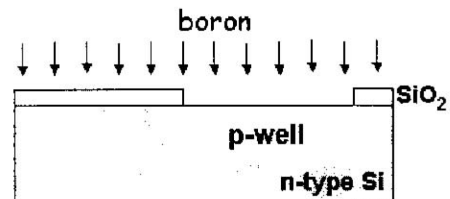
Additional Process Steps Required for CMOS

1. Well Formation

Top view of p-well mask
(dark field)



Cross-sectional view of wafer



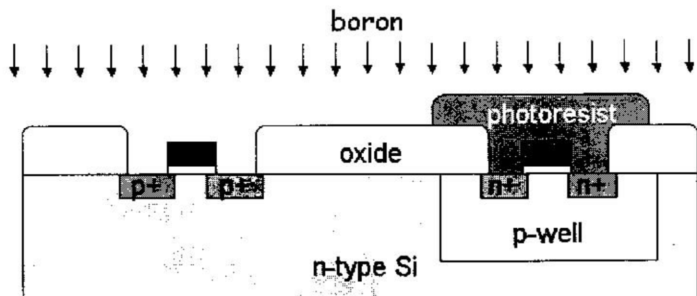
- **Before transistor fabrication, we must perform the following process steps:**
  1. grow oxide layer; pattern oxide using p-well mask
  2. implant phosphorus; anneal to form deep p-type regions

2. Masking the Source/Drain Implants

"Select p-channel" → We must protect the n-channel devices during the boron implantation step, and

"Select n-channel" → We must protect the p-channel devices during the arsenic implantation step

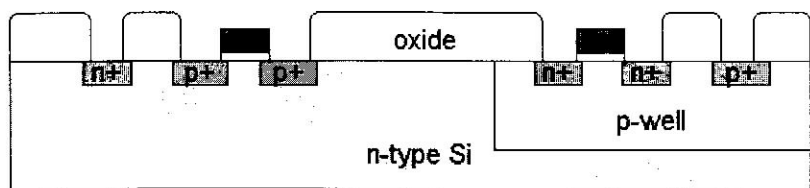
Example: Select p-channel



Forming Body Contacts

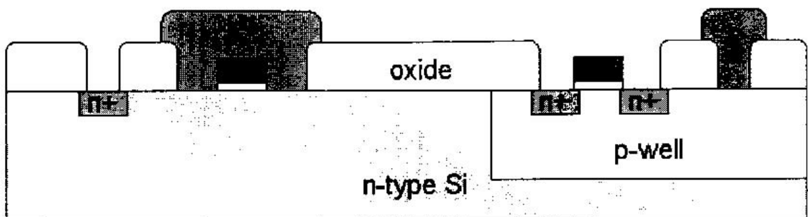
Modify oxide mask and "select" masks:

1. Open holes in original oxide layer, for body contacts
2. Include openings in select masks, to dope these regions

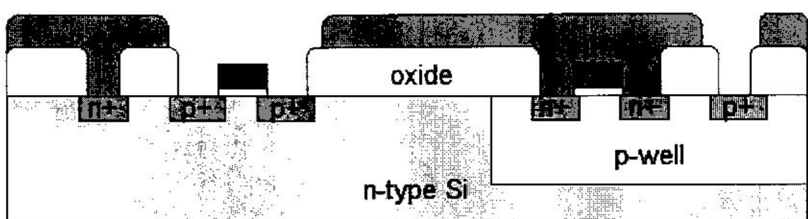


Select Masks

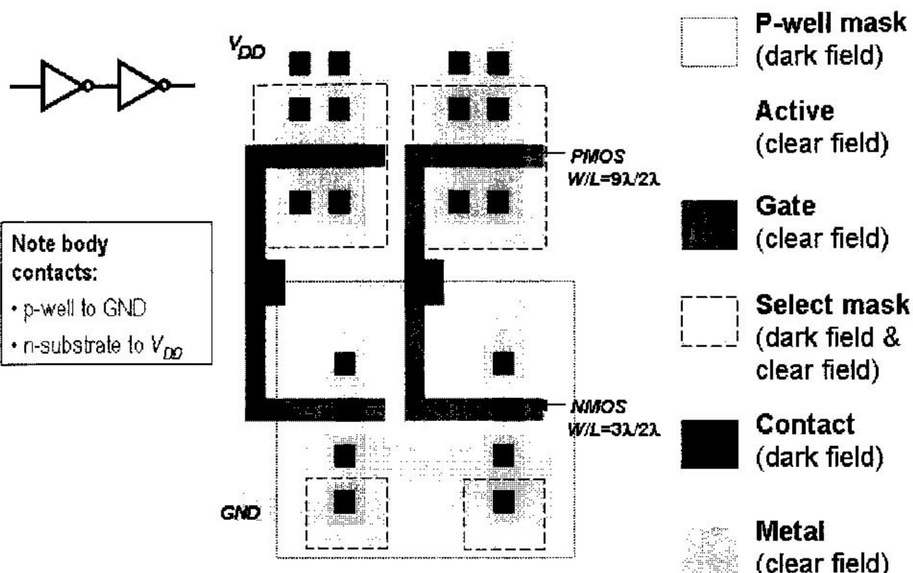
N-select:



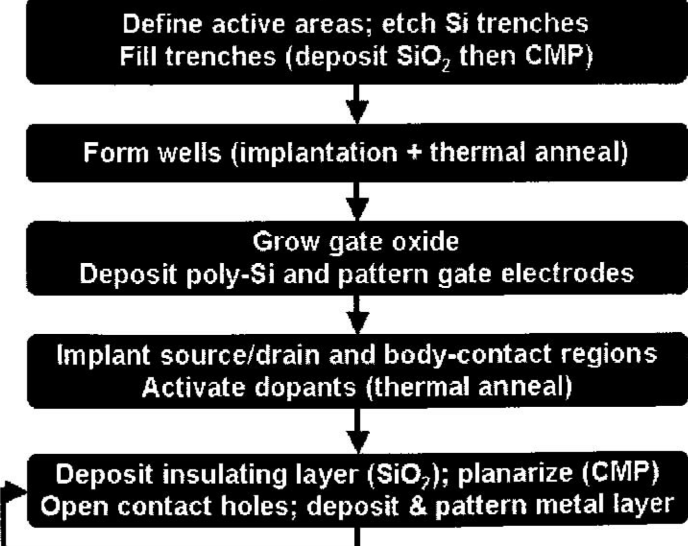
P-select:



CMOS Inverter Layout



Modern CMOS Process at a Glance



Visualizing Layouts and Cross-Sections with SIMPLer

SIMPL is a CAD tool created by Prof. Neureuther's group

- allows IC designers to visualize device cross-sections corresponding to a fabrication process and physical layout.

A Berkeley undergraduate student, Harlan Hile, created a mini-version of SIMPL (called SIMPLer) for EECS40.

- It's a JAVA program -> can be run on any computer, as well as on a web server.
- You can access it directly at

  http://www.ocf.berkeley.edu/~hhile/SIMPLer/SIMPLer.html

Circuit Extraction from Layouts

Procedure:

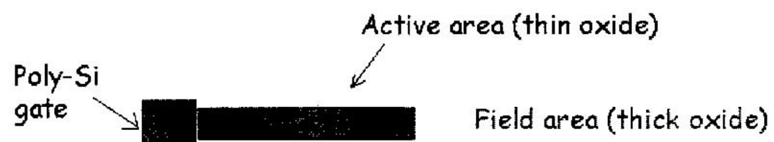
1) Inspect layout and identify obvious devices:
   - NMOSFETs
   - PMOSFETs
   - wires (metal or poly-Si)

2) Identify other (often undesired) circuit components:
   - resistances (*e.g.* associated with long wires)
   - capacitances

3) Draw schematic (V_{DD} at top, GND at bottom)

Identifying a MOSFET

Poly-Si line crossing over an "active" region → **MOSFET!**



If the active area is located within p-well region → **NMOS**

If the active area is NOT located in p-well region → **PMOS**

Example: Circuit Extraction from Layout