

EECS 42 Intro. electronics for CS Spring 2003 Lecture 20: 04/14/03 A.R. Neureuther
Version Date 04/05/03

EECS 42 Introduction to Electronics for Computer Science

Andrew R. Neureuther

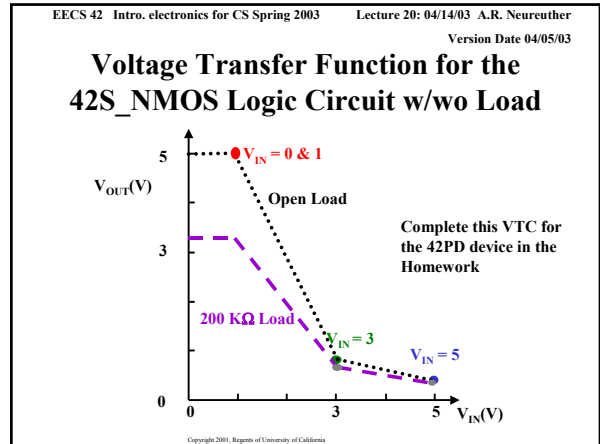
Lecture # 20 Logic Transients

Handout of Monday Lecture.

A) 2nd Midterm Review (Cont.)
B) Latch circuit to hold/release signals
C) Cascade CMOS elements with latches
D) Logic Feedback creates memory

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Game Plan 04/14/03

Last Week: Logic Delay; resistor model, CMOS operation and delay

Monday 4/14/03:

- 2nd Midterm review (Cont.)
- CMOS Latch and use in logic cascade
- Feedback in logic to produce memory

Wednesday 04/09/03:

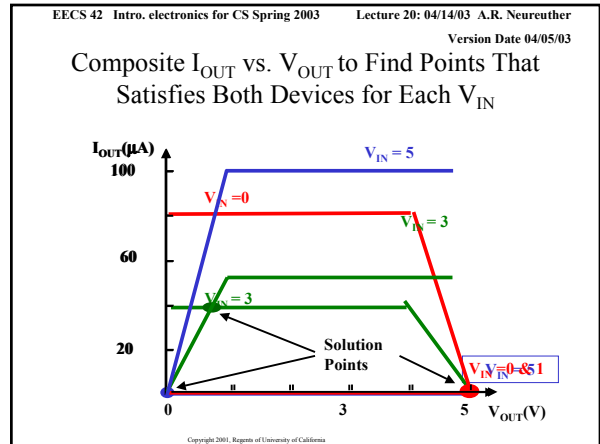
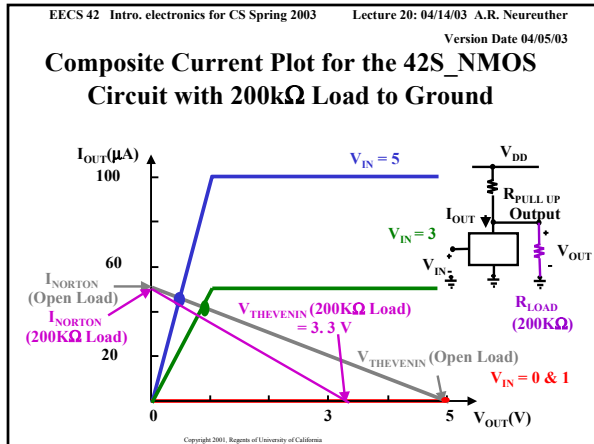
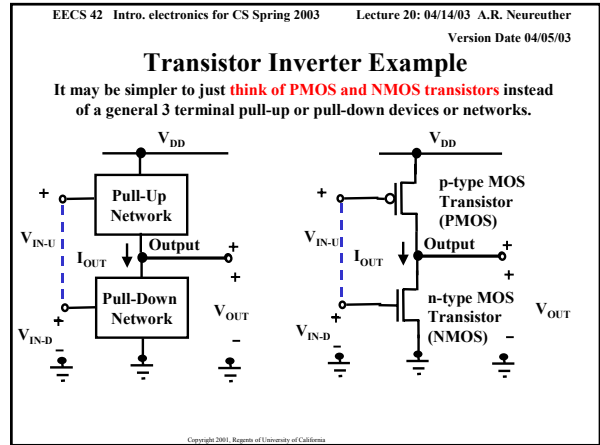
- 2nd Midterm

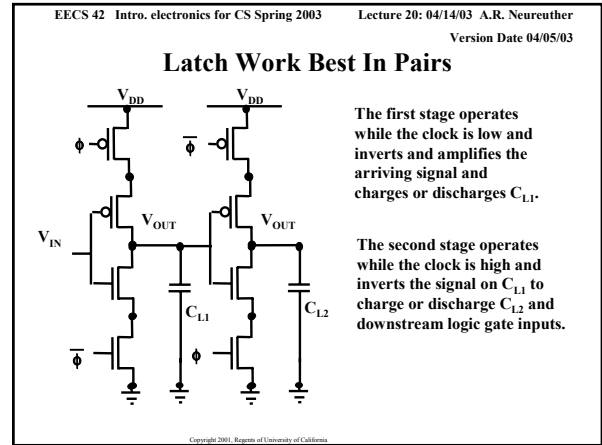
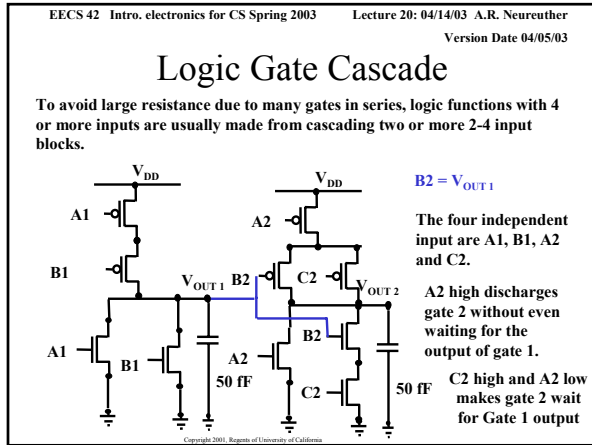
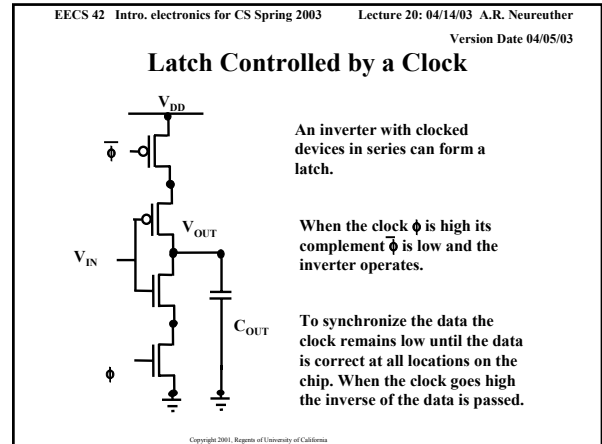
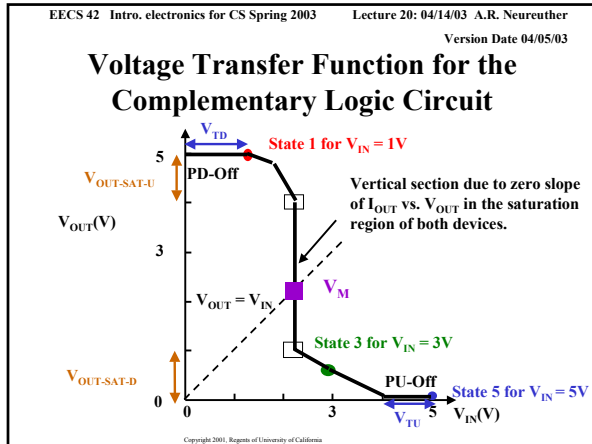
Next (13th) Week: Diodes and MOS Operation

No Problem set for 4/16 as Midterm 4/16: Lectures 1-17 with emphasis on Lectures 10-17; Review Session Monday 5:30-7PM

Problem set #10 for 4/23: Logic Delay

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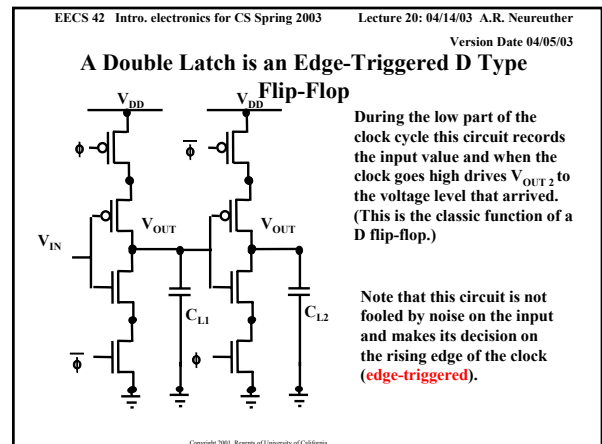


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Data Synchronization problem

- Combinatorial logic gates can give incorrect answers prematurely and may take several gate propagation delays produce an answer.
- Clocks (signals as to when to proceed) and latches (which capture and hold the correct outputs) can provide synchronization.

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Combinatorial Logic and Clocked Latches: Wiring

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Example of the Opposite State

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Combinatorial Logic and Clocked Latches: Signal Flow

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Adding Memory Controls

Set-Reset Flip-Flop

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Feedback Can Provide Memory

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Adding a Clock

Clocked S-R Flip-Flop

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