EECS 42 Introduction to Electronics for Computer Science

Andrew R. Neureuther

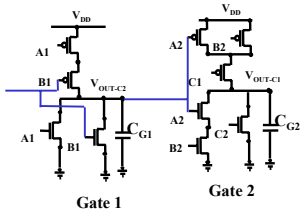
Lecture # 22 Latency, Clock Design, Memory

Handout of Wednesday Lecture.

A) Timing Diagram for a Clocked Latch
B) Latency and Maximum Clock Frequency
C) Use of Feedback to create Memory

http://inst.EECS.Berkeley.EDU/~ee42/

Example of Circuits to Integrate with Latches



Game Plan 04/21/03

Last Week: Logic Delay; resistor model, CMOS operation and delay

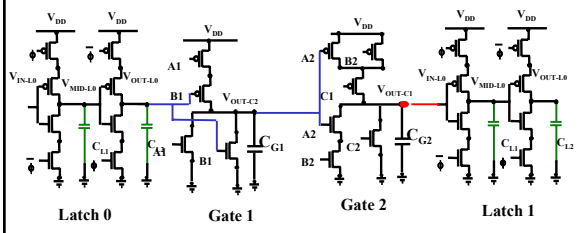
Monday 4/14/03:
- ❑ 2nd Midterm returned
- ❑ CMOS Latch and use in logic cascade

Wednesday 04/09/03:
- ❑ Clocked Latch and Timing Diagram
- ❑ Latency and Throughput
- ❑ Feedback in logic to produce memory

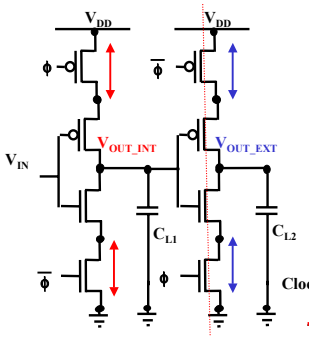
Next (13th) Week: Diodes and MOS Devices

Problem set #10 for 4/303: Logic Delay; Cascade; Latches and Clock frequency

Latch Implementation: Lumped

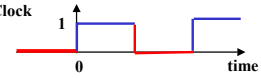


Latch Work Best In Pairs

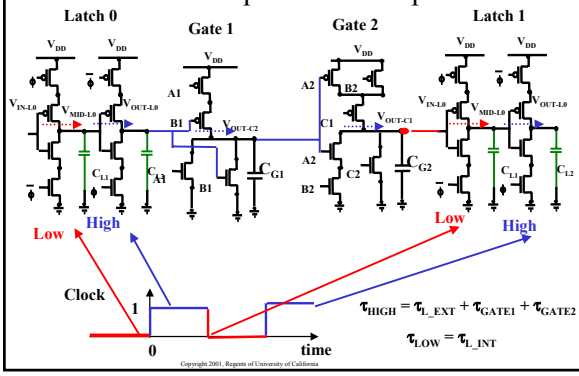


The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges C_{L1}.

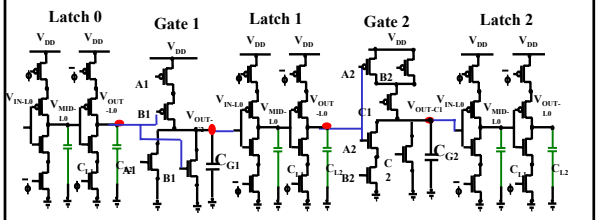
The second stage operates while the clock is high and inverts the signal on C_{L1} to charge or discharge C_{L2} and downstream logic gate inputs.



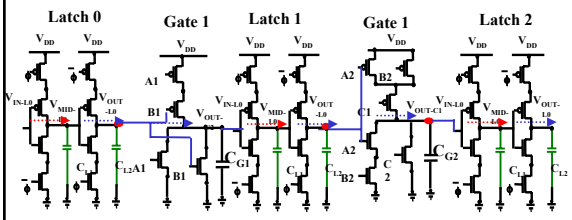
Latch Operation: Lumped



Latch Implementation: Pipelined



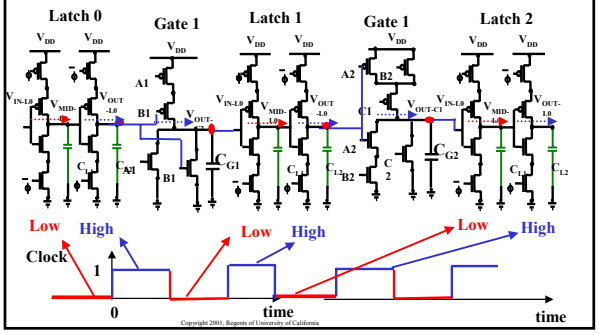
Clock Optimization: Pipelined



$\tau_{HIGH} = \tau_{L\_EXT} + \max(\tau_{GATE1}, \tau_{GATE2})$

$\tau_{LOW} = \tau_{L\_INT}$

Latch Operation: Pipelined



Latency and Throughput

Latency L is the delay between the rising edge of the clock on L0 and the data being valid internally in the last latch.

$L_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT}$
$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$

$L_{PIPLINED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{L\_INT} + \tau_{L\_EXT} + \tau_{GATE2} + \tau_{L\_INT}$
$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 12\tau_{INV}$

Throughput T is the bits per second through the latches and is the maximum clock frequency.

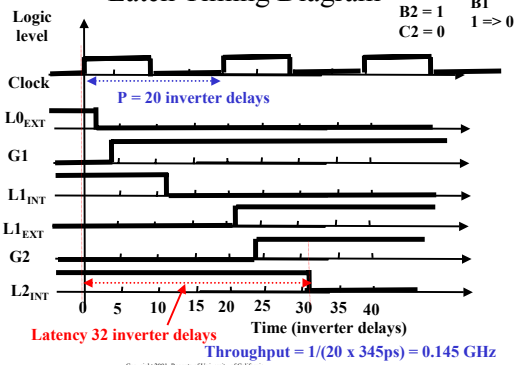
$P_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT}$
$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$
$F_{LUMPED} = 1/8(345ps) = 0.36$ GHz

$P_{PIPELINED} = \tau_{L\_EXT} + MAX(\tau_{GATE1}, \tau_{GATE2}) + \tau_{L\_INT}$
$= 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 6\tau_{INV}$ $F_{PIPLINED} = 1/6(345ps) = 0.48$ GHz

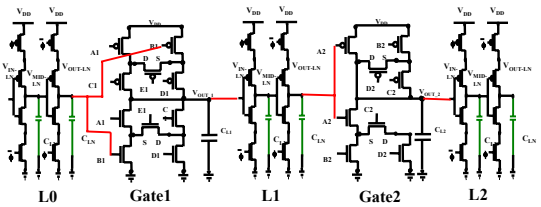
Latch Timing Diagram

A1 = 0
B2 = 1
C2 = 0

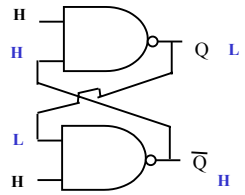
B1
1 => 0



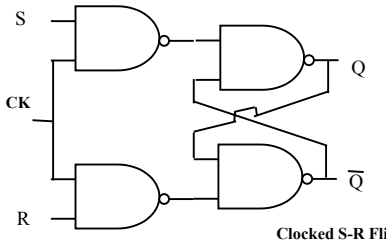
Homework 10.3



Feedback Can Provide Memory

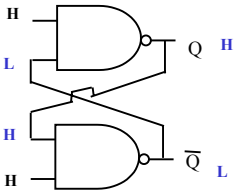


Adding a Clock

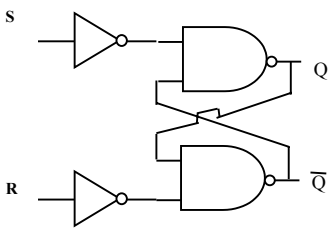


Clocked S-R Flip-Flop

Example of the Opposite State



Adding Memory Controls



Set-Reset Flip-Flop