EECS 42 Introduction to Electronics for Computer Science

Lecture # 25 Microfabrication

Handout of Monday Lecture.

Today: how are these things made?

– Silicon wafers
– Oxide formation by growth or deposition
– Other films
– Pattern transfer by lithography (start)

http://inst.EECS.Berkeley.EDU/~ee42/

Game Plan 05/05/03

Last Week: Latches

Monday 5/05/03:

- ☐ **Semiconductor Properties**
- ☐ **Diode Operation, Equation and Circuits**

Wednesday 5/07/03: Sheila Ross -

- ☐ **Review basic circuits**
- ☐ **Review Basic Logic**
- ☐ **Review Transient**
- ☐ **HKN Evaluation**

Next (16th) Week: Review of Advanced materials

Problem set #11 for 5/7: Semiconductor resistance, Diode equation, diode circuit, MOS operation

Integrated Circuits

- J. Kilby, Texas Instruments and R. Noyce, Fairchild, circa 1958.
- Make the entire circuit at one time … using concepts borrowed from printing technology
- What do we need?
  - a substrate for the circuit
  - a way to dope regions of silicon n or p type
  - insulating and conducting films to form the MOS transistor and interconnect it
  - processes for etching patterns into these films

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Early 21st Century IC Technology

- Many levels of electrical interconnect (Cu)
  - Ten-level metal is entering production
- MOSFET is shrinking:
  - gate lengths of 10 nm = 0.01 μm have been demonstrated by Intel, TSMC, AMD, → new device structures are based on late 1990s UC Berkeley research (Profs. Hu, King, and Bokor)
- Technology/economic limits …
  - Roadblocks to increasing density are a huge challenge around 2015

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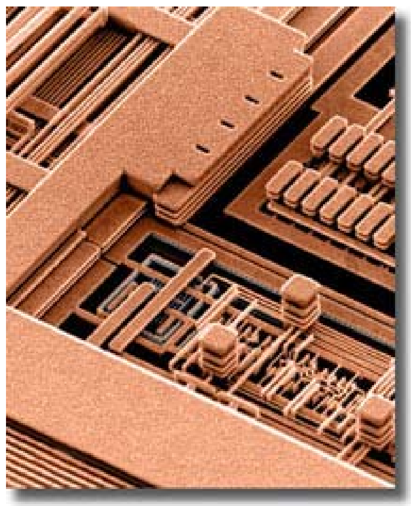
Complexity of IC Metallization



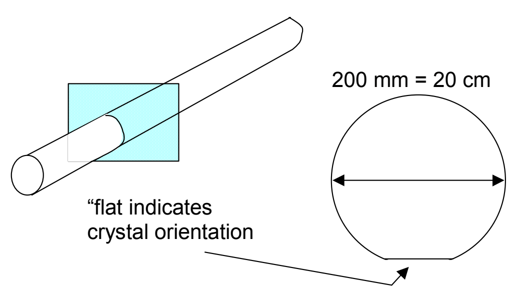
IBM Microelectronics Gallery

Colorized scanning-electron micrograph of the copper inter-connect layers, after removal of the insulating layers by a chemical etch

Note: all > 10^8 connections must work or the chip doesn't function. Current Berkeley research (Prof. Bora Nikolic) is directed at fault-tolerant design methodologies

Silicon Substrates (Wafers)

Crystals are grown from the melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a "flat" is ground along the boule) and then sliced like salami into wafers.

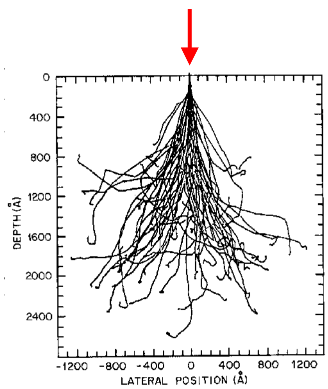


Typical wafer cost: $50

Sizes: Today 200 mm or 300 mm in diameter

Adding Dopants to Silicon

A finished wafer can have dopants added to its surface by a combination of *ion implantation* and *annealing* (heating the silicon wafer to > 800°C



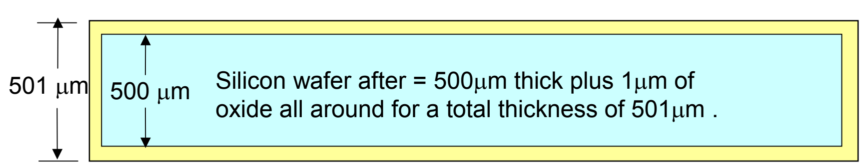
Features: crystal structure of the wafer is destroyed due to ion impact at energies of 20 keV – 5 MeV … damage can be as deep as 1 um below surface

Annealing heals the damage … nearly perfectly. The B or As or P atoms end up as substitutional impurities on lattice sites

THERMAL OXIDATION OF SILICON

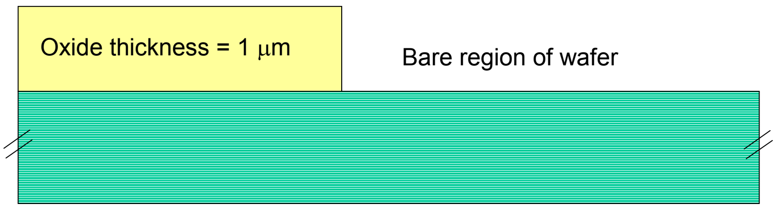
Silicon wafer before = 500μm thick

Thermal oxidation grows SiO_2 on Si, but it consumes Si from the substrate, so the wafer gets thinner. Suppose we grow 1μm of oxide:



THERMAL OXIDATION OF SILICON (continued)

Thermal oxidation rate slows with oxide thickness, so thick films hardly increase their thickness during growth of a thin film at a different position on the wafer. Consider starting with the following structure:



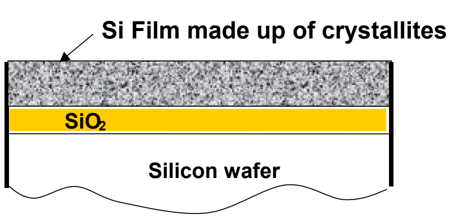
Now suppose we grow 0.1µm of SiO_2 :

Deposited IC Materials

Polycrystalline silicon (polysilicon or simply “poly”)

Wafer is heated to around 600 °C and a silicon-containing gas (SiH_4) is passed over it; a surface reaction results in a deposited layer of silicon:
$SiH_4 = Si + 2H_2$

Terminology: “CVD” =



Properties: Sheet resistance can be fairly low (e.g. if doped heavily and 500 nm thick, $R_\square = 20\ \Omega/\square$). It can withstand high temperature anneals. → major advantage for MOS gates

More Deposited Materials

Silicon Dioxide: Similar process (SiH_4 + 0_2) at 425°C
useful as an insulator between conducting layers

Metal films: (aluminum and copper)
Deposited at near room temperature using a "sputtering" process (Highly energetic argon ions batter the surface of a metal target, knocking atoms of loose which land on the surface of the wafer.)

Other films:
Special insulating layers with low dielectric constants, thin ceramic films (e.g., TiN) that are useful to keep materials from interacting during subsequent processing

Patterning the Layers - Lithography

Goal: Transfer the desired pattern information to the wafer

Fabrication process = sequence of processes in which layers are added or modified and each layer is ***patterned***, that is selectively removed or selectively added according to the circuit desired

Photolithography: invented circa 1822 by Nicéphore Niépce (France) – early pioneer in photography

Process for transferring a pattern in parallel (like printing)

Equipment , Materials, and Processes needed:

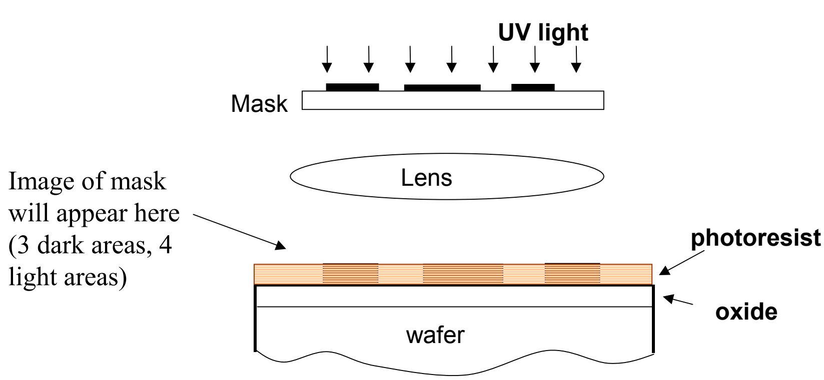
1. A mask (… where do we find masks, anyway?)
2. A photosensitive material (called ***photoresist***)
3. A light source and method of projecting the image of the mask onto the photoresist ("*printer*" or "*projection stepper*" or "*projection scanner*")
4. A method of "developing" the photoresist, that is removing it where the light hits it.
5. A method for then transferring the pattern from the photoresist to the layer underneath it, for example by etching the film, with some areas protected by the photoresist.

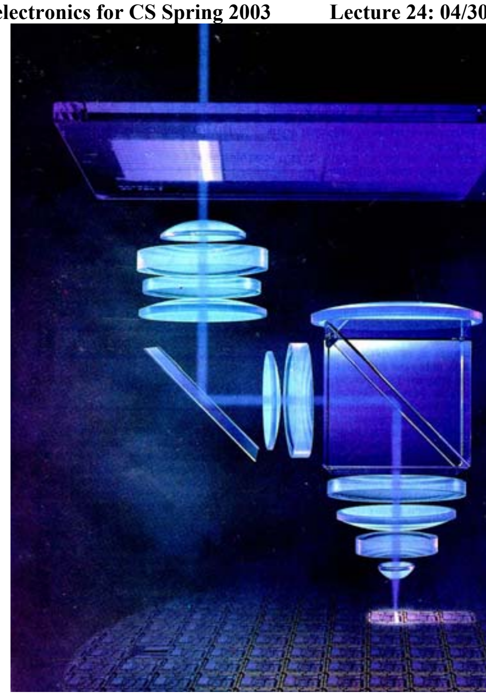
Pattern Transfer Overview

- A designer lays out a pattern for each layer in the circuit… the metal wiring layer, the transistor gate layer, etc, much like an architect lays out a city plan
- The patterns are created in an opaque material on a clear glass plate - the "mask". One mask is made for each layer. (Perhaps a total of 20)
- The wafer is prepared by coating its surface with a photo-sensitive polymer (today short-wavelength ("deep") UV light is used because smaller patterns can be created)
- The wafer is exposed in a kind of specialized "camera".. The projection stepper or scanner which has a light source, optics and holds the mask with the desired pattern. It is capable of aligning every pattern up with the patterns underneath to very high precision. Today's steppers cost circa $5M-$10M.
- The photoresist on the exposed wafer is "developed" by immersion in a liquid which removes the resist wherever the light has hit it.

Exposure Process

- A glass mask with a black/clear pattern is used to expose a wafer coated with about 1 μm of photoresist





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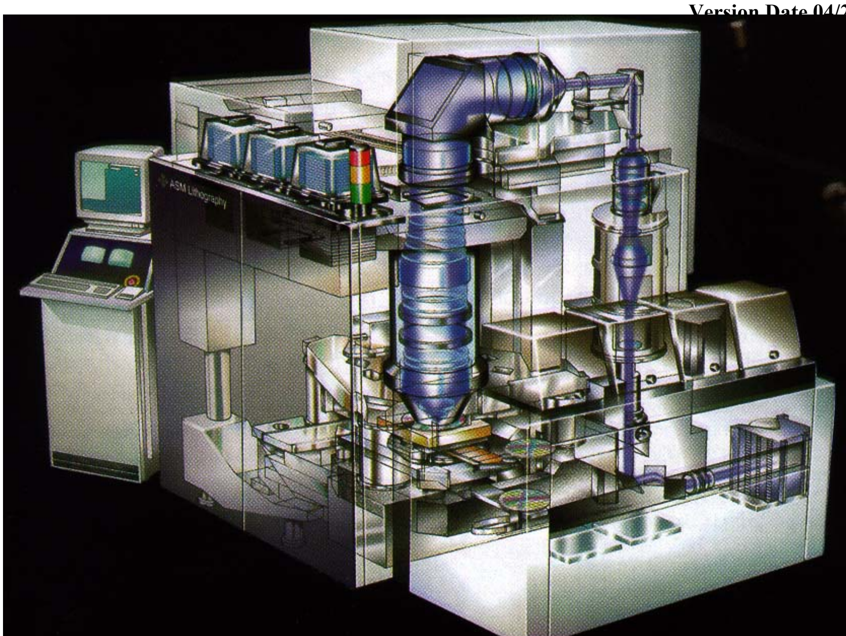

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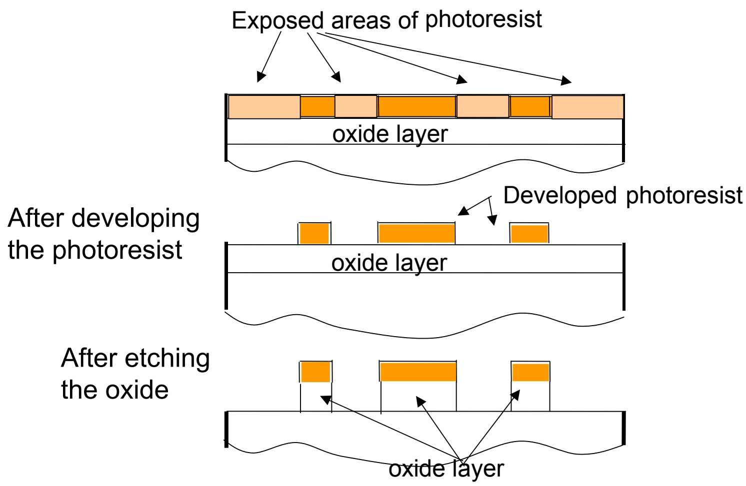
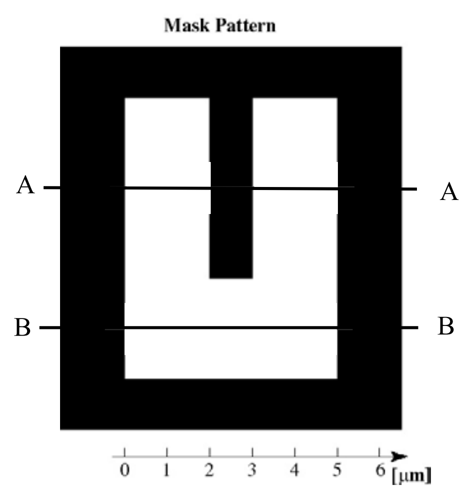
Photoresist Development and Etching

- Solutions with high pH dissolve the areas exposed to UV; unexposed areas (under the black patterns) are not dissolved



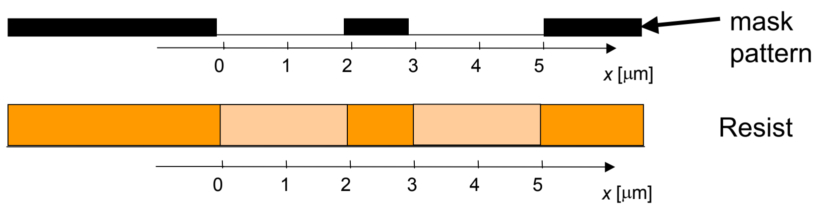
Visualizing Lithography

- Mask pattern (on glass plate)
- Look at cuts (cross sections) at various planes (*A-A* and *B-B*)

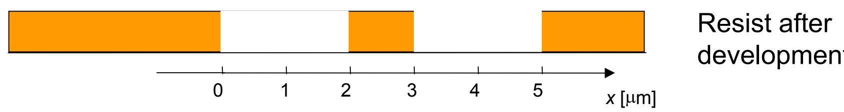


Along "A-A" Cross-Section

The photoresist is exposed in the ranges 0 < *x* < 2 μm and 3 < *x* < 5 μm

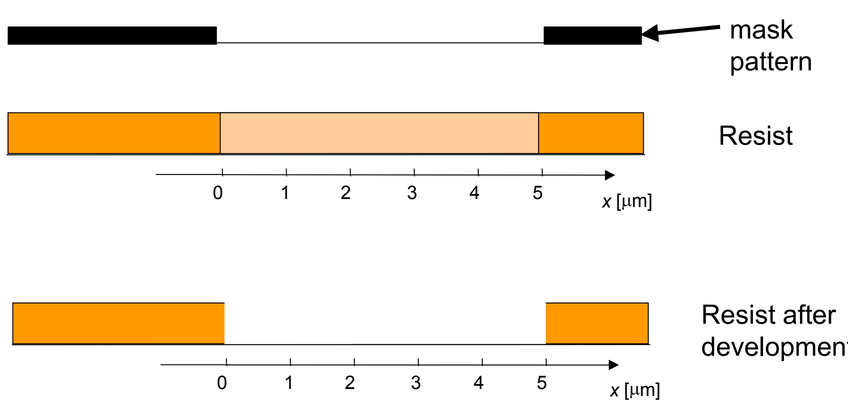


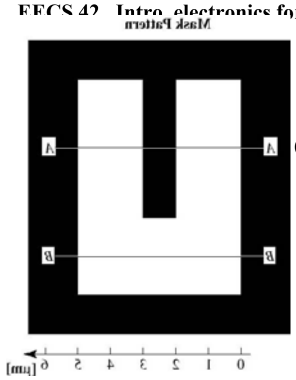
The resist will dissolve in high pH solutions wherever it was exposed



Along "B-B" Cross-Section

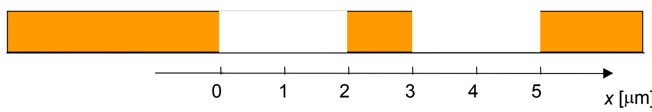
The photoresist is exposed in the ranges 0 < *x* < 5 μm



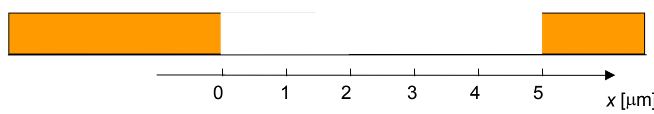


Lithography Process Sequence

Cross sections develop differently along *A-A* and *B-B*



Developed photoresist at A-A



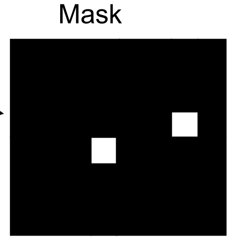
Developed photoresist at B-B

Layout Conventions in CAD*

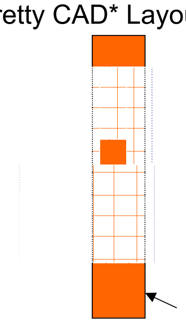
What if the glass plate (physical mask) looks like this?

In this mask almost the whole field is dark ("dark-field mask")

Mask



Pretty CAD* Layout



Pattern from another mask

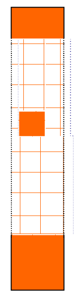
All black with a few holes … CAD layout is all color with the exception of a few holes → ***very* inconvenient to draw and to display**

* CAD = Computer-Aided Design

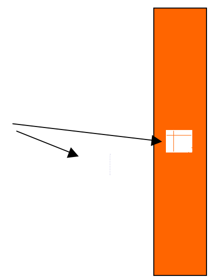
Dark-Field / Light-Field Convention

Dark-field masks block our view of other geometries that lie behind them.

But if we draw the "negative" (or "complement") of masks that are dark-field, the CAD layout is much easier and the overlay of the layer with other mask patterns is easier to display



Draw the "holes" on the layout, ie the clear areas

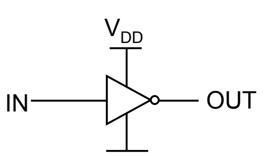


Overlap is clearer – *how to distinguish that CAD layout is the negative of the mask?*

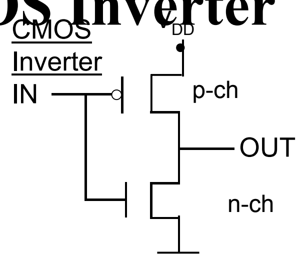
→ Label as "dark field" … "clear field" indicates a "positive" mask

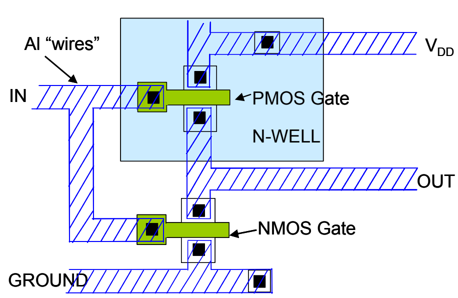
Basic CMOS Inverter

Inverter



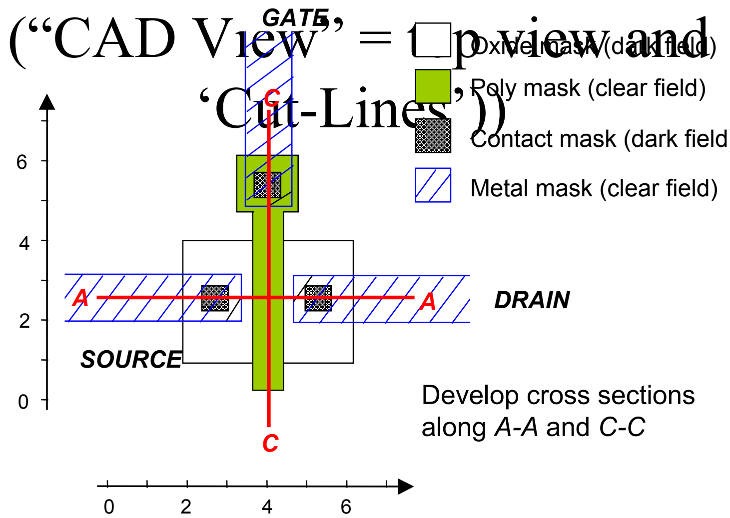
CMOS Inverter





Example layout of CMOS Inverter

NMOS Transistor Layout (“CAD View” = top view and ‘Cut-Lines’))

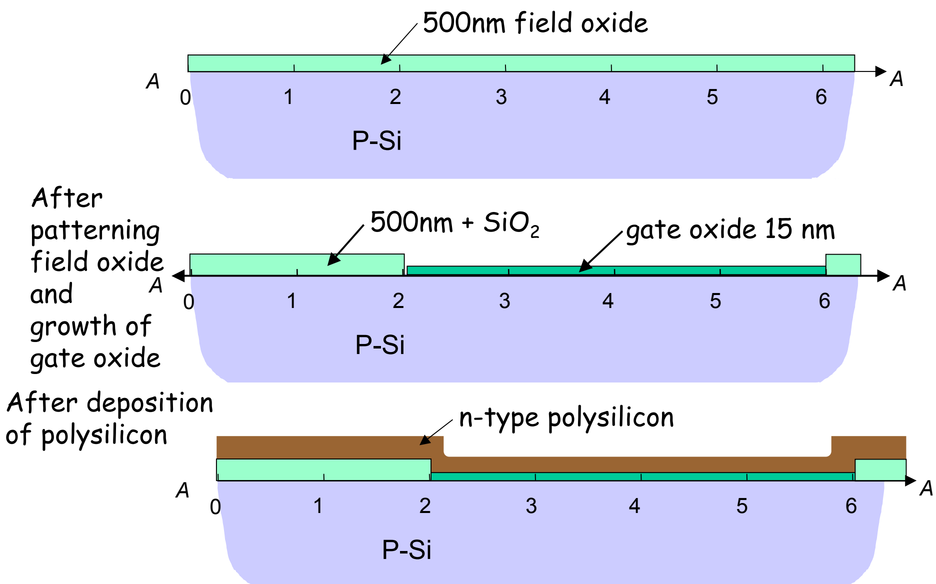


Develop cross sections along *A-A* and *C-C*

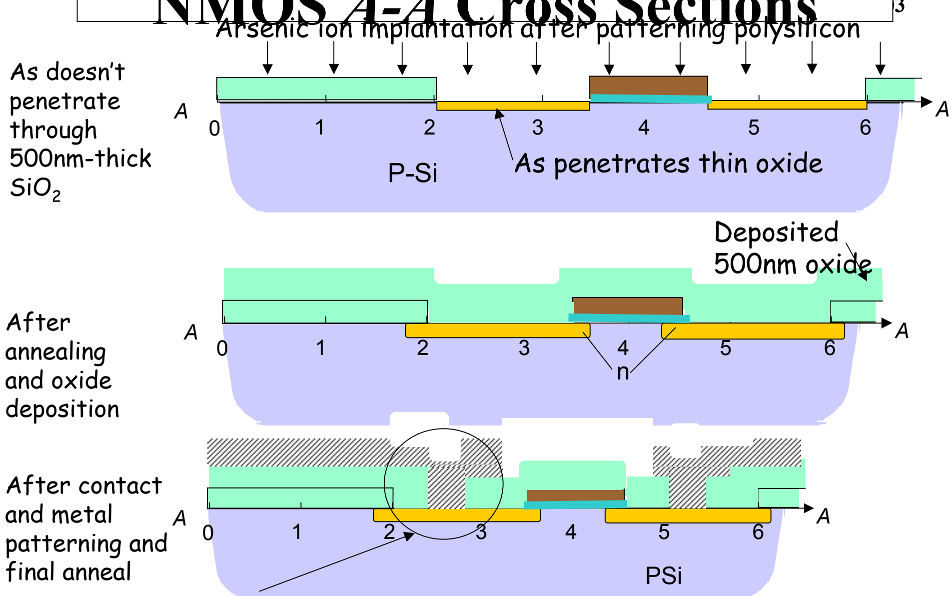
EXAMPLE NMOS Process Sequence

1. Starting material: p-type silicon. Grow 500 nm (5000 Å) of “field” SiO_2
2. Pattern oxide using the oxide mask
3. Grow 15 nm of “gate” SiO_2
4. Deposit 500 nm of n-type polysilicon
5. Pattern poly using the polysilicon mask
6. Implant arsenic (penetrates gate oxide, but not poly or field oxide) and anneal to form source and drain regions
7. Deposit 500 nm of SiO_2
8. Pattern oxide using contact mask (etch sufficiently long to clear oxide from all contact windows)
9. Deposit 1 μm of aluminum
10. Pattern aluminum with metal mask
11. Anneal at 450 °C to heal gate oxide damage and make good Si-Al contacts

NMOS *A-A* Cross Sections

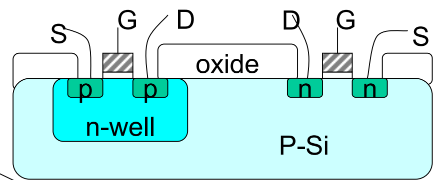


NMOS *A-A* Cross Sections



Note: Step 8 removes gate oxide from contacts to source and drain regions…otherwise, there's no current! (Al **must** touch n-type silicon!)

Conceptual CMOS Process



Start with p-type wafer

Create N-Well

Grow thick oxide

Remove it in transistor areas

Grow gate oxide

Grow and pattern polysilicon for gates

Dope n channel source and drains

Dope p-channel source and drains

Deposit oxide over gates

Pattern contacts

Deposit and Pattern Metal

NEW

Need to protect p-mos areas

Need to protect n-mos areas

It looks like we need three more masks than in NMOS