Calbot Contest Monday 5/12

Jason Gatt and Kevin Ha "Best in Show" in Tutbot/Calbot Contest F00

Lecture Review

Version Date 4/30/03

Review of Basic Circuit Concepts

Sheila Ross

Circuit Analysis
Transients
Logic
Timing Diagrams

Dependent Sources and Op-Amps

Load Line and V_{OUT} vs V_{IN}

Diodes

MOS Operation

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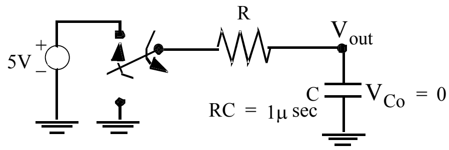
Lecture 7

PULSE: Output is Rising exponential then Falling exponential

Example: Switch rises at t =0, falls at t = 0.1, 1 or 10µsec (Do 1µsec case)

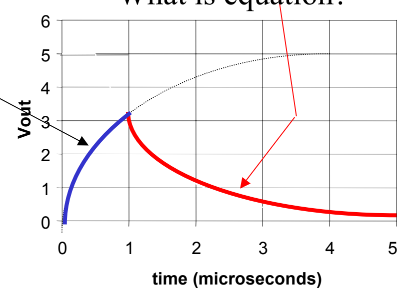


Now starting at 1µsec we are discharging the capacitor so the form is a falling exponential with initial value 3.16 V:

What is equation?

Solution: for RC = 1µsec: during the first rise V obeys:

$$V = 5[1 - e^{\frac{-t}{10^{-6}}}]$$

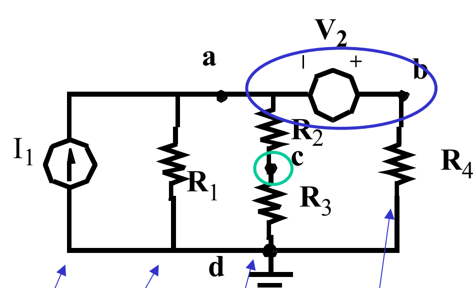


Thus at t = 1µsec, rising voltage reaches

$$5[1 - e^{-1}] = 3.16\text{V}$$

EXAMPLE WITH BOTH SPECIAL CASES

Lecture 8

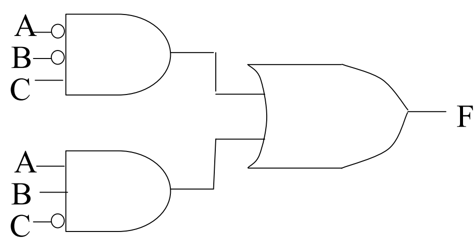


$$I_1 - \frac{V_a}{R_1} - \frac{V_a}{R_2 + R_3} - \frac{(V_a + V_2)}{R_4} = 0$$

How to Combine Gate to Produce a Desired Logic Function? (More basic Logical Synthesis)

Example:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0



$$F = \overline{A}\,\overline{B}\,C + A B \overline{C}$$

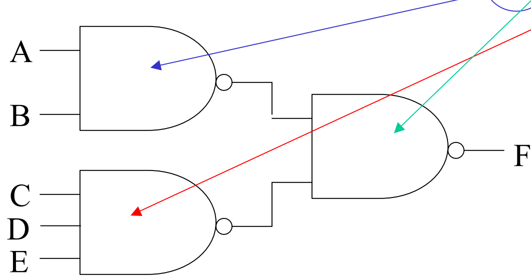
Logical Synthesis Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{\left[\overline{A}\,\overline{B}\,\overline{C}\right]} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{\left[A\,B\,C\right]}$$

Example of Using DeMorgan's Theorem:

$$F = A \bullet B + C \bullet D \bullet E \;= \overline{\overline{AB} \bullet \overline{CDE}}$$



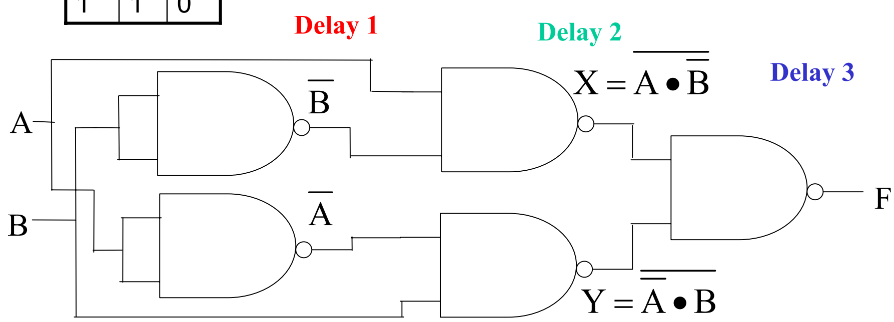
Thus any sum of products expression can be immediately synthesized from NAND gates alone

Logical Synthesis of XOR

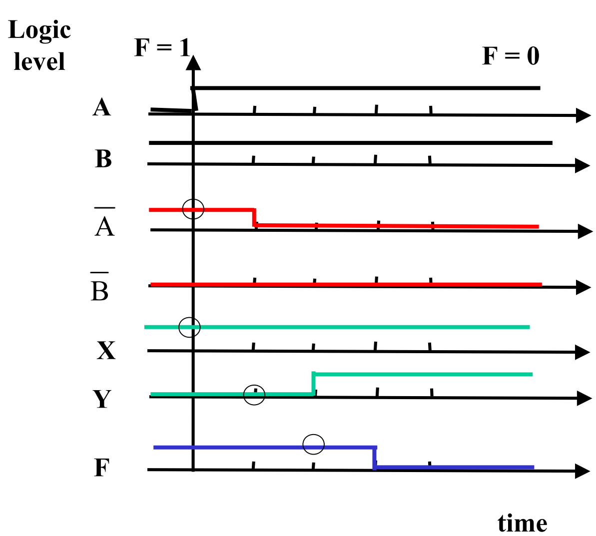
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

$$F = A \bullet \overline{B} + \overline{A} \bullet B$$

We Need a Timing Diagram!

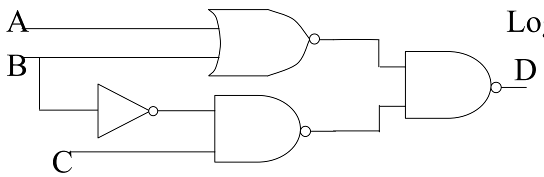


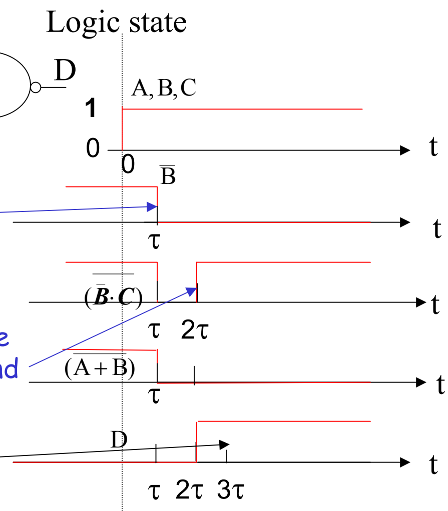
Timing Diagram for Delays in Logic



TIMING DIAGRAMS

Show transitions of variables vs time





Note $\overline{B}$ becomes valid one gate delay after B switches

Note that $(\overline{\overline{B}\cdot C})$ becomes valid two gate delays after B&C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3τ

The 4 Basic Linear Dependent Sources

Lecture 13

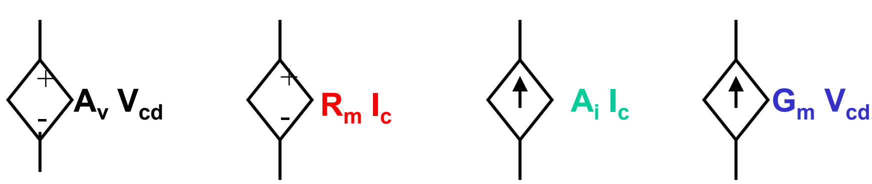
Constant of proportionality | Parameter being sensed | Output

Voltage-controlled voltage source … $V = A_v\ V_{cd}$

Current-controlled voltage source … $V = R_m\ I_c$

Current-controlled current source … $I = A_i\ I_c$

Voltage-controlled current source … $I = G_m\ V_{cd}$

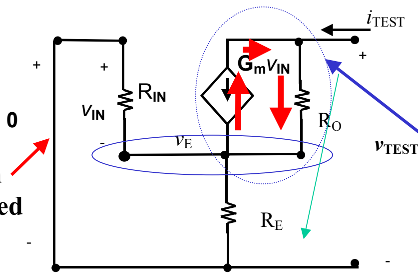


EXAMPLE CIRCUIT: INCREASED OUTPUT RESISTANCE

Add resistor R_E

v = 0

The input has been assumed to be shorted



Try a bag. It is even easier

Analysis: apply i_{TEST} and evaluate v_{TEST}

Unknowns: i_{TEST}, v_{TEST}, v_{IN}, v_E

Need 3 equations to find the ratio of i_{TEST} / v_{TEST}

$v_{IN} = -v_E$ and is not zero!

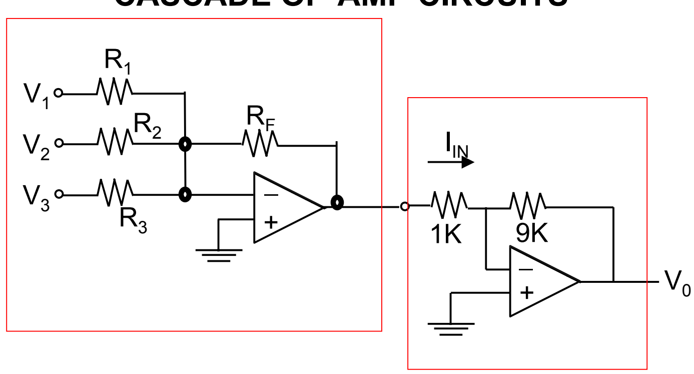
KCL at v_E

KVL at v_{OUT}

Intuitive Explanation: GmV_{IN} burps current which has to also go through R_0. This raises v_{TEST} and the output impedance v_{TEST}/i_{TEST}

Finish this in the homework

CASCADE OP-AMP CIRCUITS



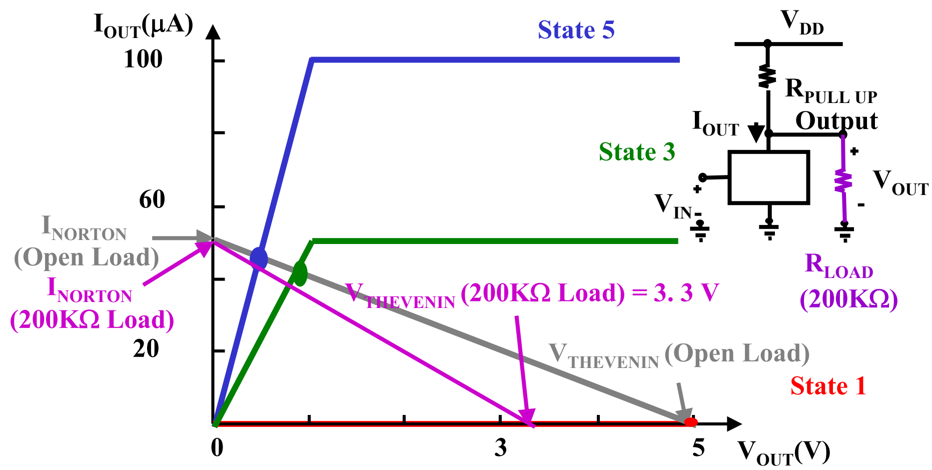
How do you get started on finding V_O?

Hint: Identify Stages

Hint: I_{IN} does not affect V_{O1}

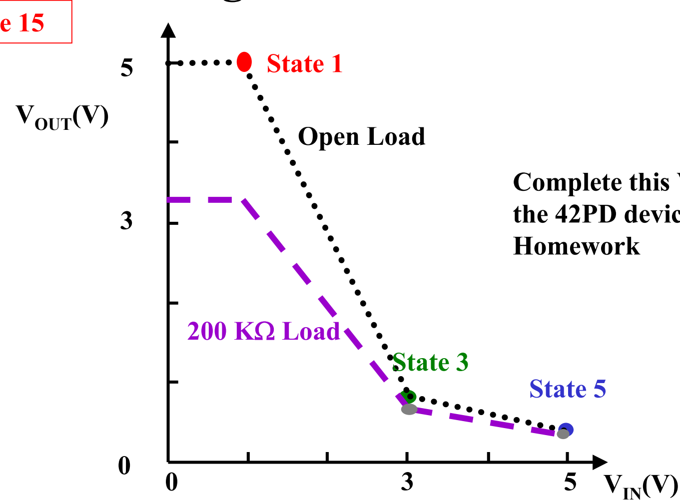
See the further examples of op-amp circuits in the reader

Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground



Voltage Transfer Function for the 42PD Logic Circuit w/wo Load

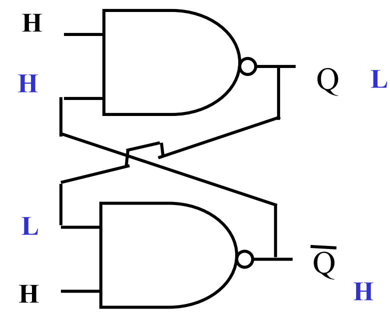
Lecture 15



Complete this VTC for the 42PD device in the Homework

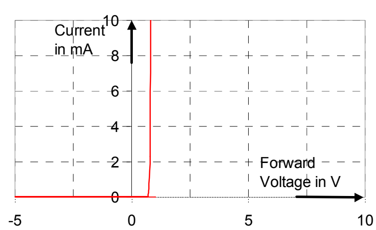
Feedback Can Provide Memory

Lecture 19

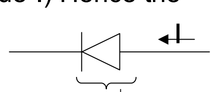


DIODE I-V CHARACTERISTICS AND MODELS

The equation $I = I_0 \exp(qV/kT - 1)$ is graphed below for $I_0 = 10^{-15}$ A

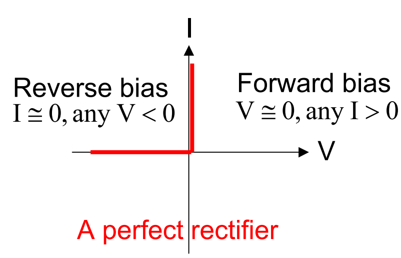


The characteristic is described as a "rectifier" – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a "check value".) Hence the symbol:



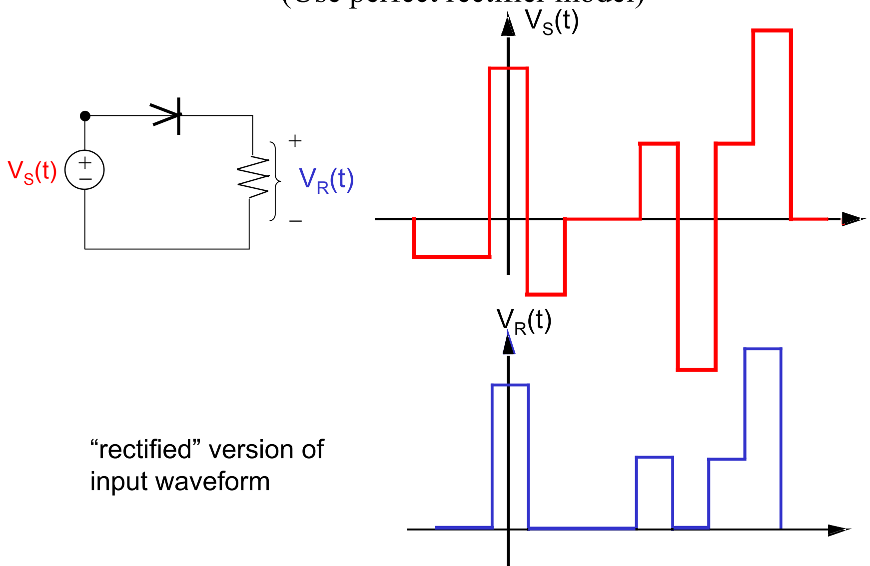
Simple "Perfect Rectifier" Model

If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the "perfect rectifier," whose I-V characteristic is given below:



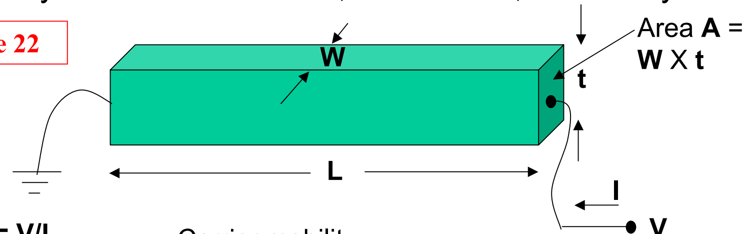
A perfect rectifier

COOL THINGS A DIODE CAN DO
(Use perfect rectifier model)



Physics of Current Flow, Resistance, Resistivity

Lecture 22



E = V/L.

I = V/R

Carrier mobility

Carriers per unit volume

$R = \rho L/A = (1/q\mu N)\ L/W\ t = (L/W)/\mu(qNt)$

But **q N t** has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness **t** when the film has **N** carriers/cm^3 and is **t** units thick. Thus we call **q N t** the "**Q**" and

$R = (L/W)/\mu Q = L/W\ R_\square$

Where $R_\square$ is the resistance of a "square" of the film. Clearly if L is four times W, then R = 4 $R_\square$.

Relation of Current to Physical Parameters

$$I_D = \mu_n C_{ox} \left(\frac{W}{L} \right)_n (V_{GS} - V_T) \cdot V_{OUT-SAT-n}$$

Mobility of carriers

Oxide thickness

Geometrical Layout

Excess Gate drive

Voltage of scattering velocity limit

$$\mu_n = 500 \left(cm^2 / Vs \right) \qquad \mu_p = 150 \left(cm^2 / Vs \right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\left(8.85x10^{-14} F / cm\right)(3.9)}{6x10^{-7} cm} = 5.75x10^{-7} F / cm^2$$

$$V_{OUT-SAT-n} = E_{Crit} \cdot L = 10^4 \left(V / cm \right) \cdot 0.25x10^{-4} cm = 0.25V$$