EECS 42 Introduction to Electronics for Computer Science

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Lecture # 27 Review For Final

Coverage and Emphasis Handout.

A) Diodes with circuits and MOS Resistance
B) Static NMOS and CMOS
C) CMOS resistor model and Delay
D) Worst Case Delay, Timing, Latches
E) Op-Amps and Dependent Sources

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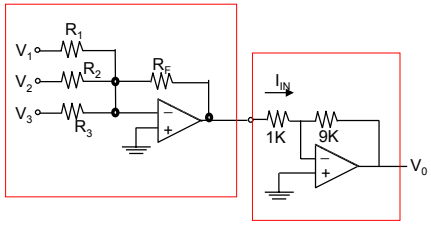
CASCADE OP-AMP CIRCUITS



How do you get started on finding V_O?

Hint: Identify Stages

Hint: I_{IN} does not affect V_{O1}

See the further examples of op-amp circuits in the reader

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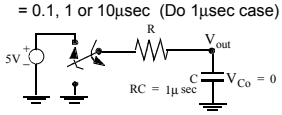
Lecture 7

PULSE: Output is Rising exponential then Falling exponential

Example: Switch rises at t =0, falls at t = 0.1, 1 or 10μsec (Do 1μsec case)



Solution: for RC = 1μsec: during the first rise V obeys:

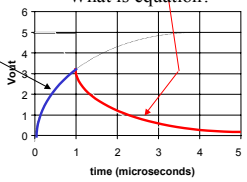
$$V = 5[1 - e^{\frac{-t}{10^{-6}}}]$$

Thus at t = 1μsec, rising voltage reaches

$$5[1 - e^{-1}] = 3.16V$$

Now starting at 1μsec we are discharging the capacitor so the form is a falling exponential with initial value 3.16 V:

What is equation?



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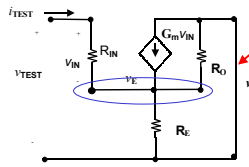
EXAMPLE CIRCUIT: INCREASED INPUT RESISTANCE

Lecture 20

Add resistor R_E



The output has been assumed to be shorted $v_{OUT} = 0$

Analysis: apply i_{TEST} and evaluate v_{TEST}

$$v_{IN} = R_{IN} i_{TEST} \qquad v_{TEST} = R_{IN} i_{TEST} + v_E$$

Similar to the homework

KCL $\dfrac{v_E}{R_E} + \dfrac{v_E}{R_0} - i_{TEST} - G_m R_{IN} i_{TEST} = 0$

Check for special case for R_0 infinite $\dfrac{v_{TEST}}{i_{TEST}} = R_{IN} + (1 + G_m R_{IN}) R_E$

Intuitive Explanation: R_E puts R_{IN} on a node whose voltage increases in response to current in R_{IN}.

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EXAMPLE WITH BOTH SPECIAL CASES

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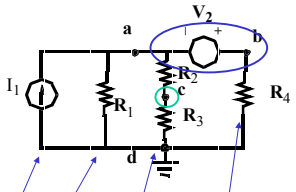

$$I_1 - \frac{V_a}{R_1} - \frac{V_a}{R_2 + R_3} - \frac{V_a + V_2}{R_4} = 0$$

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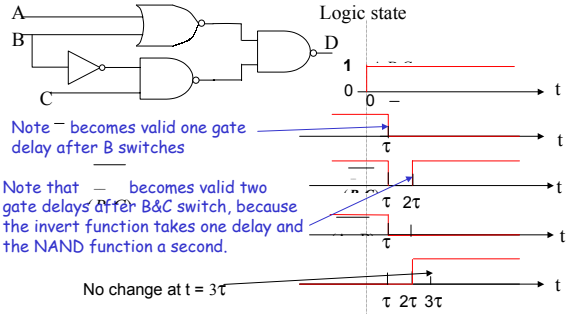
Lecture 12

TIMING DIAGRAMS

Show transitions of variables vs time



Note $\overline{}$ becomes valid one gate delay after B switches

Note that $\overline{}$ becomes valid two gate delays after B&C switch, because the invert function takes one delay and the NAND function a second.

No change at t = 3τ

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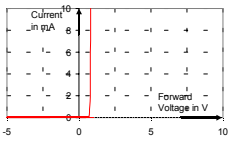
Lecture 23

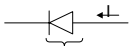
DIODE I-V CHARACTERISTICS AND MODELS

The equation $I = I_0 \exp(qV/kT - 1)$

is graphed below for $I_0 = 10^{-15}$ A

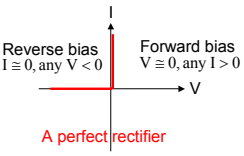


The characteristic is described as a "rectifier" – that is, a device that permits current to pass in only one direction. (The hydraulic analog is a "check value".) Hence the symbol:



Simple "Perfect Rectifier" Model

If we can ignore the small forward-bias voltage drop of a diode, a simple effective model is the "perfect rectifier," whose I-V characteristic is given below:



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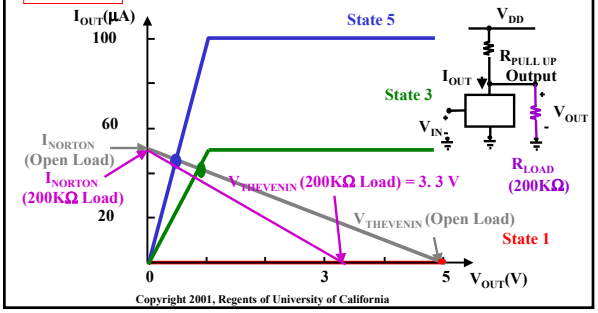
Composite Current Plot for the 42PD Circuit with 200kΩ Load to Ground

Lecture 16



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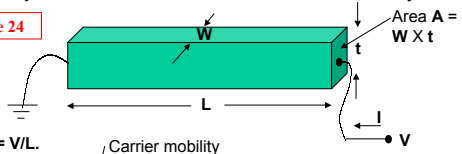
Physics of Current Flow, Resistance, Resistivity

Lecture 24



E = V/L.

I = V/R

Carrier mobility

Carriers per unit volume

R = ρL/A =(1/q μN) L/W t = (L/W) /μ(qNt)

But **q N t** has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness **t** when the film has **N** carriers/cm^3 and is **t** units thick. Thus we call **q N t** the "**Q**" and

R = (L/W)/ μQ = L/W $R_{\square}$

Where $R_{\square}$ is the resistance of a "square" of the film. Clearly if L is four times W, then R = 4 $R_{\square}$.

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Voltage Transfer Function for the 42PD Logic Circuit w/wo Load

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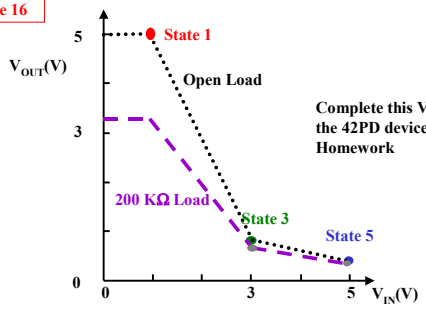

Complete this VTC for the 42PD device in the Homework

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Lecture 17

Saturation Current NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD}) V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

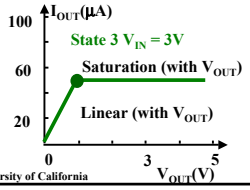
Example:

k_D = 25 μA/V²

V_{TD} = 1V

$V_{OUT-SAT-D}$ = 1V

Use these values in the homework.



$I_{OUT-SAT-PD} = 25 \frac{\mu A}{2} (3V - 1V)^2 = 50 \mu A$

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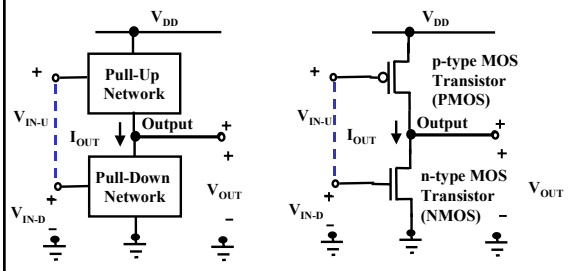
Lecture 17

Transistor Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.



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Composite I_{OUT} vs. V_{OUT} for CMOS

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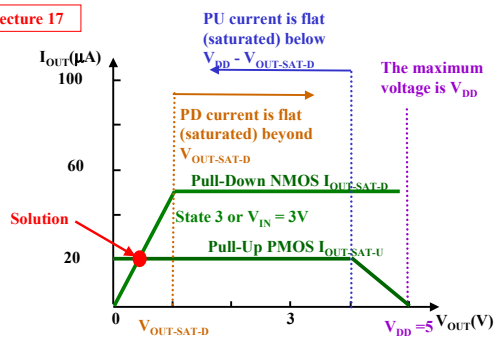

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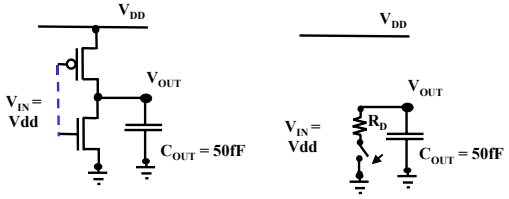
Lecture 18

Inverter Propagation Delay

Discharge (pull-down)



$\Delta t = 0.69 R_D C_{OUT} = 0.69(10k\Omega)(50fF) = 345$ ps

Discharge (pull-up)

$\Delta t = 0.69 R_U C_{OUT} = 0.69(10k\Omega)(50fF) = 345$ ps

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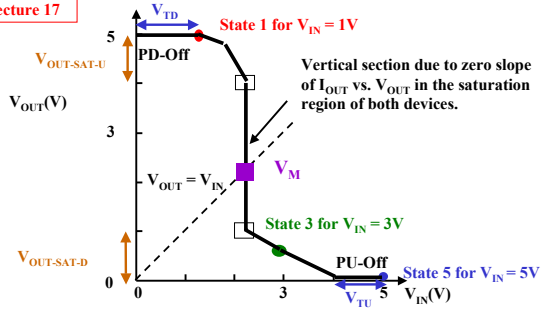
Voltage Transfer Function for the Complementary Logic Circuit

Lecture 17



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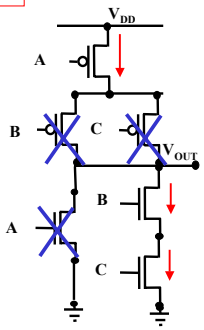
Lecture 18

CMOS Logic Gate: Example Inputs

A = 0
B = 1
C = 1



PMOS A conducts; B and C Open

Output is High

= 0

NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

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¾ V_{DD}/I_{SAT} Physical Interpretation

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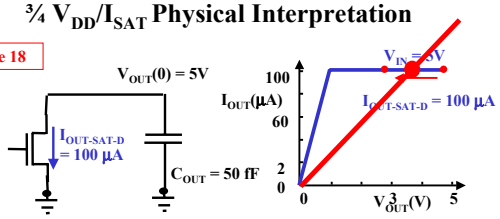

¾ V_{DD} is the average value of V_{OUT}

Approximate the NMOS device curve by a straight line from (0,0) to ($I_{OUT-SAT-D}$, ¾ V_{DD}).

Interpret the straight line as a resistor with

slope = $1/R = ¾ V_{DD}/I_{SAT}$

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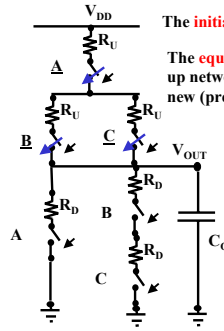
Lecture 19

Logic Gate Propagation Delay: Initial State



The initial state depends on the old (previous) inputs.

The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to V_{DD} for a long time and the capacitor has precharged up to V_{DD} = 5V.

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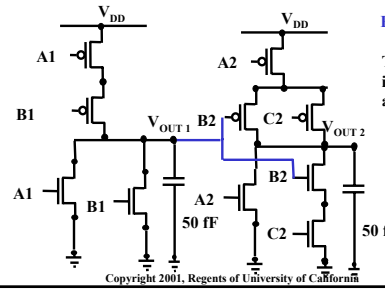
Lecture 20

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



$B2 = V_{OUT\ 1}$

The four independent input are A1, B1, A2 and C2.

A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

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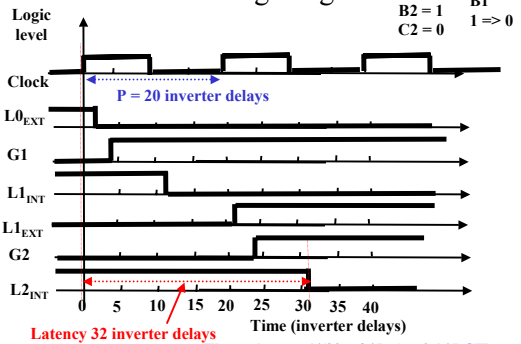
Lecture 22

Latch Timing Diagram

A1 = 0
B2 = 1
C2 = 0
B1
1 => 0



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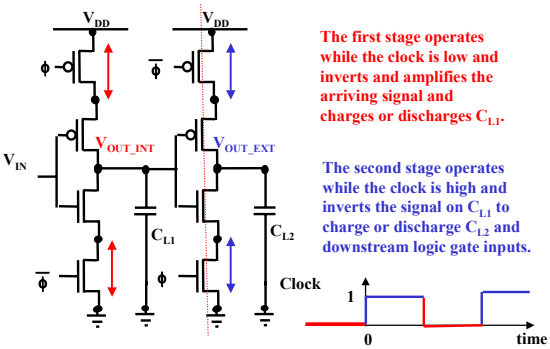
Lecture 21

Latch Work Best In Pairs



The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges C_{L1}.

The second stage operates while the clock is high and inverts the signal on C_{L1} to charge or discharge C_{L2} and downstream logic gate inputs.

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Lecture 22

Latency and Throughput

Latency L is the delay between the rising edge of the clock on L0 and the data being valid internally in the last latch.

$$L_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT} = 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$$

$$L_{PIPLINED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{L\_INT} + \tau_{L\_EXT} + \tau_{GATE2} + \tau_{L\_INT} = 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 12\tau_{INV}$$

Throughput T is the bits per second through the latches and is the maximum clock frequency.

$$P_{LUMPED} = \tau_{L\_EXT} + \tau_{GATE1} + \tau_{GATE2} + \tau_{L\_INT} = 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 8\tau_{INV}$$

F_{LUMPED} =1/8(345ps) = 0.36 GHz

$$P_{PIPELINED} = \tau_{L\_EXT} + MAX(\tau_{GATE1}, \tau_{GATE2}) + \tau_{L\_INT} = 2\tau_{INV} + 2\tau_{INV} + 2\tau_{INV} = 6\tau_{INV}$$

$F_{PIPLINED}$ =1/6(345ps) = 0.48 GHz

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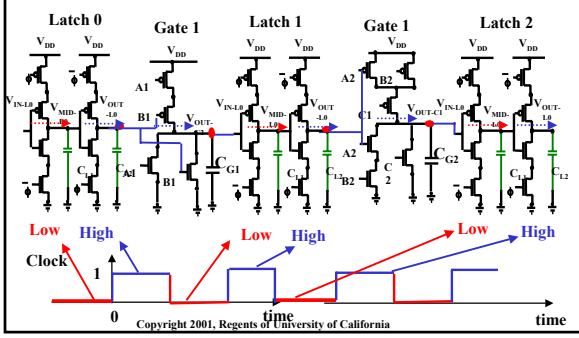
Lecture 22

Latch Operation: Pipelined



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Lecture 25: on blackboard

Limitations of Power Consumption

- The resistive load of NMOS results in D.C. current and hence static power consumption given by the product of current times voltage.
- CMOS avoids this static loss as the pull-up device shuts off the current completely.
- CMOS still suffers a.c. power consumption that is proportional to the switching frequency.
- The energy expended per cycle of in charging and discharging can never be less than CV^2

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