University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE141/CS150 V. Stojanovic, J. Wawrzynek
Fall 2014 10/16/14

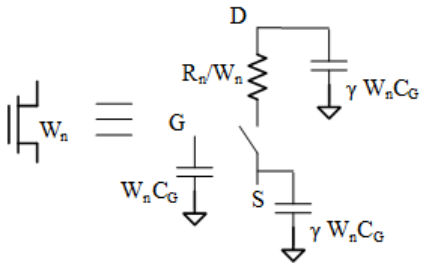
Midterm Exam

Name: _____

ID number: _____

This is a *closed-book* exam, but you are allowed a single sheet of notes. Calculators *are* allowed, but no phones, pads, or laptops. Each question is marked with its number of points (one point per expected minute of time). Start by answering the easier questions then move on to the more difficult ones. You can tear off the spare pages at the end of the booklet and/or use the backs of the pages to work out your answers. Neatly copy your answer to the allocated places. **Neatness counts.** We will deduct points if we need to work hard to understand your answer.

For all relevant problems, assume the following transistor switch model:

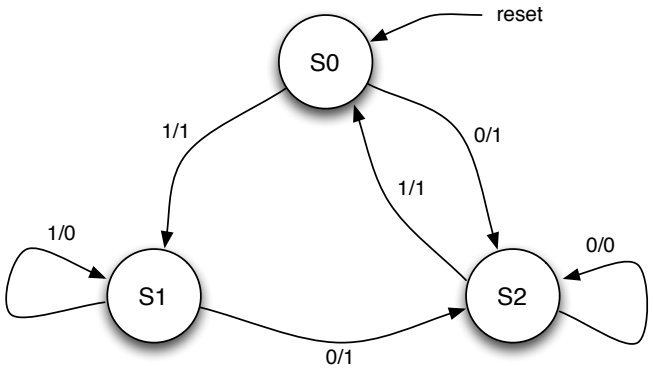


Put your name and SID on each page.

problem	maximum	score
1	12pts	
2	6pts	
3	10pts	
4	12pts	
5	6pts	
6	8pts	
7	10pts	
8	6pts	
9	10pts	
10 (EE241a only)	15pts	
Total		

1. [12pts] Verilog.

   In the space below write out the Verilog code for a module that implements an FSM with the behavior of the following state transition diagram. The FSM has a one-bit wide input named `x` and a one-bit wide output named `y`. The arcs in the diagram are labeled with values for `x` and `y` as "`x/y`".



2. [6pts] Boolean Optimization.

Find the minimal sum-of-products form for the following Boolean function. *Hint: use a K-map.*

$$f = \overline{a}b\overline{c}d + \overline{a}bcd + ab\overline{c}d + abcd + \overline{a}\overline{b}c\overline{d} + \overline{a}bc\overline{d} + a\overline{b}c\overline{d}$$

3. [10pts] Combinational Logic Design.

Consider the design of the combinational logic block that takes as input an unsigned 3-bit integer, X, and produces a 2-bit integer output, Y, where $Y = X mod\ 3$.

(a) Derive Boolean expressions that represent the output signals, y_0 (the least significant bit) and y_1 (the most significant bit) in terms of the inputs x_2, x_1, x_0. You don't need to simplify the equations.

(b) In the space below neatly draw the gate-level circuit diagram for y_0. Use simple logic gates with any number of inputs.

4. [12pts] Finite State Machine Design.

   Consider a finite state machine circuit designed to compare 2 4-bit strings. The circuit accepts one bit at a time from each string over 4 clock periods. It produces a 0 at its output as long as the strings match in less than 2 bit positions and produces a 1 at its output once they match in 2 or more bit positions. After 4 clock cycles, the output stays constant until the reset signal is set to 1 to re-initialize the circuit.

   (a) Draw a state transition diagram for the finite state machine.

   (b) Write down the logic equations for combinational logic parts of the circuit. Assume that you are using flip-flops with a built-in reset.

5. [6pts] CMOS Logic.

Draw the single, complex gate, transistor level CMOS representation of the following functions:

(a) $F = \overline{(AB + C)D}$

(b) $F = (\overline{A} + \overline{B})\overline{C}$

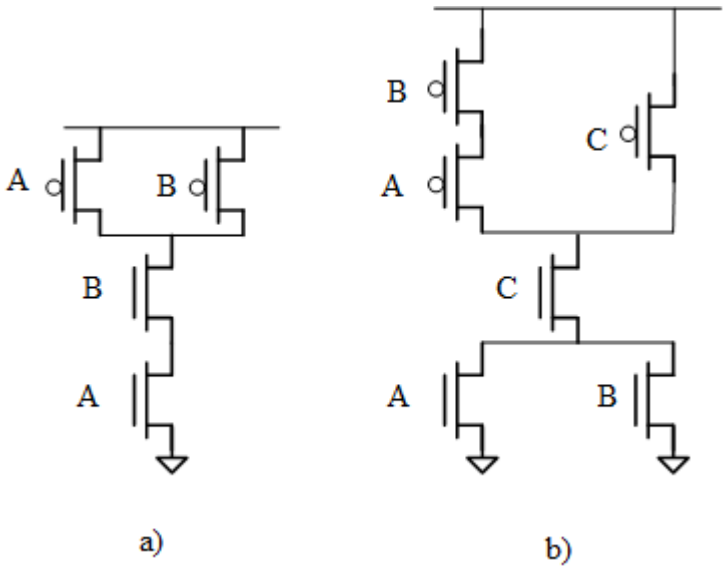
6. [8pts] Gate sizing and function.

1 Size the following gates for equal pull-up and pull-down resistance.

2 Determine the logical effort of each gate input.

3 Determine the logic function of each gate.

Assume that in this technology NMOS and PMOS devices have the same mobility (i.e. for $W_p = W_n$, $R_p = R_n$).



7. [10pts] Voltage Transfer Characteristics (VTCs).

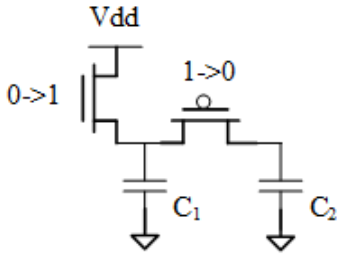
You are a new college graduate in Low-Joule Inc. (A low-power microprocessor company). Their technology has the following parameters: $V_{th,N} = 0.3V$ and $|V_{th,P}| = 0.4V$, $R_n = 2k\Omega * \mu m$, $R_P = 3k\Omega * \mu m$ at $V_{dd} = 1V$.

(a) Draw the voltage transfer characteristics of the inverter with $W_n = W_p = 1\mu m$ and label V_{OL}, V_{IL}, V_{OH}, and V_{IH}. Determine the noise margins N_{MH} and N_{ML}. Determine the short-circuit current that flows through both transistors during input transition from 0 to V_{dd}.

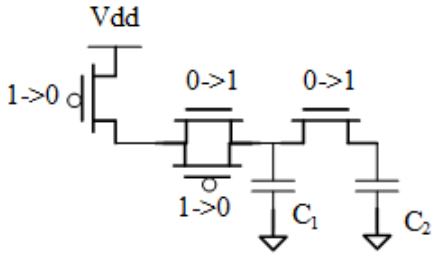
(b) In attempt to save on short-circuit current, you propose to operate the circuit at $0.6V$. Draw a separate VTC for a raising and a falling transition marking the V_{OL}, V_{IL}, V_{OH}, V_{IH} where applicable. Determine the noise margins N_{MH} and N_{ML}. Determine the short-circuit current that flows through both transistors during input transition from 0 to V_{dd}. Assume that at $V_{dd} = 0.6V$ transistor on resistances $R_n = 5k\Omega * \mu m$ and $R_p = 15k\Omega * \mu m$.

8. [6pts] Switching.

Determine the switching energy drawn from the supply for the following circuits (neglect all capacitances except C_1 and C_2 shown on the schematics). Assume $V_{th,N} = 0.3V$ and $|V_{th,P}| = 0.4V$ and $V_{dd} = 1V$. Assume voltage on all the capacitors is $0V$ prior to the switching event. Label the voltages at each node in the circuit after the switching event.



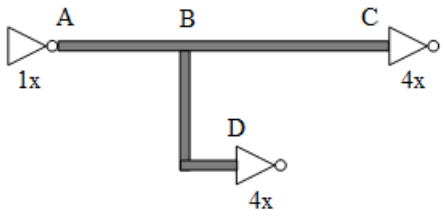
a)



b)

9. [10pts] Gates and Wires.

Calculate the delay from point A to point C in the circuit below. Assume that $R_{wire} = 5\Omega/\square$ and $C_{wire} = 0.2fF/\mu m$, $R_n = 2k\Omega * \mu m$, $R_p = 4k\Omega * \mu m$, $\gamma = 1$, $C_G = 1fF/\mu m$. The unit-size (1x) inverter at point A has $W_p = 2W_n = 2\mu m$. The inverters at points C and D are size 4x. For calculations, use the π-model of the wire, for each wire segment. Wire segment AB is $100\mu m$ long, segment BC is $900\mu m$ long, and segment BD is $200\mu m$ long. Wire width is $1\mu m$.



(a) Draw the RC schematics of the circuit above and label all the resistances and capacitances.

(b) Calculate the values of all the resitances and capacitances in part a).

(c) Write the delay formula for the delay from point A to point C in terms of the resistance and capacitance labels (not numbers) from part a).

10. **Extra problem for EE241A students** [15pts]

You are a new college graduate at Road Runner, Inc.—a high-performance processor startup. Your first task is to design a buffer circuit that will minimize the delay between an inverter of size $W_p = 2W_n = 1\mu m$ and the microprocessor bus wire load of $C_L = 200fF$. Assume that $R_p = 2k\Omega * \mu m$, $R_n = 1k\Omega * \mu m$, $\gamma = 1$ and $C_G = 1fF/\mu m$.

Having taken EE241A, you jump right at it and determine the number of inverters needed to minimize the delay, keeping the $W_p/W_n = 2$ sizing in each inverter for equal pull-up and pull-down. You also pay attention to not inverting the logic function.

(a) How many inverter stages need to be inserted to minimize the delay?

(b) Given the number of stages in a), determine the delay value.

(c) After determining the optimal number of stages, you run-off to your boss and tell her about the solution. She smiles and says she can do even better by sizing all the buffering inverters at a W_p/W_n = 1 ratio. Determine the logical effort of one inverter pair (back-to-back inverters) sized with W_p/W_n = 1 ratio, compared to your standard inverter with W_p/W_n = 2 ratio.

(d) Now determine the number of inverter stages with a W_p/W_n = 1 ratio, which are inserted to minimize the delay.

(e) What is the delay value given the number of inverter stages in d)?

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